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Data Sheet, DS 1, Nov. 2001

T-SMINTI

4B3T Second Gen. Modular ISDN NT (Intelligent)

PEF 82902 Version 1.1

Wired Communications

Infineon technologies

Never stop thinking.

Edition 2001-11-09

Published by Infineon Technologies AG,
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Data Sheet, DS 1, Nov. 2001

T-SMINTI

4B3**T** **S**econd Gen. **M**odular **I**SDN **NT** (**I**ntelligent)

PEF 82902 Version 1.1

Wired Communications

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Page	Subjects (major changes since last revision)
Table 18 **Figure 41** **Chapter 2.4.7.4**	Additional C/I-command LTD
Chapter 3.2.3 **Chapter 4.3** **Chapter 4.9.4**	The Framer / Deframer Loopback (DLB) is no more supported
Chapter 4.3	Reset value of MASKU is FFh (not 00h)
Chapter 4.3 **Chapter 4.9.8**	Reset value of FW-Version is 3Eh
Chapter 4.9.4	Restriction of LOOP.LB1, LB2 and LBBD to Transparent state
Chapter 5.2	Input Leakage Current AIN, BIN: max. 30µA
Chapter 5.4	Reduced power consumption

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1 Overview

The **PEB 82902** (T-SMINT®I) offers U-transceiver, S-transceiver and an IOM®-2 interface. A microcontroller interface provides access to both transceivers as well as the IOM®-2 interface.

However, as opposed to its bigger brother T-SMINT®IX, the T-SMINT®I does not have an HDLC controller. Main target applications of the T-SMINT®I are intelligent NT applications where the HDLC controller(s) is (are) provided by the microcontroller. An example for such a microcontroller is the Infineon UTAH chip which features four flexible HDLC controllers.

Table 1 on **Page 1** summarizes the 2nd generation NT products.

Table 1 NT Products of the 2nd Generation

	PEF 80902	PEF 81902	PEF 82902
	T-SMINT®O	**T-SMINT®IX**	**T-SMINT®I**
Package	P-MQFP-44	P-MQFP-64 P-TQFP-64	P-MQFP-64 P-TQFP-64
Register access	no	U+S+HDLC+ IOM®–2	U+S+IOM®–2
Access via	n.a	parallel (or SCI or IOM®–2)	parallel (or SCI or IOM®–2)
MCLK, watchdog timer, SDS, BCL, D-channel arbitration, IOM®–2 access and manipulation etc. provided	no	yes	yes
HDLC controller	no	yes	no
NT1 mode available	yes (only)	no	no

1.1 References

[1] TS 102 080, Transmission and Multiplexing; ISDN basic rate access; Digital transmission system on metallic local lines, ETSI, November 1998

[2] FTZ 1 TR 220 Technische Richtlinie, Spezifikation der ISDN Schnittstelle Uk0 Schicht 1, Deutsche Telecom AG, August 1991

[3] TS 0284/96 Technische Spezifikation Intelligenter Netzabschluß (iNT) mit den Funktionen eines Terminaladapters TA 2a/b (ohne Internverkehr), Deutsche Telekom AG, März 2001

[4] pr ETS 300 012 Draft, ISDN; Basic User Network Interface (UNI), ETSI, November 1996

[5] T1.605-1991, ISDN-Basic Access Interface for S and T Reference Points (Layer 1 Specification), ANSI, 1991

[6] I.430, ISDN User-Network Interfaces: Layer 1 Recommendations, ITU, November 1988

[7] IEC-T, ISDN Echocancellation Circuit, PEB 20901 (IEC - TD) / PEB 20902 (IEC - TA), preliminary Target Specification 11.88, Siemens AG, 1988

[8] SBCX, S/T Bus Interface Circuit Extended, PEB 2081 V3.4, User's Manual 11.96, Siemens AG, 1996

[9] NTC-T, Network Termination Controller (4B3T), PEB 8090 V1.1, Data Sheet 06.98, Siemens AG, 1998

[10] INTC-Q, Intelligent Network Termination Controller (2B1Q), PEB 8191 V1.1, Data Sheet 10.97, Siemens AG, 1997

[11] Q-SMINTO, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(O**rdinary), PEF 80912
Q-SMINTIX, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent e**X**tended), PEF 81912
Q-SMINTI, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent), PEF 82912 V1.3, Data Sheets 03.01, Infineon AG, 2001

[12] IOM®-2 Interface Reference Guide, Siemens AG, 03.91

[13] SCOUT-S(X), Siemens Codec with S/T-Transceiver, PSB 2138x V1.1, Preliminary Data Sheet 08.98, Infineon Technologies AG, 1999

[14] PITA, PCI Interface for Telephony/Data Applications V0.3, SICAN GmbH, September1997

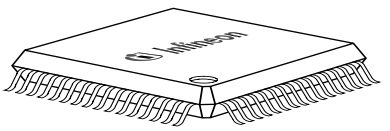
[15] Dual Channel SLICOFI-2, HV-SLIC; DUSLIC; PEB3265, 4265, 4266; Data Sheet DS2, Infineon Technologies, July 2000.

T-SMINT®I **PEF 82902**

4B3T Second Gen. Modular ISDN NT (Intelligent)

Version 1.1 **CMOS**

1.2 Features



P-MQFP-64-

P-TQFP-64·

Features known from the PEB 8090

- U-transceiver and S-transceiver on one chip
- U-interface (4B3T) conform to ETSI [1] and FTZ [2]:
  - Meets all transmission requirements on all ETSI and FTZ loops with margin
- S/T-interface conform to ETSI [4], ANSI [5] and ITU [6]
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
- Access to IOM®-2 C/I and Monitor channels
- Power-on reset and Undervoltage Detection with no external components
- ESD robustness 2kV

New Features

- Conforms to 'Technische Spezifikation Intelligenter Netzabschluß (iNT) mit den Funktionen eines Terminaladapters TA 2a/b' of Deutsche Telekom AG [3]
- Perfectly suited for high-end intelligent NTs that require multiple HDLC controllers
- Pin compatible with Q-SMINT®I (2nd Generation)
- Parallel or serial µP-interface
  - Siemens/Intel non-multiplexed (direct or indirect addressing (SCOUT))
  - Siemens/Intel multiplexed
  - Motorola
  - programmable MCLK (can be disabled) (SCOUT)

Type	Package
PEF 82902	P-MQFP-64
PEF 82902	P-TQFP-64

- Enhanced IOM®–2 interface
  - Timeslot access and manipulation (SCOUT)
  - BCL output; programmable and flexible strobes SDS1/2, e.g. active during several timeslots.
  - Optional: All registers can be read and written to via new Monitor channel concept
  - External Awake ($\overline{\text{EAW}}$)
- Optional: Implementation of S-transceiver statemachine in software
- Power Down and reset states (e.g. S-transceiver) for individual circuits
- Automatic D-channel arbitration between S-bus and external HDLC controller
- Priority setting (8/10) for off-chip HDLC controller
- Pin Vref and the according external capacitor removed
- Inputs accept 3.3V and 5V
- I/O (open drain) accepts pull-up to 3.3V[1)]
- Lowest power consumption due to
  - Low power CMOS technology (0.35µ)
  - Newly optimized low power libraries
  - High output swing on U- and S-line interface leads to minimized power consumption
  - Single 3.3 Volt power supply

1.3 Not Supported are ...

- No integrated hybrid is provided by the T-SMINT®I. Therefore, an external hybrid is always required, which consists of only two additional resistors as compared to an integrated hybrid, but allows for more flexibility in board design.
- On-chip HDLC controller
- Auxiliary IOM®–2 interface
- SRA (capacitive receiver coupling is not suited for S-feeding)
- NT-Star with star point on the IOM®-2 bus (already not supported in NTC-T).
- No access to S2-5 channels. Access only to S1 and Q channel as in Scout-S. No selection betweeen transparent and non-auto mode provided.

1) Pull-ups to 5V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

1.4 Pin Configuration

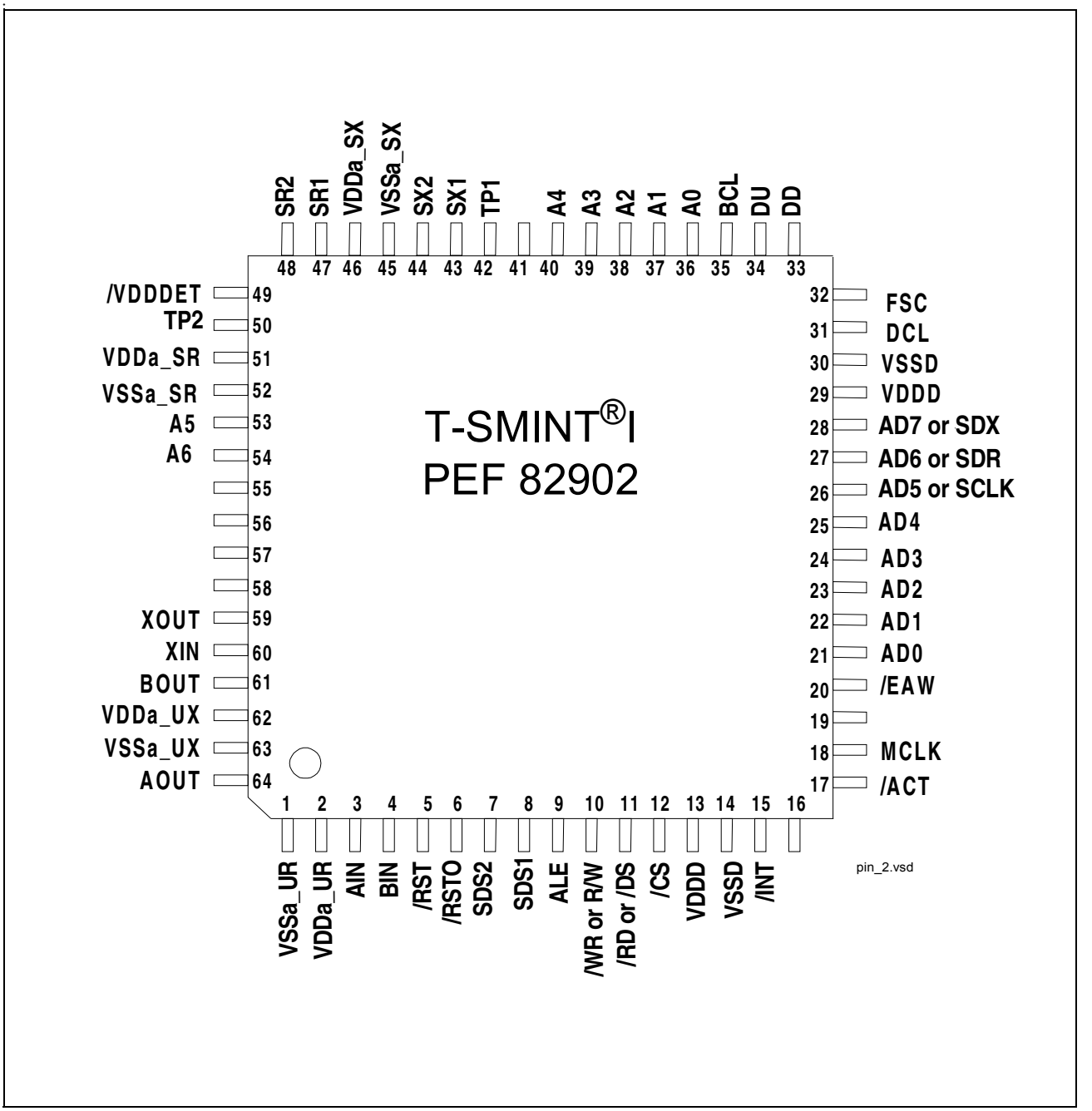


Figure 1 Pin Configuration

1.5 Block Diagram

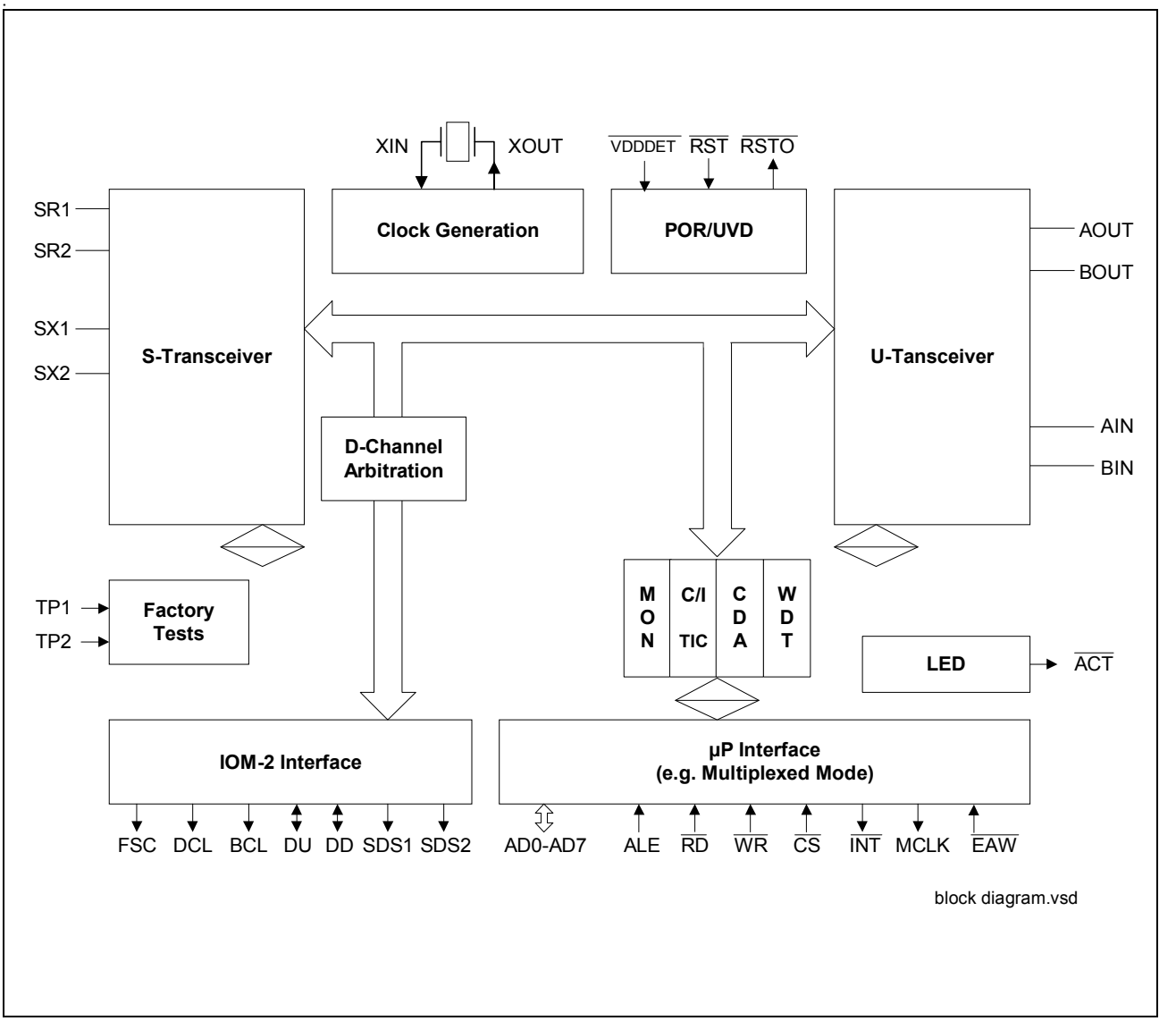


Figure 2 Block Diagram

1.6 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

	Pin	Symbol	Type	Function
	2	VDDa_UR	–	Supply voltage for U-Receiver (3.3 V ± 5 %)
	1	VSSa_UR	–	Analog ground (0 V) U-Receiver
	62	VDDa_UX	–	Supply voltage for U-Transmitter (3.3 V ± 5 %)
	63	VSSa_UX	–	Analog ground (0 V) U-Transmitter
	51	VDDa_SR	–	Supply voltage for S-Receiver (3.3 V ± 5 %)
	52	VSSa_SR	–	Analog ground (0 V) S-Receiver
	46	VDDa_SX	–	Supply voltage for S-Transmitter (3.3 V ± 5 %)
	45	VSSa_SX	–	Analog ground (0 V) S-Transmitter
	29	VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
	30	VSSD	–	Ground (0 V) digital circuits
	13	VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
	14	VSSD	–	Ground (0 V) digital circuits
	32	FSC	O	**Frame Sync:** 8-kHz frame synchronization signal
	31	DCL	O	**Data Clock:** IOM®-2 interface clock signal (double clock): 1.536 MHz
	35	BCL	O	**Bit Clock:** The bit clock is identical to the IOM®-2 data rate (768 kHz)
	33	DD	I/O OD	**Data Downstream:** Data on the IOM®-2 interface
	34	DU	I/O OD	**Data Upstream:** Data on the IOM®-2 interface

Table 2 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	8	SDS1	O	**Serial Data Strobe1:** Programmable strobe signal for time slot and/or D-channel indication on IOM®-2
	7	SDS2	O	**Serial Data Strobe2:** Programmable strobe signal for time slot and/or D-channel indication on IOM®-2
	12	$\overline{CS}$	I	**Chip Select:** A low level indicates a microcontroller access to the T-SMINT®I
	26	SCLK	I	**Serial Clock:** Clock signal of the SCI interface if a serial interface is selected
	26	AD5	I/O	**Multiplexed Bus Mode:** **Address/data bus** Address/data line AD5 if the parallel interface is selected **Non-Multiplexed Bus Mode:** **Data bus** Data line D5 if the parallel interface is selected
	27	SDR	I	**Serial Data Receive:** Receive data line of the SCI interface if a serial interface is selected
	27	AD6	I/O	**Multiplexed Bus Mode:** **Address/data bus** Address/data line AD6 if the parallel interface is selected **Non-Multiplexed Bus Mode:** **Data bus** Data line D6 if the parallel interface is selected

Table 2 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	28	SDX	OD/O	**Serial Data Transmit:** Transmit data line of the SCI interface if a serial interface is selected
	28	AD7	I/O	**Multiplexed Bus Mode:** **Address/data bus** Address/data line AD7 if the parallel interface is selected **Non-Multiplexed Bus Mode:** **Data bus** Data line D7 if the parallel interface is selected
	21 22 23 24 25	AD0 AD1 AD2 AD3 AD4	I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the microcontroller to the T-SMINT®I and data between the microcontroller and the T-SMINT®I. **Non-Multiplexed Bus Mode:** **Data bus.** Transfers data between the microcontroller and the T-SMINT®I (data lines D0-D4).
	36 37 38 39 40 53 54	A0 A1 A2 A3 A4 A5 A6	I I I I I I I	**Non-Multiplexed Bus Mode:** Address bus transfers addresses from the microcontroller to the T-SMINT®I. For indirect address mode only A0 is valid. **Multiplexed Bus Mode** Not used in multiplexed bus mode. In this case A0-A6 should directly be connected to VDD.
	11	$\overline{RD}$	I	**Read** Indicates a read access to the registers (Intel bus mode).
		$\overline{DS}$	I	**Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).

Table 2 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	10	$\overline{WR}$	I	**Write** Indicates a write access to the registers (Intel bus mode).
		R/$\overline{W}$	I	**Read/Write** A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).
	9	ALE	I	**Address Latch Enable** An address on the external address/data bus (multiplexed bus type only) is latched with the falling edge of ALE. ALE also selects the microcontroller interface type (multiplexed or non multiplexed).
	5	$\overline{RST}$	I	**Reset:** Low active reset input. Schmitt-Trigger input with hysteresis of typical 360mV. Tie to '1' if not used.
	6	$\overline{RSTO}$	OD	**Reset Output:** Low active reset output.
	15	$\overline{INT}$	OD	**Interrupt Request:** $\overline{INT}$ becomes active if the T-SMINT®I requests an interrupt.
	18	MCLK	O	**Microcontroller Clock:** Clock output for the microcontroller
	20	$\overline{EAW}$	I	**External Awake**: A low level on $\overline{EAW}$ during power down activates the clock generation of the T-SMINT®I, i.e. the IOM®-2 interface provides FSC, DCL and BCL for read and write access.[1)]
	43	SX1	O	**S-Bus Transmitter Output (**positive**)**
	44	SX2	O	**S-Bus Transmitter Output (**negative**)**
	47	SR1	I	**S-Bus Receiver Input**

Table 2 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	48	SR2	I	**S-Bus Receiver Input**
	60	XIN	I	**Crystal 1:** Connected to a 15.36 MHz crystal
	59	XOUT	O	**Crystal 2:** Connected to a 15.36 MHz crystal
	64	AOUT	O	**Differential U-interface Output**
	61	BOUT	O	**Differential U-interface Output**
	3	AIN	I	**Differential U-interface Input**
	4	BIN	I	**Differential U-interface Input**
	49	$\overline{\text{VDDDET}}$	I	**VDD Detection:** This pin selects if the V_{DD} detection is active ('0') and reset pulses are generated on pin $\overline{\text{RSTO}}$ or whether it is deactivated ('1') and an external reset has to be applied on pin $\overline{\text{RST}}$.
	17	$\overline{\text{ACT}}$	O	**Activation LED.** Indicates the activation status of U- and S-transceiver. Can directly drive a LED (4mA).
	42	TP1	I	**Test Pin 1.** Used for factory device test. Tie to 'V_{SS}'
	50	TP2	I	**Test Pin 2.** Used for factory device test. Tie to 'V_{SS}'
	16, 19, 41, 55			Tie to '1'
	56, 57, 58	res		**Reserved** These pins are reserved for future use. Do not connect.

1) This function of pin $\overline{\text{EAW}}$ is different to that defined in Ref. [13]

I: Input

O: Output (Push-Pull)

OD: Output (Open Drain)

1.6.1 Specific Pins and Test Modes

LED Pin $\overline{\text{ACT}}$

A LED can be connected to pin **$\overline{\text{ACT}}$** to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U- and S-transceiver according to **Table 3**. or it is programmable via two bits (LED1 and LED2 in register MODE2).

Table 3 ACT States

Pin $\overline{\text{ACT}}$	LED	U_Deactivated	U_Activated	S_Activated
V_{DD}	OFF	1	x	x
2Hz (1 : 1)*	fast flashing	0	0	x
1Hz (3 : 1)*	slow flashing	0	1	0
GND	ON	0	1	1

Note: * denotes the duty cycle 'high' : 'low'.

with:

U_Deactivated: 'Deactivated State' as defined in **Chapter 2.4.7.6**.

U_Activated: 'SBC Synchronizing', 'Wait for Info U4H', and 'Transparent' as defined in **Chapter 2.4.7.6**.

S-Activated: 'Activated State' as defined in **Chapter 2.5.5.2**.

Note: Optionally, pin $\overline{\text{ACT}}$ can drive a second LED with inverse polarity (connect this additional LED to 3.3V only).

Test Modes

The test patterns on the S-interface ('2 kHz Single Pulses', '96 kHz Continuous Pulses') and on the U-interface ('Data Through', 'Send Single Pulses',) are invoked via C/I codes (TM1, TM2, DT, SSP). Setting SRES.RES_U to '1' forces the U-transceiver into test mode 'Quiet Mode' (QM), i.e. the U-transceiver is hardware reset.

1.7 System Integration

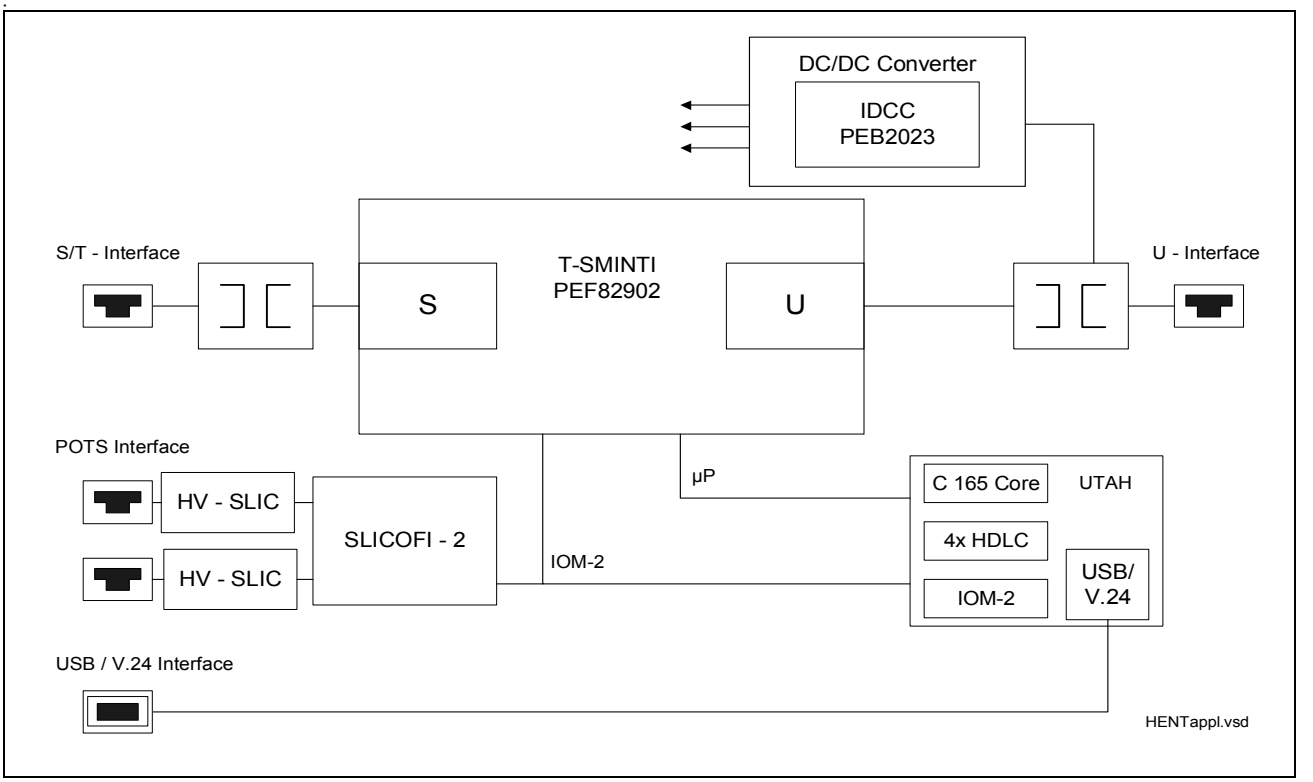


Figure 3 Application Example T-SMINT®I: High Feature Intelligent NT

The U-transceiver, the S-transceiver and the IOM®-2 channels can be controlled and monitored via:

a) the parallel or serial microprocessor interface
- Access of on-chip registers via µP interface Address/Data format
- Activation/Deactivation control of U- and S-transceiver via µP interface and C/I handler
- T-SMINT®I is Monitor channel master
- TIC bus is transparent on IOM®–2 interface and is used for D-channel arbitration between S-transceiver and off-chip HDLC controllers.