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Q-SMINT[®]
2B1Q Second Gen. Modular ISDN NT
(Intelligent)
PEF 82912/82913 Version 1.3

Wired
Communications



Never stop thinking.

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Q-SMINT[®]I

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Previous Version: Preliminary Data Sheet 10.00

Page	Subjects (major changes since last revision)
All	Editorial changes, addition of notes for clarification etc.
Table 1, Chapter 1.3	Introduced new version 82913 with extended performance of the U-interface
Chapter 2.1.1.1	SCI: header description: added to sequences 43 _H , 41 _H and 49 _H : 'Generally, it can be used for any register access to the address range 20 _H -7D _H .'
Chapter 2.3.2	IOM-2 handler: removed 'U-transceiver (U)' from listing of functional units with programmable time slot and data port.
Figure 12	Figure 'Data Access via CDAX0 and CDAX1 register pairs' corrected: input swap has influence on the input enable (EN_I0,1), too
Chapter 2.5.5.2	C/I commands: removed 'unconditional command' from description C/I-command 'DR'
Chapter 2.5.5.3	LT-S state machine: C/I=command AIL removed (no valid input to the LT-S state machine)
Chapter 4	Detailed register description: <ul style="list-style-type: none"> U-transceiver Mode Evaluation Timing: clarified description register ID: reset value of version 1.3 is 01_H (not 00_H) CIX1.CODX1: bits 5-0 of C/I-channel 1 (not 7-2) IOM_CR:TIC_DIS: added for clarification: 'This means that the timeslots TIC, A/B, S/G and BAC are not available any more.'
Chapter 5.1	Refined references for ESD requirements: '...(CDM), EIA/JESD22-A114B (HBM) ---'
Chapter 5.2	Input/output leakage current set to 10µA (before: 1µA)
Table 38	U-transceiver characteristics: enhanced S/N+D for 82913 and threshold level for 82912 and 82913 distinguished
Chapter 5.1	Absolute Maximum Ratings: Maximum Voltage on VDD: 4.2V (before: 4.6V)
Chapter 5.6.2 Chapter 5.6.3	AC-Timing SCI/parallel µC interface: enhanced timing specifications
Chapter 5.6.3	Added restriction for control interval t _{RI}
Chapter 5.6.5	Parameters of the UVD/POR Circuit: defined reduced range of hysteresis: min. 30mV/max. 90mV relaxed upper limit of Detection Threshold to 2.92V (before: 2.9V) defined max. rising VDD for power-on
Chapter 7.2.5	Register summary U-transceiver 4B3T: Reset value of MASKU is FF _H (not 00 _H)
Chapter 7.3	External circuitry for T-SMINT updated

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1 Overview

The **PEF 82912 / 82913** (Q-SMINT[®]I) offers U-transceiver, S-transceiver and an IOM[®]-2 interface. A microcontroller interface provides access to both transceivers as well as the IOM[®]-2 interface.

However, as opposed to its bigger brother Q-SMINT[®]IX, the Q-SMINT[®]I does not have an HDLC controller. Main target applications of the Q-SMINT[®]I are intelligent NT applications where the HDLC controller(s) is (are) provided by the microcontroller or other additional components. An example for such a microcontroller is the Infineon UTAH chip which features four flexible HDLC controllers.

Table 1 summarizes the 2nd generation NT products.

Table 1 NT Products of the 2nd Generation

	PEF80912	PEF80913	PEF81912	PEF81913	PEF82912	PEF82913
	Q-SMINT [®] O		Q-SMINT [®] IX		Q-SMINT [®] I	
Package	P-MQFP-44		P-MQFP-64 P-TQFP-64		P-MQFP-64 P-TQFP-64	
Register access	no		U+S+HDLC+ IOM [®] -2		U+S+ IOM [®] -2	
Access via	n.a.		parallel (or SCI or IOM [®] -2)		parallel (or SCI or IOM [®] -2)	
MCLK, watchdog timer, SDS, BCL, D-channel arbitration, IOM [®] -2 access and manipulation etc. provided	no		yes		yes	
HDLC controller	no		yes		no	
NT1 mode available	yes (only)		no		no	
Extended U-Performance 20kft	no	yes	no	yes	no	yes

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2B1Q Second Gen. Modular ISDN NT (Intelligent) Q-SMINT®

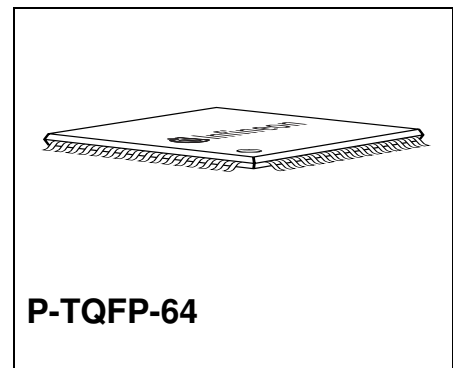
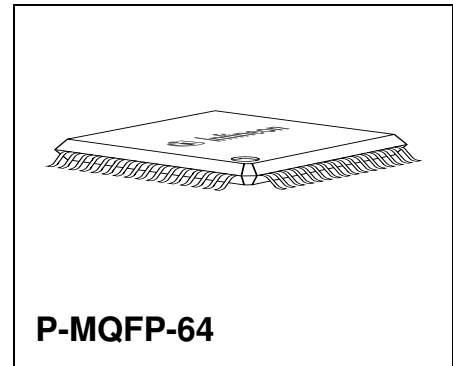
PEF 82912/82913

Version 1.3

1.2 Features PEF 82912

Features known from the PEB/PEF 8191

- U-transceiver and S-transceiver on one chip
- Perfectly suited for high-end intelligent NTs that require multiple HDLC controllers (which are provided externally)
- U-interface (2B1Q) conform to ETSI [1], ANSI [2] and CNET [3]:
 - Meets all transmission requirements on all ETSI, ANSI and CNET loops with margin
 - Conform to British Telecom’s RC7355E [4]
 - Compliant with ETSI 10 ms micro interruptions
 - MLT input and decode logic (ANSI [2])
- S/T-interface conform to ETSI [6], ANSI [7] and ITU [8]
 - Supports point-to-point and bus configurations
 - Meets and exceeds all transmission requirements
- Activation status LED supported
- BCL, SDS1, SDS2, programmable MCLK, watchdog timer,
- Access to IOM®-2 C/I and Monitor channels
- Power-down and reset states (e.g. S-transceiver) for individual circuits
- Automatic D-channel arbitration between S-bus and external HDLC controller
- Parallel or serial μ P-interface



Type	Package
PEF 82912/82913	P-MQFP-64
PEF 82912/82913	P-TQFP-64

New Features

- Reduced number of external components for external U-hybrid required
- Optional use of up to 2x20 Ω resistors on the line side of the transformer (e.g. PTCs)
- Pin Uref and the according external capacitor removed
- Improved ESD (2 kV instead of <850 V)
- Inputs accept 3.3 V and 5 V
- I/O (open drain) accepts pull-up to 3.3 V¹⁾
- LED signal is programmable but can also automatically indicate the activation status (mode select via 1 bit)
- Pin compatible with T-SMINT[®]I (2nd Generation)
- Priority setting (8/10) for off-chip HDLC controller
- Enhanced IOM[®]-2 timeslot access and manipulation (SCOUT)
- MCLK can be disabled (SCOUT)
- External Awake ($\overline{\text{EAW}}$)
- Optional: All registers can be read and written to via new Monitor channel concept
- Optional: Implementation of S-transceiver statemachine in software
- Indirect Addressing (SCOUT)
- Programmable strobes SDS1/2 are more flexible, e.g. active during several timeslots
- Power-on reset and Undervoltage Detection with no external components
- Lowest power consumption due to:
 - Low power CMOS technology (0.35 μ)
 - Newly optimized low-power libraries
 - High output swing on U- and S-line interface leads to minimized power consumption
 - Single 3.3 Volt power supply
- 200 mW (INTC-Q: 295 mW) power consumption with random data over ETSI Loop 2 (external loads on the S and U interface only and no additional external loads).
- 15 mW typical power consumption in power down (INTC-Q: 28 mW)

1.3 Features PEF 82913

The Q-SMINT[®]I PEF 82913 provides all features of the PEF 82912. Additionally, a significantly enhanced performance of the U-interface as compared to ETSI [1], ANSI [2] and CNET [3] requirements is guaranteed:

Transparent transmission on 20kft AWG26 with a BER < 10⁻⁷ (without noise).

¹⁾ Pull-ups to 5 V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

1.4 Not Supported are ...

- Integrated U-hybrid
- On-chip HDLC controller
- 'Self test request' and 'Self test passed' of U-transceiver
- TE-mode of the S-transceiver
- DECT-link capability
- SRA (capacitive receiver coupling is not suited for S-feeding).
- 'NT-Star' with star point on the IOM[®]-2 bus (already not supported in INTC-Q).
- No access to S2-5 channels. Access only to S1 and Q channel as in SCOUT. No selection between transparent and non-auto mode provided.
- The oscillator architecture was changed with respect to the INTC-Q to reduce power consumption. As a consequence, the Q-SMINT[®]I always needs a crystal and pin XIN can not be connected to an external clock as it was possible for IEC-Q and NTC-Q. This does not limit the use of the Q-SMINT[®]I in NTs since all NT designs use crystals anyway.

1.5 Pin Configuration

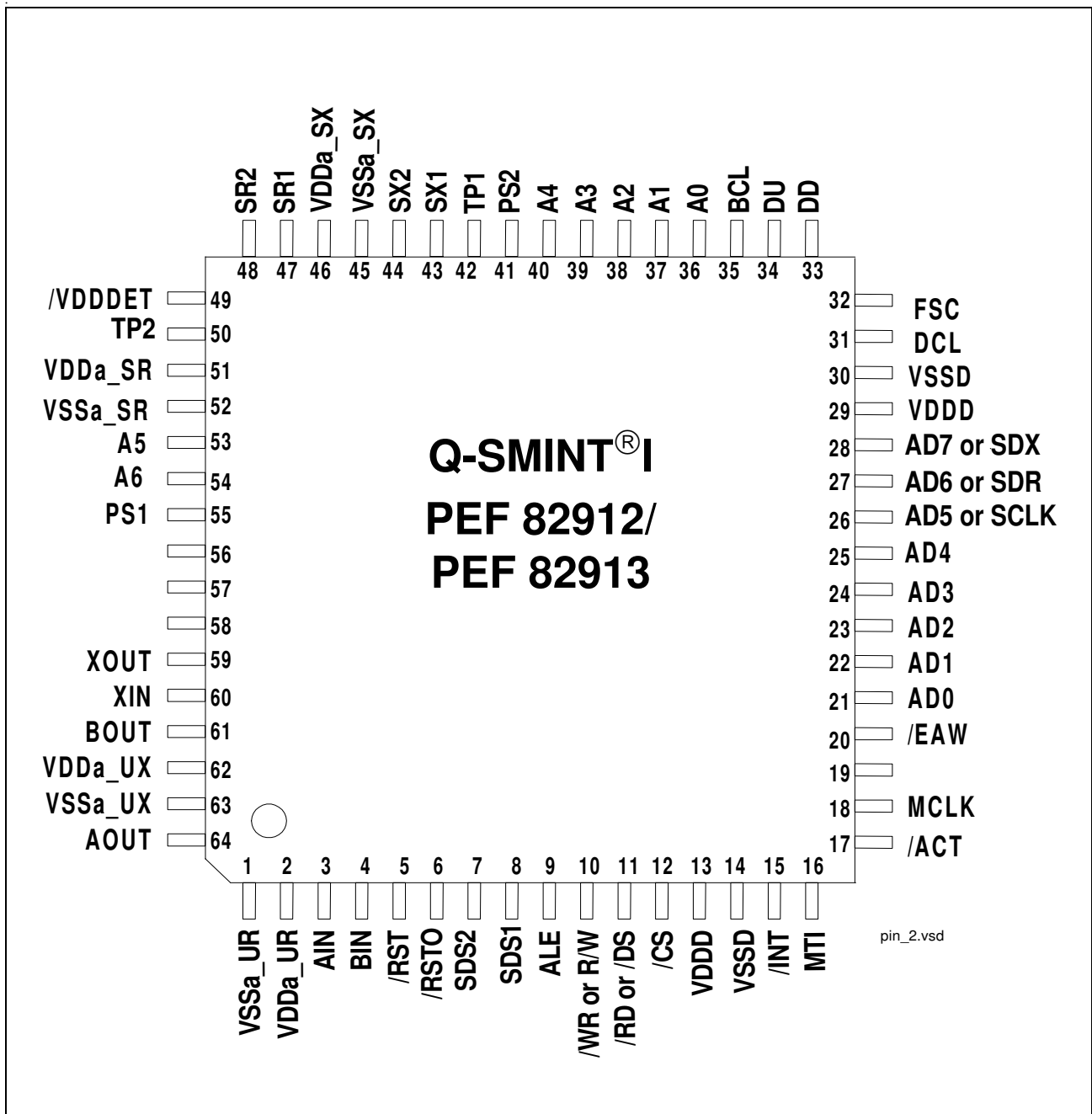


Figure 1 Pin Configuration

1.6 Block Diagram

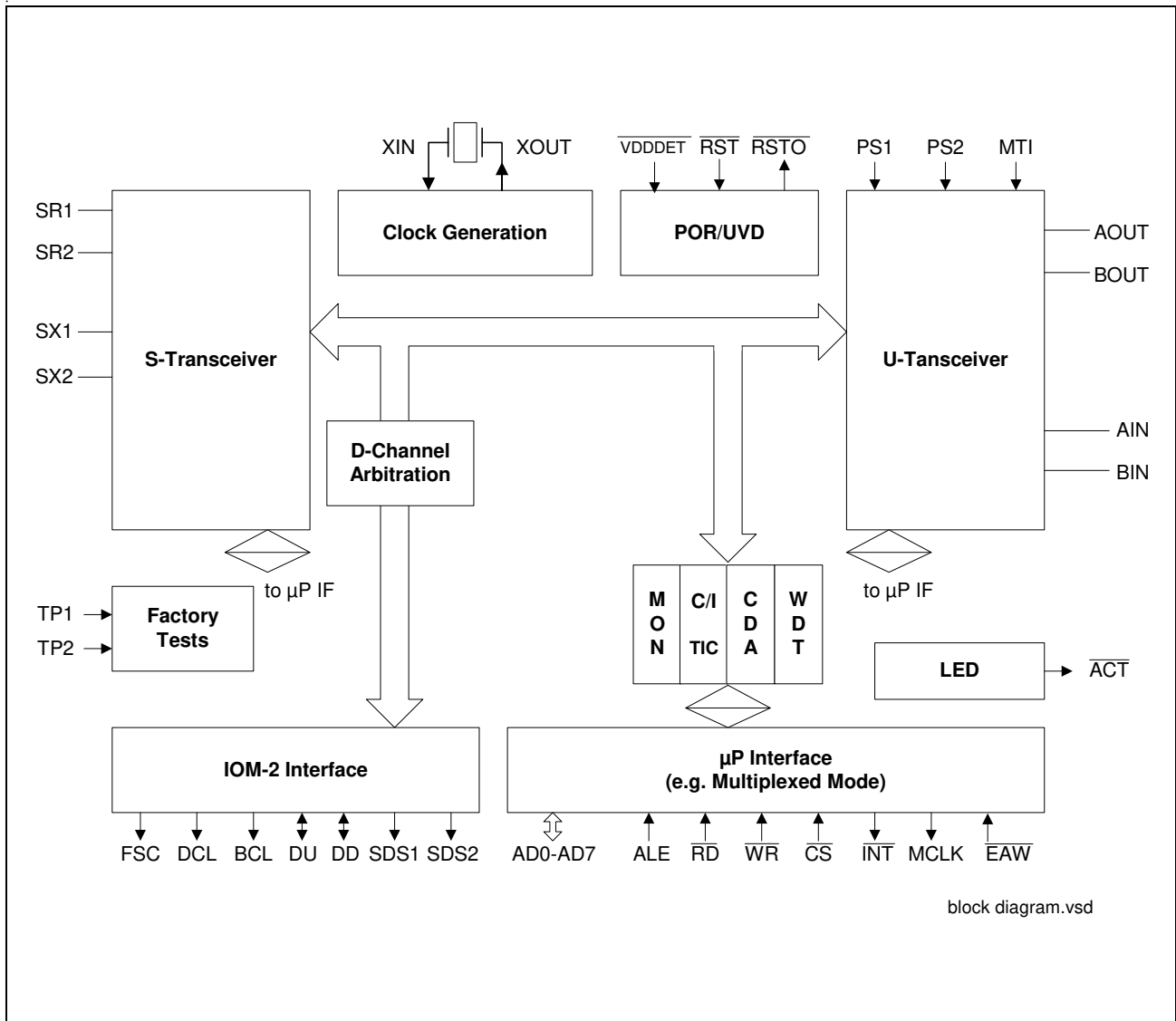


Figure 2 Block Diagram

1.7 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

	Pin	Symbol	Type	Function
	2	VDDa_UR	–	Supply voltage for U-Receiver (3.3 V ± 5 %)
	1	VSSa_UR	–	Analog ground (0 V) U-Receiver
	62	VDDa_UX	–	Supply voltage for U-Transmitter (3.3 V ± 5 %)
	63	VSSa_UX	–	Analog ground (0 V) U-Transmitter
	51	VDDa_SR	–	Supply voltage for S-Receiver (3.3 V ± 5 %)
	52	VSSa_SR	–	Analog ground (0 V) S-Receiver
	46	VDDa_SX	–	Supply voltage for S-Transmitter (3.3 V ± 5 %)
	45	VSSa_SX	–	Analog ground (0 V) S-Transmitter
	29	VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
	30	VSSD	–	Ground (0 V) digital circuits
	13	VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
	14	VSSD	–	Ground (0 V) digital circuits
	32	FSC	O	Frame Sync: 8-kHz frame synchronization signal
	31	DCL	O	Data Clock: IOM [®] -2 interface clock signal (double clock): 1.536 MHz
	35	BCL	O	Bit Clock: The bit clock is identical to the IOM [®] -2 data rate (768 kHz)
	33	DD	I/O OD	Data Downstream: Data on the IOM [®] -2 interface
	34	DU	I/O OD	Data Upstream: Data on the IOM [®] -2 interface

Overview

Table 2 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	8	SDS1	O	Serial Data Strobe1: Programmable strobe signal for time slot and/or D-channel indication on IOM [®] -2
	7	SDS2	O	Serial Data Strobe2: Programmable strobe signal for time slot and/or D-channel indication on IOM [®] -2
	12	$\overline{\text{CS}}$	I	Chip Select: A low level indicates a microcontroller access to the Q-SMINT [®] 1
	26	SCLK	I	Serial Clock: Clock signal of the SCI interface if a serial interface is selected
	26	AD5	I/O	Multiplexed Bus Mode: Address/data bus Address/data line AD5 if the parallel interface is selected Non-Multiplexed Bus Mode: Data bus Data line D5 if the parallel interface is selected
	27	SDR	I	Serial Data Receive: Receive data line of the SCI interface if a serial interface is selected
	27	AD6	I/O	Multiplexed Bus Mode: Address/data bus Address/data line AD6 if the parallel interface is selected Non-Multiplexed Bus Mode: Data bus Data line D6 if the parallel interface is selected

Overview

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Type	Function
28	SDX	OD,O	Serial Data Transmit: Transmit data line of the SCI interface if a serial interface is selected
28	AD7	I/O	Multiplexed Bus Mode: Address/data bus Address/data line AD7 if the parallel interface is selected Non-Multiplexed Bus Mode: Data bus Data line D7 if the parallel interface is selected
21 22 23 24 25	AD0 AD1 AD2 AD3 AD4	I/O I/O I/O I/O I/O	Multiplexed Bus Mode: Address/data bus Transfers addresses from the microcontroller to the Q-SMINT [®] I and data between the microcontroller and the Q-SMINT [®] I. Non-Multiplexed Bus Mode: Data bus. Transfers data between the microcontroller and the Q-SMINT [®] I (data lines D0-D4).
36 37 38 39 40 53 54	A0 A1 A2 A3 A4 A5 A6	I I I I I I I	Non-Multiplexed Bus Mode: Address bus transfers addresses from the microcontroller to the Q-SMINT [®] I. For indirect address mode only A0 is valid. Multiplexed Bus Mode Not used in multiplexed bus mode. In this case A0-A6 should directly be connected to VDD.
11	\overline{RD} \overline{DS}	I I	Read Indicates a read access to the registers (Intel bus mode). Data Strobe The rising edge marks the end of a valid read or write operation (Motorola bus mode).

Overview

Table 2 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	10	\overline{WR} R/\overline{W}	I I	Write Indicates a write access to the registers (Intel bus mode). Read/Write A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).
	9	ALE	I	Address Latch Enable An address on the external address/data bus (multiplexed bus type only) is latched with the falling edge of ALE. ALE also selects the microcontroller interface type (multiplexed or non multiplexed).
	5	\overline{RST}	I	Reset: Low active reset input. Schmitt-Trigger input with hysteresis of typical 360 mV. Tie to '1' if not used.
	6	\overline{RSTO}	OD	Reset Output: Low active reset output.
	15	\overline{INT}	OD	Interrupt Request: \overline{INT} becomes active if the Q-SMINT [®] I requests an interrupt.
	18	MCLK	O	Microcontroller Clock: Clock output for the microcontroller
	19			Tie to '1'
	20	\overline{EAW}	I	External Awake: A low level on \overline{EAW} during power down activates the clock generation of the Q-SMINT [®] I, i.e. the IOM [®] -2 interface provides FSC, DCL and BCL for read and write access. ¹⁾
	43	SX1	O	S-Bus Transmitter Output (positive)
	44	SX2	O	S-Bus Transmitter Output (negative)
	47	SR1	I	S-Bus Receiver Input