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MICROCHIP

8-Pin SOIC/MSOP/TSSOP/DIP
Evaluation Board
User's Guide

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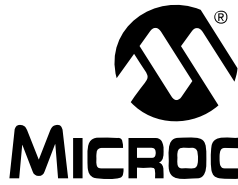
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8-PIN SOIC/MSOP/TSSOP/DIP EVALUATION BOARD USER'S GUIDE

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NOTES:

8-PIN SOIC/MSOP/TSSOP/DIP EVALUATION BOARD USER'S GUIDE

Preface

INTRODUCTION

This chapter contains general information that will be useful to know before using the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- The Microchip Web Site
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board. The manual layout is as follows:

- **Chapter 1. "Product Overview"** – Important information about the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board.
- **Chapter 2. "Installation and Operation"** – Includes instructions on how to get started with this evaluation board.
- **Appendix A. "Schematic and Layouts"** – Shows the schematic and layout diagrams for the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board.
- **Appendix B. "Bill of Materials (BOM)"** – Lists the parts used to build the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board.
- **Appendix C. "Microchip Analog and Interface Device Compatibility"** – Documents the Microchip Analog & Interface devices that are footprint compatable with this PCB.
- **Appendix D. "Rev. 1 PCB Errata"** – Describes the PCB Errata for the Revision 1 board.

8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board User's Guide

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...

RECOMMENDED READING

This blank PCB is generic and can be used with any Microchip device that is offered in one of the following 8-pin packages:

• SOIC

• DIP

• MSOP

• TSSOP

For more information regarding devices available in these 8-pin packages, please refer to the Microchip web site at www.microchip.com.

THE MICROCHIP WEB SITE

Microchip provides online support via our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

• **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software

• **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing

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- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

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Technical support is available through the web site at: http://support.microchip.com

In addition, there is a Development Systems Information Line which lists the latest versions of Microchip's development systems software products. This line also provides information on how customers can receive currently available upgrade kits.

The Development Systems Information Line numbers are:

1-800-755-2345 – United States and most of Canada

1-480-792-7302 – Other International Locations

DOCUMENT REVISION HISTORY

Revision A (March 2005)

- Initial Release of this Document.

NOTES:

Chapter 1. Product Overview

1.1 INTRODUCTION

This chapter provides an overview of the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board and covers the following topics:

- What is the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board?
- What the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board kit includes

1.2 WHAT IS THE 8-PIN SOIC/MSOP/TSSOP/DIP EVALUATION BOARD?

The 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board allows the system designer to quickly evaluate the operation of Microchip Technology's devices in any of the following 8-pin packages:

- SOIC
- DIP
- MSOP
- TSSOP

Some of the Microchip family of devices that can be evaluated in the PCB include:

- A/D Converters (ADCs) (ADCs)
- Battery Chargers
- Comparators
- D/A Converters (DACs) (DACs)
- DC-to-DC Converters
- Digital Potentiometers (Digi-Pots)
- Fan Controllers
- Integrated Devices
- Interface Devices
- Linear Regulators
- Operational Amplifiers (Op Amps)
- Power MOSFET Drivers
- Programmable Gain Amplifiers (PGAs)s (PGAs)
- Switching Regulators
- Temperature Sensors
- Voltage Supervisors and Voltage Detectors
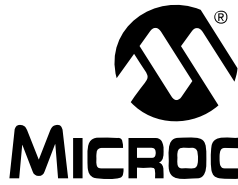- PICmicro® Microcontrollers

1.3 WHAT THE 8-PIN SOIC/MSOP/TSSOP/DIP EVALUATION BOARD KIT INCLUDES

This 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board Kit includes:

- Three 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board PCBs
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board User's Guide (DS51544) (Electronic version on CD)

NOTES:

Chapter 2. Installation and Operation

2.1   INTRODUCTION

This blank Printed Circuit Board (PCB) allows any 8-pin device in the following four package types to be installed:

1. SOIC-8
2. PDIP-8
3. MSOP-8
4. TSSOP-8

This board is generic so that any device may be installed. Refer to the device data sheet, however, for suitability of device evaluation.

As well as the device, other desired passive components (resistors and capacitors) and connection posts may be installed. This allows the board to evaluate a minimum configuration for the device. Also, this allows the device to be easily jumpered into an existing system.

2.2   FEATURES

The 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board has the following features:

- Connection terminals may be either through-hole or surface-mount
- Four 8-pin package footprints supported:
  - SOIC
  - DIP
  - MSOP
  - TSSOP
- Footprints for optional passive components for:
  - Power supply filtering
  - Device bypass capacitor
  - Output filtering
  - Output pull-up resistor
  - Output pull-down resistor
  - Output loading resistor
  - Output series resistor
  - Up to four additional passive components
- Silk-screen area to write specifics of implemented circuit (on back of PCB), such as TC1232 4.75V, (to indicate that the device is the TC1232 with the 4.75V trip point)
- PICmicro® MCU Baseline Flash Microcontroller Programmer (BFMP) Header
- Can be used for SOIC-8, MSOP-8, TSSOP-8 to DIP-8 converter

2.3   GETTING STARTED

The 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board is a blank PCB that allows the user to configure the circuit to the exact requirements. The passive components use the surface-mount 805 package layout.

This evaluation board supports the following Microchip device families:

- A/D Converters (ADCs) (ADCs)
- Battery Chargers
- Comparators
- D/A Converters (DACs) (DACs)
- DC-to-DC Converters
- Digital Potentiometers (Digi-Pots)
- Fan Controllers
- Integrated Devices
- Interface Devices
- Linear Regulators
- Operational Amplifiers (Op Amps)
- Power MOSFET Drivers
- Programmable Gain Amplifiers (PGAs)s (PGAs)
- Switching Regulators
- Temperature Sensors
- Voltage Supervisors and Voltage Detectors
- PICmicro Microcontrollers

Figure 2-1 shows the evaluation board circuit. Pin "n" of each device (U1, U2, U3 and U4) are tied together. These pins are then connected with pad "n" of the PCB (through a circuit). This circuit allows each pin to individually have any of the following: a pull-up resistor, a pull-down resistor, an in-line resistor and/or a loading/filtering capacitor. Device-filtering capacitors are available (C2 and C3), as well as a power supply filtering capacitor (C1).

There may be cases where some additonal passive components are desired for the evaluation circuit. The PCB has four 805 footprints that are not connected (labled P1, P2, P3 and P4) and can easily be jumpered into the desired circuit.
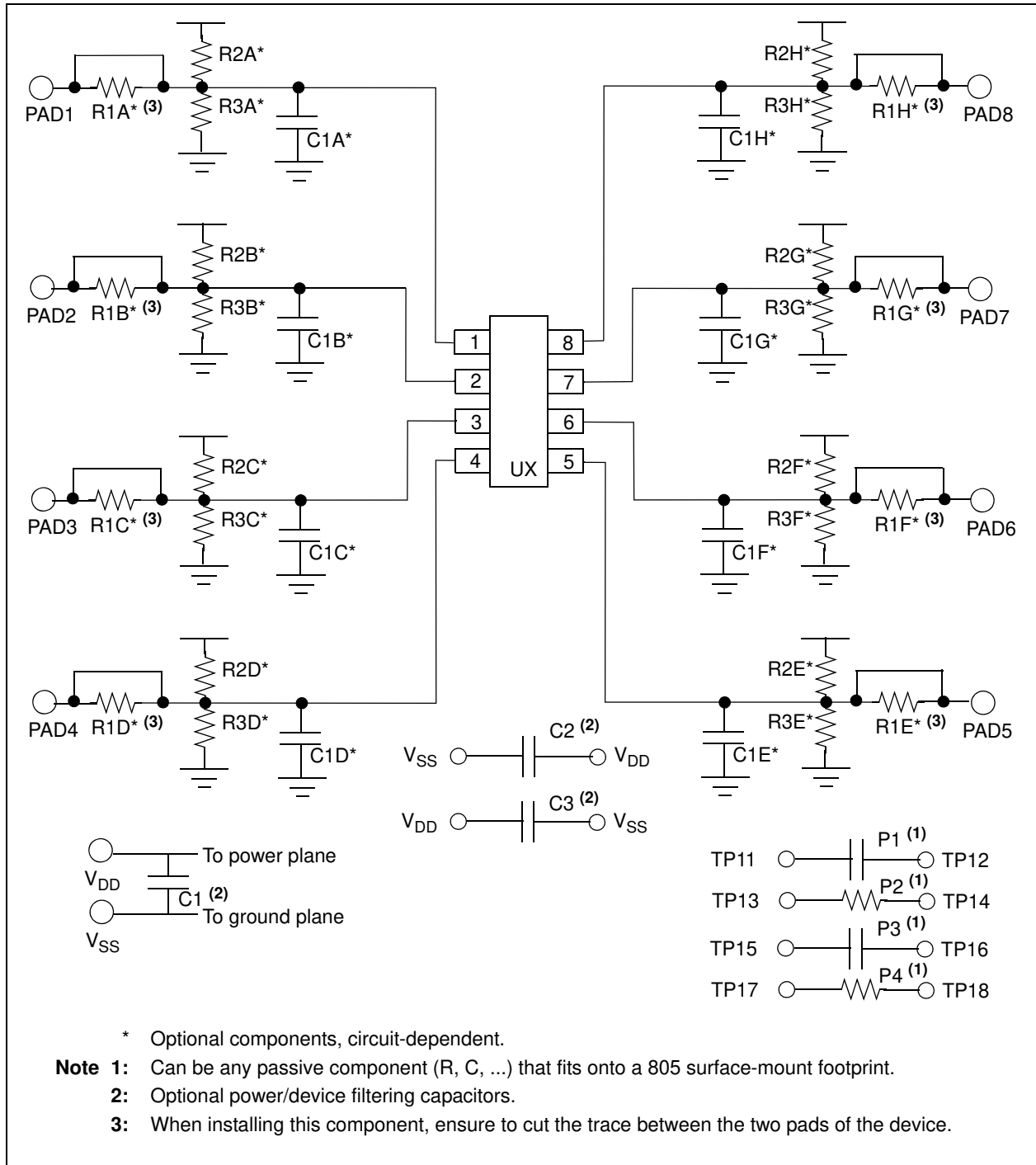
FIGURE 2-1: *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board Circuit.*

The figure contains the following labels:

Left side, top to bottom:
- PAD1, R1A* (3), R2A*, R3A*, C1A*
- PAD2, R1B* (3), R2B*, R3B*, C1B*
- PAD3, R1C* (3), R2C*, R3C*, C1C*
- PAD4, R1D* (3), R2D*, R3D*, C1D*

Right side, top to bottom:
- PAD8, R1H* (3), R2H*, R3H*, C1H*
- PAD7, R1G* (3), R2G*, R3G*, C1G*
- PAD6, R1F* (3), R2F*, R3F*, C1F*
- PAD5, R1E* (3), R2E*, R3E*, C1E*

Center device UX with pins 1, 2, 3, 4 on left and 8, 7, 6, 5 on right.

- V_{SS} —||— V_{DD} : C2 (2)
- V_{DD} —||— V_{SS} : C3 (2)

- V_{DD} To power plane
- V_{SS} To ground plane
- C1 (2)

- TP11 —||— TP12 : P1 (1)
- TP13 —\/\/\— TP14 : P2 (1)
- TP15 —||— TP16 : P3 (1)
- TP17 —\/\/\— TP18 : P4 (1)

* Optional components, circuit-dependent.

Note 1: Can be any passive component (R, C, ...) that fits onto a 805 surface-mount footprint.

2: Optional power/device filtering capacitors.

3: When installing this component, ensure to cut the trace between the two pads of the device.

2.3.1 The Hardware

Figure 2-2 shows the layout of the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board. This is a small four-layer board (1.5" x 2" (38.1 mm x 50.8 mm)). There are ten connection points/pads that can use either through-hole or surface-mount connector posts.

The pad labeled VDD is connected to the PCB power plane, while the pad labeled VSS is connected to the PCB ground plane. All the passive components that are connected to VDD or VSS are connected to either the power plane or ground plane.

The eight remaining PCB pads correspond to the device pins (i.e.; pad 1 connects to pin 1).

Each pad has four passive components associated with them: a pull-up resistor, a pull-down resistor, an in-line resistor and a filtering/load capacitor. The pull-up resistor is always R2X, the pull-down resistor is R3X, the in-line resistor is R1X and the filtering/load capacitor is C1X. The "X" is an alpha character that corresponds to a particular pad (A to H). As an example, Pad 5's pull-up resistor is R2E.

The green area of Figure 2-2 shows the silk-screen on the bottom layer of the PCB. This is where the details of the implemented circuit can be written.

Capacitor C1 is the power supply filtering capacitor.

Capacitors C2 and C3 are bypass capacitors that may be required to be installed, depending on the device selected and the system requirements (such as the noise present on the power supply). Table 2-1 describes the components.

A 6-pin header interface is available that supports the PICmicro MCU Baseline Flash Microcontroller Programmer (BFMP) interface. For additional information, refer to **Section 2.4.5 "Baseline Flash Microcontroller Programmer (BFMP) Interface (Header J1)"**.
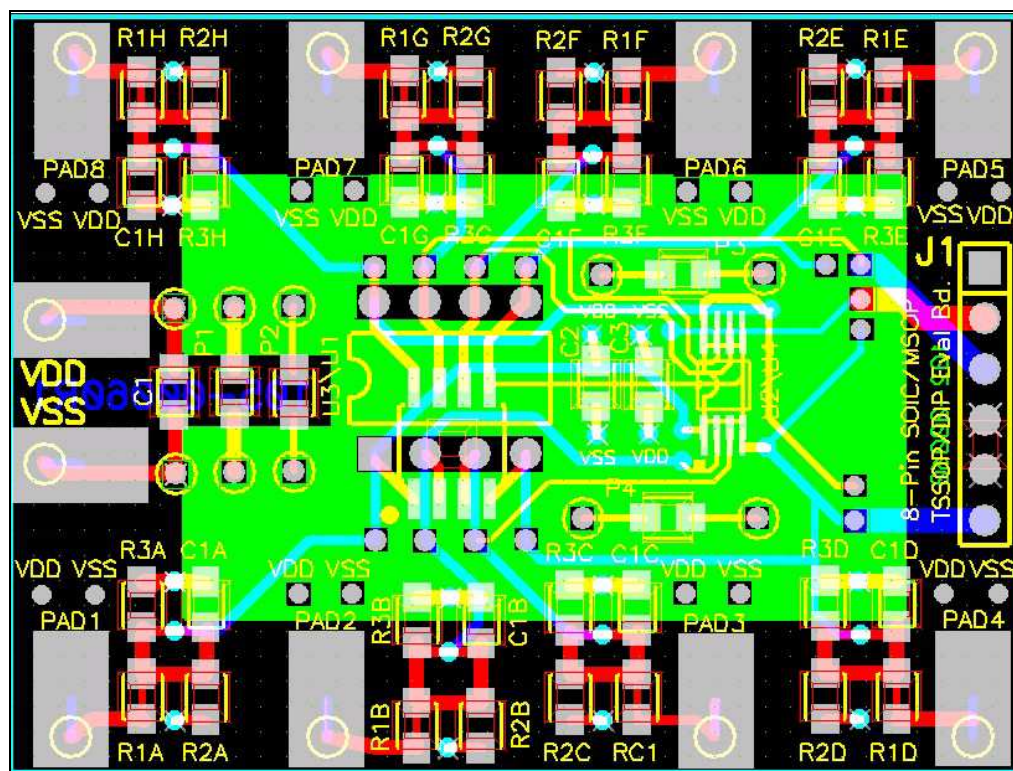

FIGURE 2-2:   *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board Layout.*

TABLE 2-1:   OPTIONAL PASSIVE COMPONENTS

Device	Comment
C1	Power supply bypass capacitor
C2, C3	Device Filtering capacitor
C1A, C1B C1C, C1D, C1E, C1F, C1G, C1H	Output filter capacitor
R1A, R1B, R1C, R1D, R1E, R1F, R1G, R1H	In-line resistance of device output
R2A, R2B, R2C, R2D, R2E, R2F, R2G, R2H	Pull-up resistor
R3A, R3B, R3C, R3D, R3E, R3F, R3G, R3H	Pull-down resistor
P1, P2, P3, P4	Optional Passive Components

2.4 8-PIN SOIC/MSOP/TSSOP/DIP EVALUATION BOARD DESCRIPTION

The 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board PCB is designed to be flexible in the type of device evaluation that can be implemented.

The following sections describe each element of this evaluation board in further detail. Refer to Figure 2-3.

2.4.1 Power and Ground

The 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board has a VDD Pad and a VSS pad. These pads can have connection posts installed that allows easy connection to the power (V_{DD}) and ground (V_{SS}) planes. The layout allows either through-hole or surface-mount connectors.

The power and ground planes are connected to the appropriate passive components on the PCB (such as power plane to R2X and ground plane to R3X and C1X).

2.4.2 PCB PADs

For each package pin (pins 1 to 8), there is a PCB pad (pads 1 to 8). The device will have some power pins (V_{DD}) and some ground pins (V_{SS}). To ease connections on the PCB, vias to the power and ground plane have been installed close to each PCB pad. This allows any pad to be connected to the power or ground plane, so when power is connected to the VDD and VSS pads, the power is connected to the appropriate device pin.
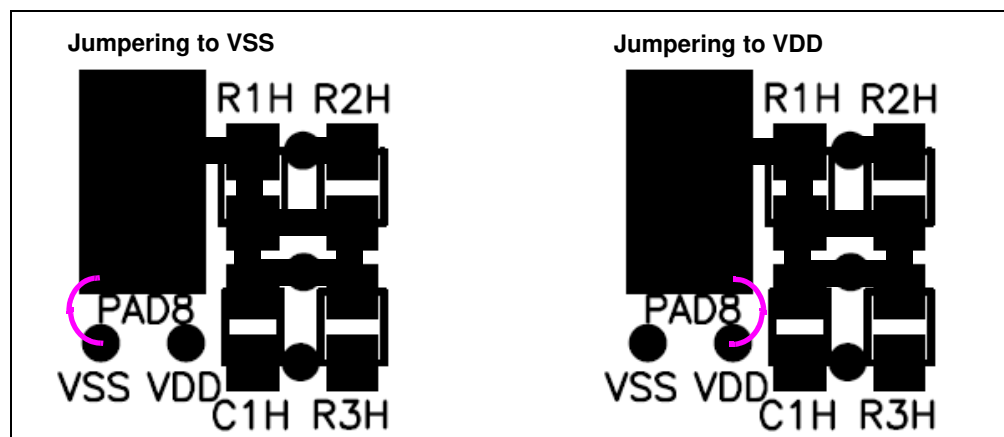

FIGURE 2-3:   *Jumpering the PCB pad to either VDD or VSS.*

Revision 1 of this PCB has an issue that these vias are not connected to the desired power and ground planes (they are open). For additional information, refer to **Appendix D. "Rev. 1 PCB Errata"**.

2.4.3 Passive Components (R1X, R2X, R3X, C1X, R1, R2, C1, C2, C3, P1, P2, P3 and P4)

The footprints for these components are present to allow maximum flexibility in the use of this PCB to evaluate a wide range of SOT-23-3 devices. The purpose of these components may vary depending on the device under evaluation and how it is to be used in the desired circuit. Refer to the device data sheet for the recommended components that should be used when evaluating that device.

- Component R1X allows an in-line resistor that can be installed between the device pin and the PCB pad. This may be required when interfacing this PCB to other circuits
- Component R2X allows a pull-up resistor to be installed for the device pin
- Component R3X allows a pull-down resistor to be installed for the device pin
- Component C1X allows a capacitive load/filter to be installed for the device pin
- Component C1 allows a power supply filtering capacitor to be installed
- Components C2 and C3 allows a device filtering capacitor to be installed
- Components P1, P2, P3, and P4 are not connected and give a footprint (805 surface-mount) for a passive component (resistor, capacitor, etc.) to be installed and jumpered into the PCB circuit. This allows for the evaluation of some simple device circuits to be implemented on this PCB

2.4.4 Installing Resistor R1X

Resistor R1X is shorted by default. Therefore, if resistor R1X is to be installed, the trace across the component must be cut before it is installed (see Figure 2-4).

While evaluating a device, it may be desireable to see the signals on both sides of this resistor. A test point is available so that both signals may be monitored. This test point is the avenue between components R3X and C1X (see Figure 2-4).
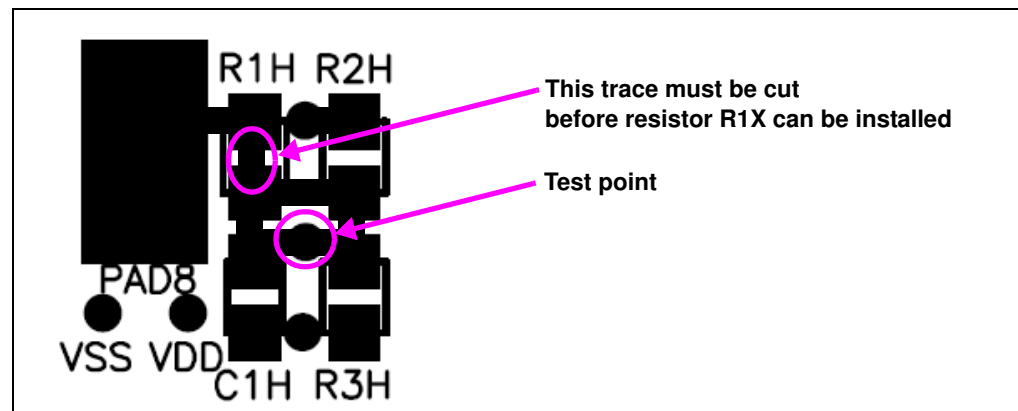

FIGURE 2-4: *Test point when resistor R1X is installed.*

2.4.5 Baseline Flash Microcontroller Programmer (BFMP) Interface (Header J1)

The BFMP interface allows a PICmicro MCU device to be programmed with programmers that support this interface, such as the BFMP programmer (part number PG164101).

The PCB supports two device pinouts. The default pinout already has the traces connected to the appropriate PICmicro MCU pins. The optional pinout requires three PCB traces to be cut and then three connections to be made (see Figure 2-5).

TABLE 2-2: BFMP HEADER SIGNALS AND PICMICRO MCU PINS

BFMP Header Signal	Pin Number		Comment
	Default Pinout	Optional Pinout [1]	
CLK	6	4	ICSP™ Clock
DT	7	5	ICSP Data
VPP	4	8	

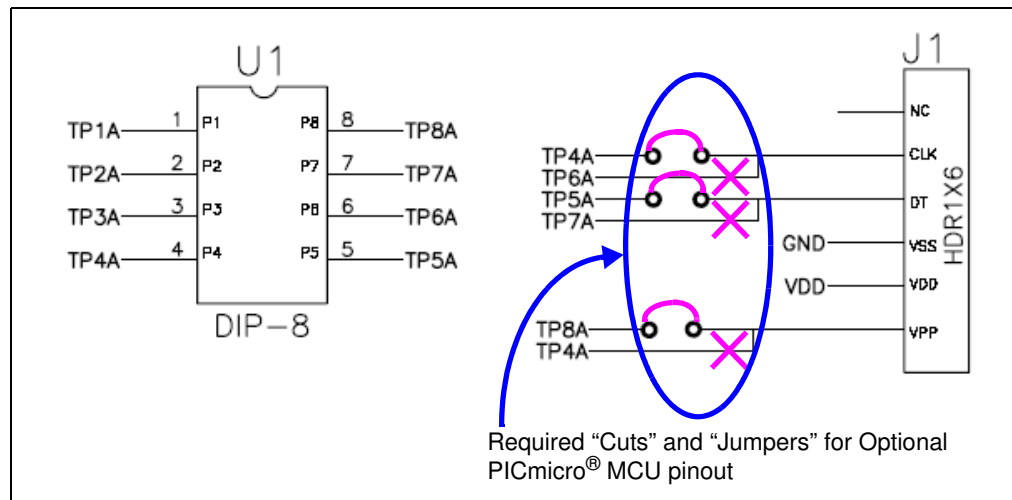**Note 1:** Requires PCB traces to be cut and then jumpered.

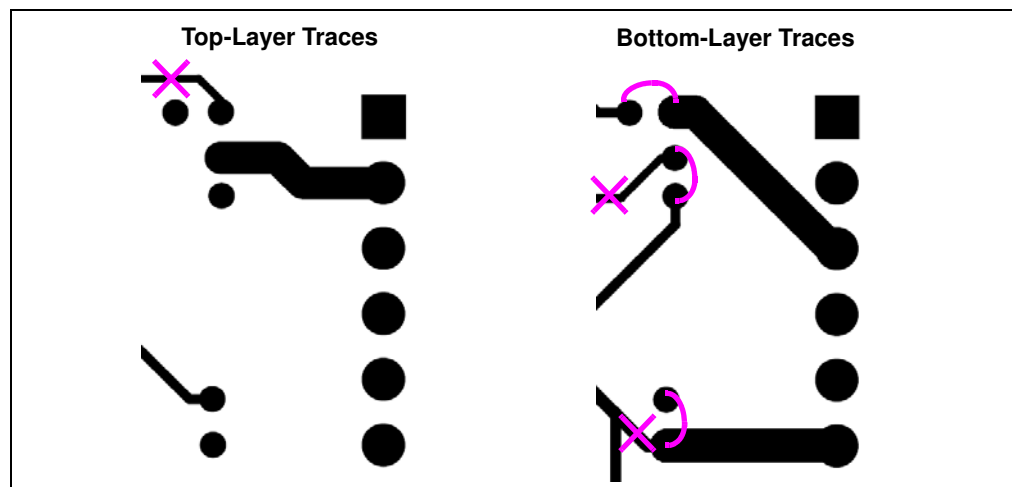

FIGURE 2-5: *BFMP Header and Connections*

FIGURE 2-6: *PCB Traces (Top and Bottom Layers).*

2.4.6 The PCB as a SOIC-8, MSOP-8, or TSSOP-8 to DIP-8 Socket Converter

There may be occasions when it is desireable to convert the footprint of the device to that of a DIP package. This allows the device to be installed into an exsisting DIP socket. Two 1x4 row pins need to be installed into the PCB's DIP footprint when the device is installed into the appropriate package footprint.

This allows the PCB to convert the SOIC-8, MSOP-8 or TSSOP-8 footprints to a 300-mil DIP-8 footprint.

2.4.7 Evaluating a Voltage Supervisor or Voltage Detector Device

2.4.7.1 VOLTAGE SUPERVISORS

The following voltage supervisor is supported by this evaluation board.

TABLE 2-3:   8-PIN VOLTAGE SUPERVISOR

Device	SOIC	DIP	MSOP	TSSOP	Comment
TC1232	Yes	Yes	—	—	

2.4.7.2 TESTING THE VOLTAGE SUPERVISORS TRIP POINT OPERATION

When evaluating a voltage supervisor/voltage detector device, a minimum set of test equipment should be available. Table 2-4 shows the recommended test equipment.

TABLE 2-4:   TEST EQUIPMENT

Hardware	Connect to:	Comment
Variable Power Supply	V_{DD}, V_{SS}	This allows the voltage to the SOT23 Evaluation Board to be varied so the device output can be monitored.
Arbitrary Waveform Generator	V_{DD}, V_{SS}	This is similar to a variable power supply, but allows programmability into the input signal that the device will be subjected to. This also allows a particular waveform to be repeated (such as a 60 Hz sine wave that varies from 1V to 5V).
Digital Multi-Meter (D.M.M.)	V_{OUT} [1]	Used to indicate the output state (low or high) of the voltage supervisor/voltage detector.
Oscilloscope	V_{OUT} [1]	Allows the device conditions and response to be evaluated due to the ability to capture this information. This is useful for faster signals and cases where small spikes need to be detected.
Test Light (LED)	V_{OUT} [1]	Used to visually indicate the output state (low or high) of the voltage supervisor/voltage detector. Ensure that the current requirements of this LED can be supplied by the device's output pin.

Note 1: The pad connection to connect to the V_{OUT} or $\overline{RST}$ pin will be dependent on the device and the footprint option used.

A typical system that would be used to evaluate the voltage supervisor/voltage detector device is shown in Figure 2-7. This also shows an example input and output waveform for a voltage supervisor/voltage detector device.
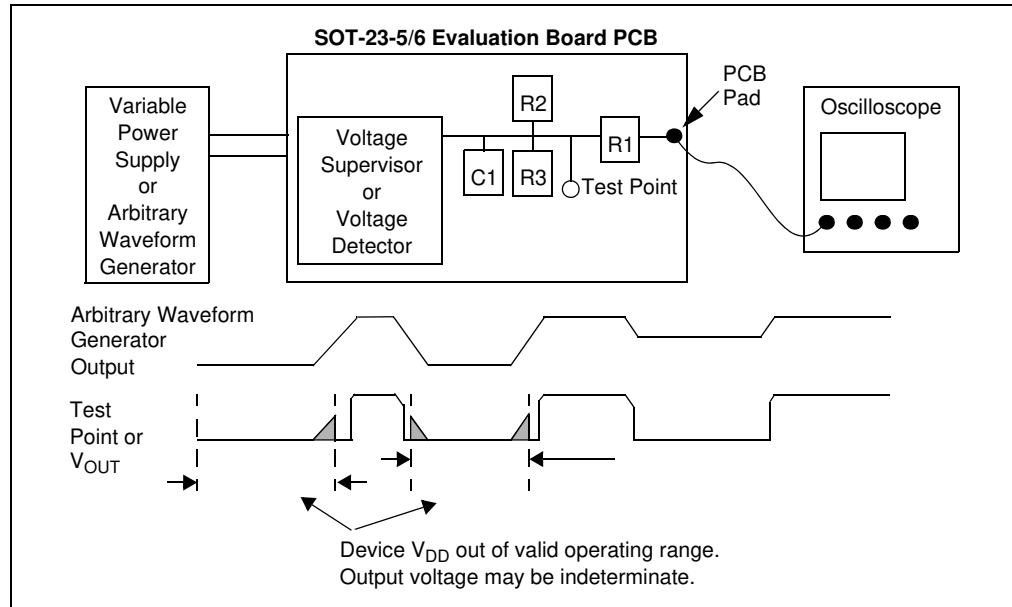

FIGURE 2-7: *Evaluation System.*

2.4.8 Example Op Amp Circuits

This section shows how the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board could be used to evaluate op amp circuits. The first circuit is for the MCP601 and is shown in Figure 2-8. Figure 2-9 shows which components on the PCB would be installed and how the "unconnected" passive components would be jumpered into the circuit.
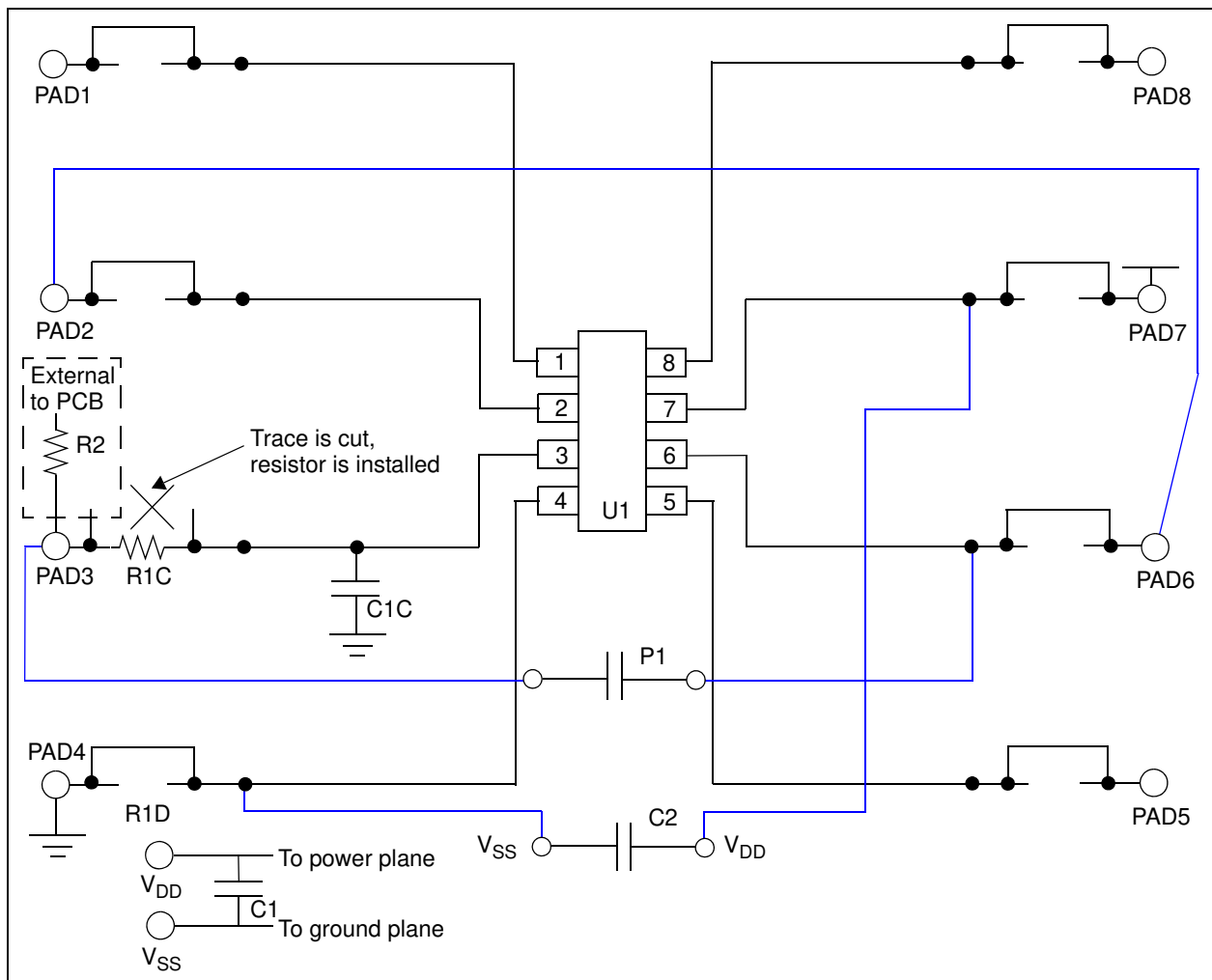
The second circuit is for the MCP6021 and is shown in Figure 2-10. Figure 2-11 shows which components on the PCB would be installed and how the "unconnected" passive components would be jumpered into the circuit.
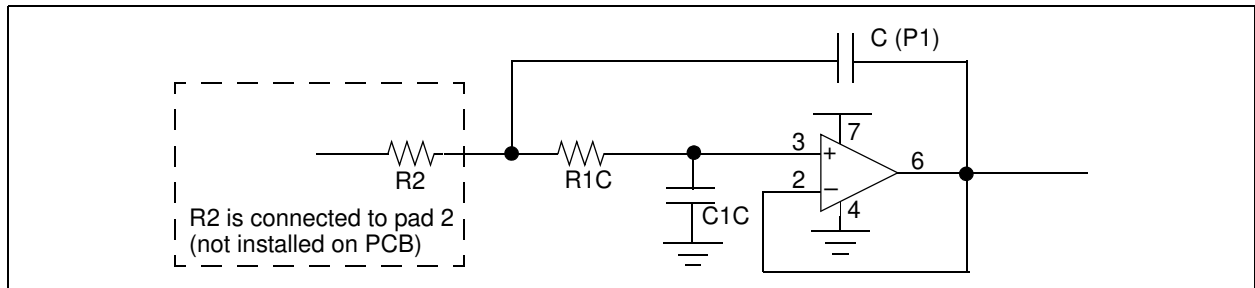
FIGURE 2-8: *Op Amp Circuit #1 (MCP601).*

FIGURE 2-9: *PCB Connections for Op Amp Circuit #1 (MCP601).*
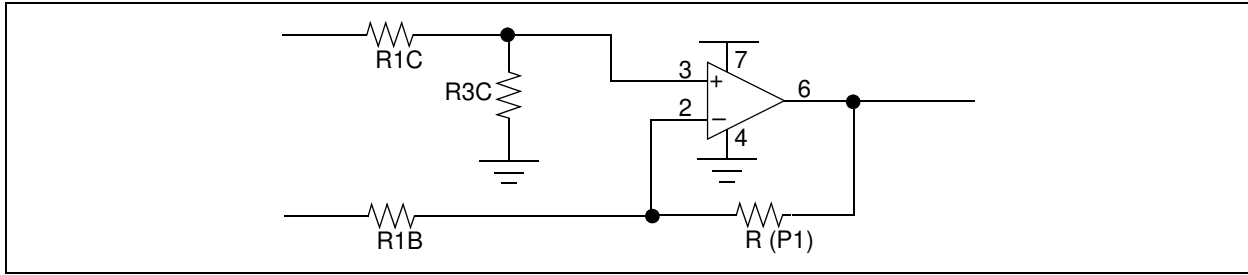
FIGURE 2-10: *Op Amp Circuit #2 (MCP6021).*
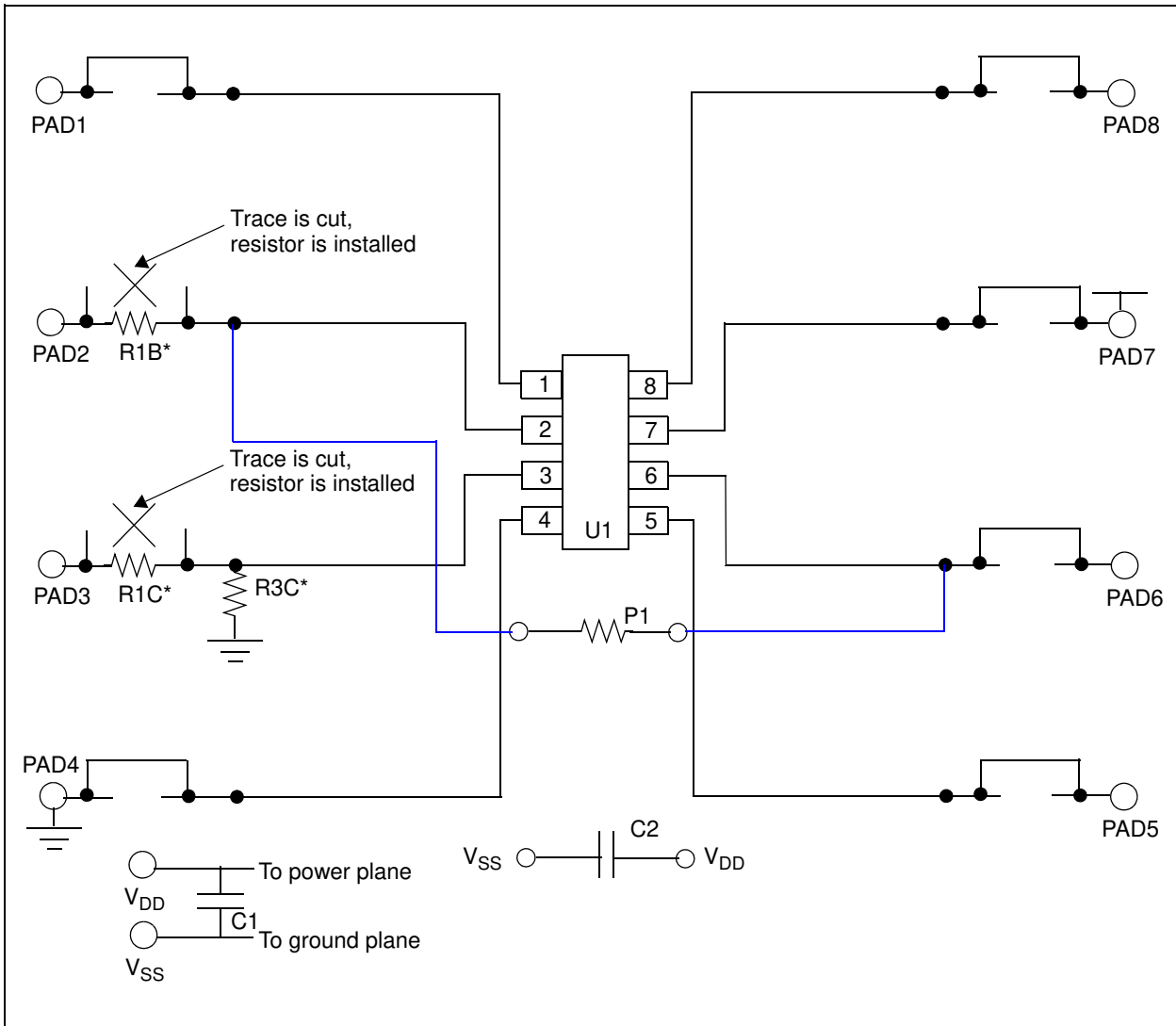
FIGURE 2-11: *PCB Op Amp Circuit #2 (MCP6021).*

Appendix A. Schematic and Layouts

A.1   INTRODUCTION

This appendix contains the schematics and layouts for the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board. Diagrams included in this appendix:

- Board Schematic - Digital Circuitry
- Board – Top Layer + Bottom Layer + Silk-Screen
- Board – Top Layer + Silk-Screen
- Board – Bottom Layer
- Board – Power Plane
- Board – Ground Plane
- Board – Component Layer

A.2   SCHEMATICS AND PCB LAYOUT

Figure A-3 shows the schematic of the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board.

Figure A-2 shows the layout for the top layer of the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board. The layer order is shown in Figure A-1.
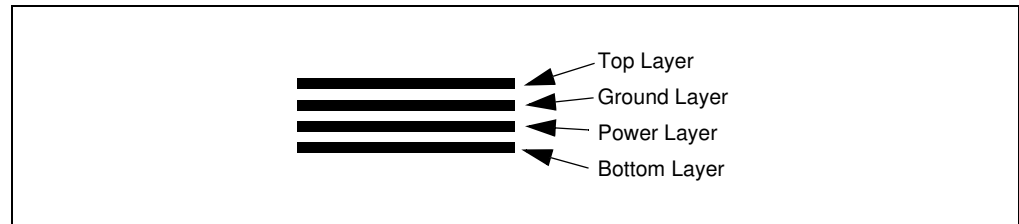

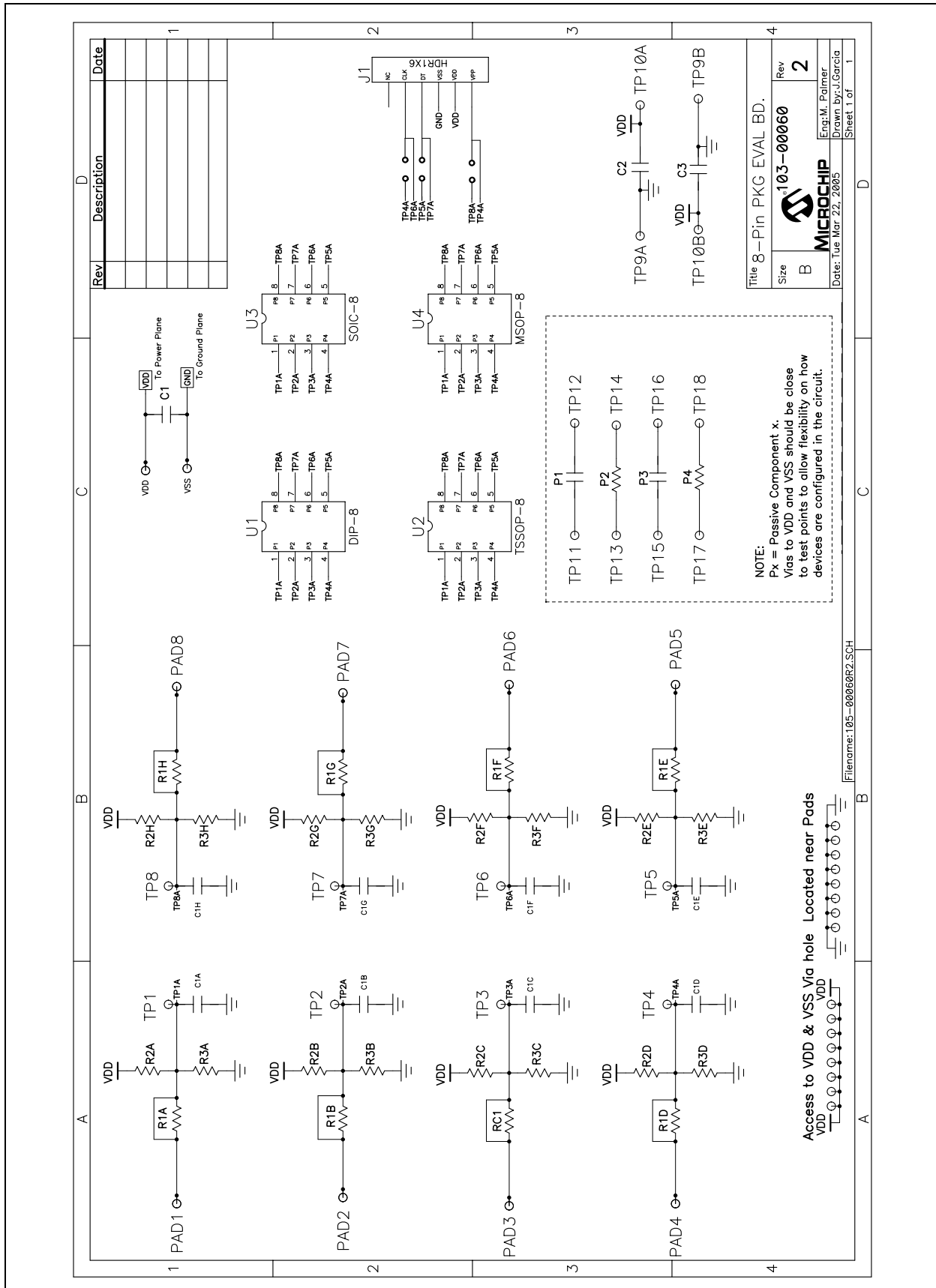**FIGURE A-1:**   *Layer Order.*

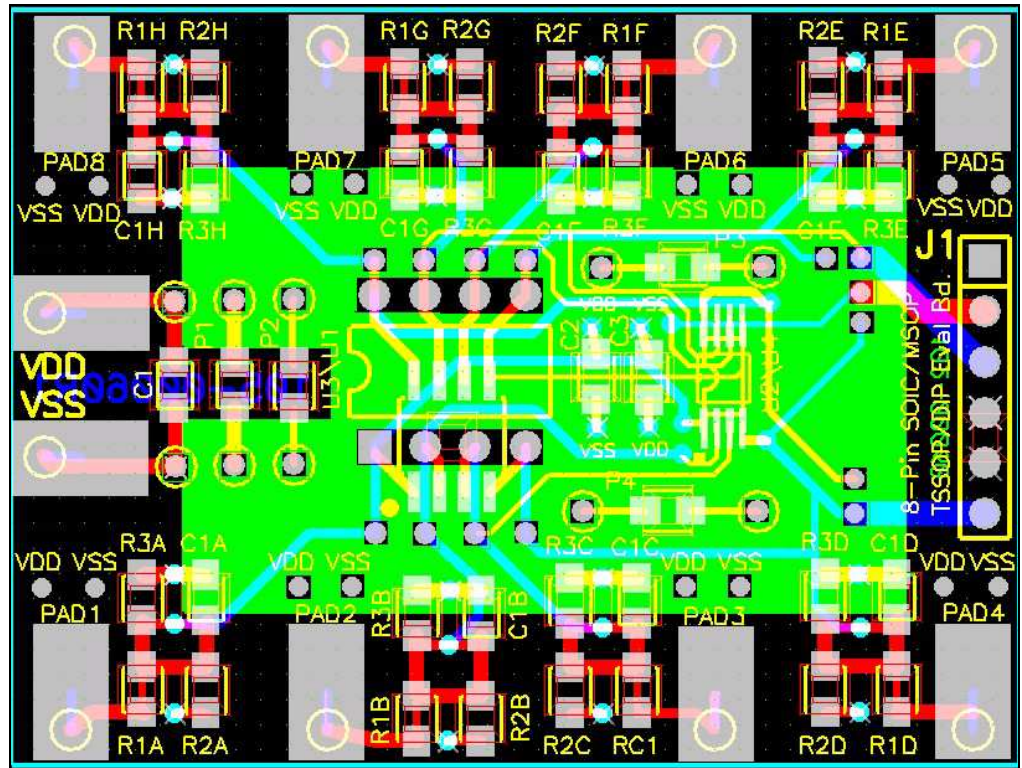**FIGURE A-2:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board Schematic.*

FIGURE A-3: *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board Layout – Top Layer + Bottom Layer + Silk-Screen.*