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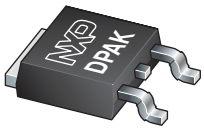


PHD101NQ03LT

N-channel TrenchMOS logic level FET

Rev. 5 — 31 October 2011 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters

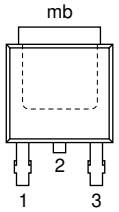
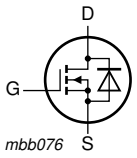
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	30	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	166	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	4.5	5.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 5 V; I_D = 50 A; V_{DS} = 15 V; T_j = 25 °C; see Figure 11	-	8	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT428 (DPAK)

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

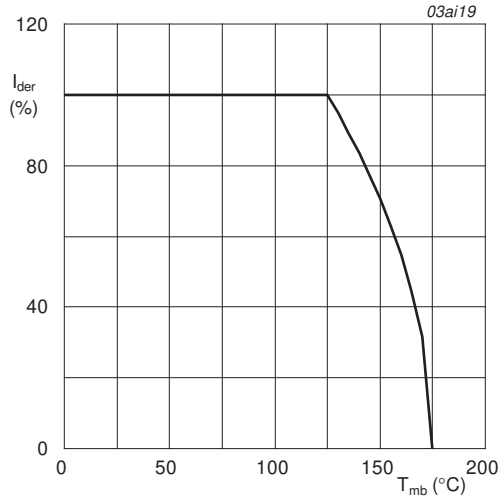
Type number	Package		
	Name	Description	Version
PHD101NQ03LT	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

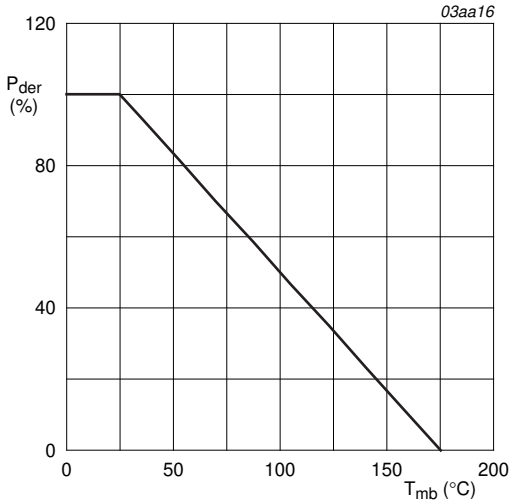
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	75	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3	-	75	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; see Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	166	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; δ = 25 %; $t_p \leq 50$ µs	-25	25	V
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C	-	240	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 43$ A; $V_{sup} \leq 15$ V; unclamped; $t_p = 0.19$ ms; $R_{GS} = 50$ Ω	-	185	mJ



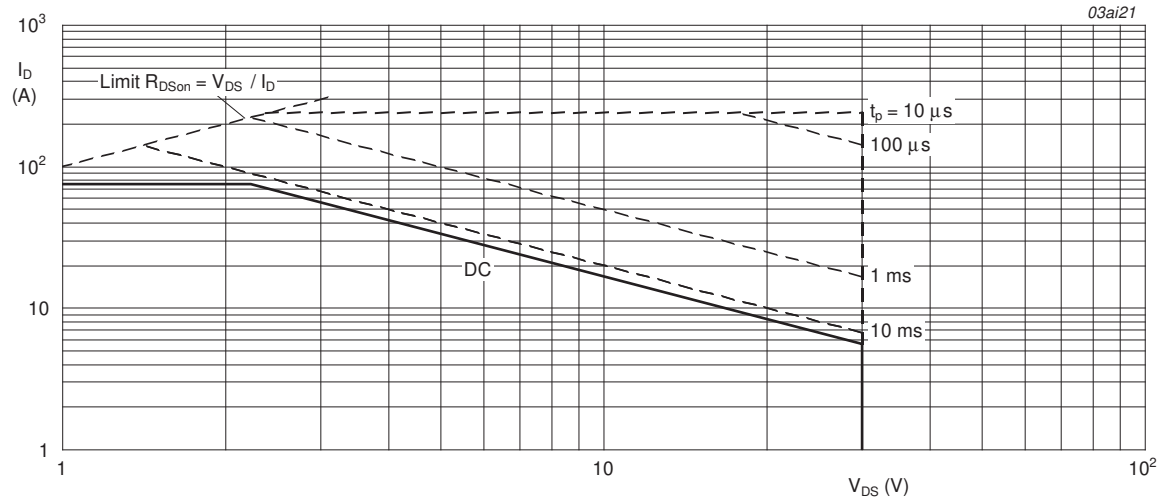
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25°C; I_{DM} \text{is single pulse}; V_{GS} = 10V$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4		-	-	0.9	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	-	75	-	K/W
		SOT404 minimum footprint	[1]	-	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

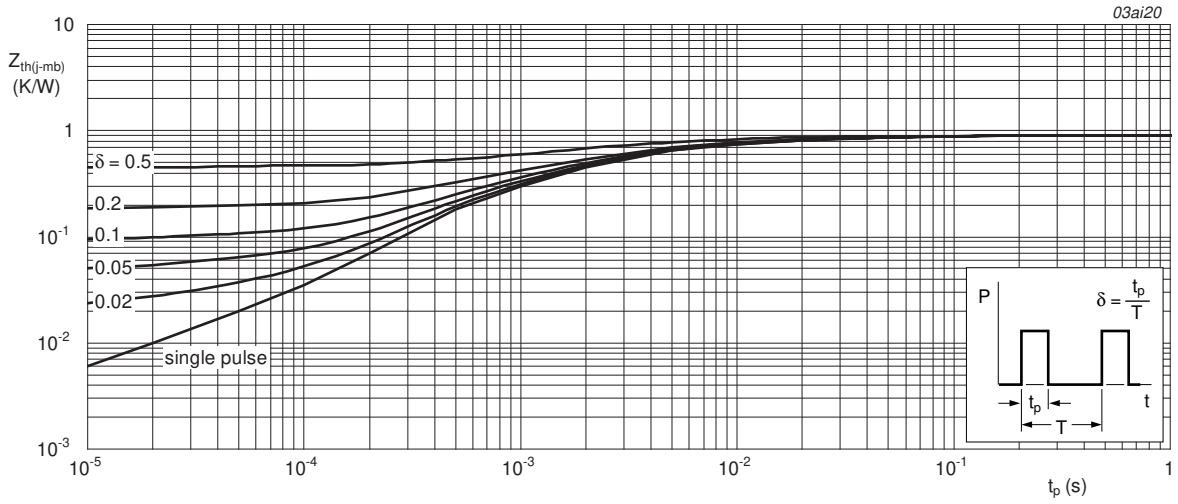
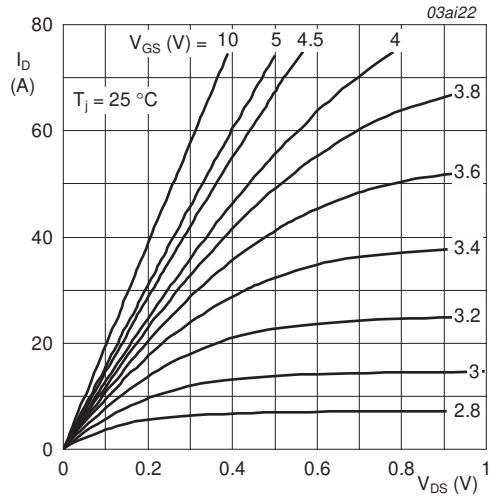


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

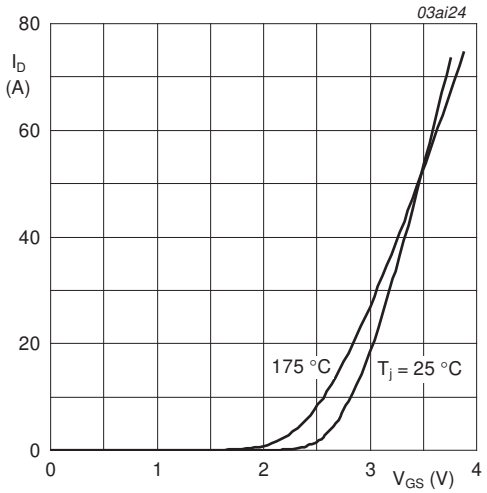
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 7; see Figure 8	0.6	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 7; see Figure 8	-	-	2.9	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 7; see Figure 8	1	1.9	2.5	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	4.5	5.5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 9; see Figure 10	-	10.5	13.5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 9; see Figure 10	-	5.8	7.5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 50 A; V_{DS} = 15 V; V_{GS} = 5 V; T_j = 25 °C; see Figure 11	-	23	-	nC
Q_{GS}	gate-source charge		-	10.5	-	nC
Q_{GD}	gate-drain charge		-	8	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 12	-	2180	-	pF
C_{oss}	output capacitance		-	600	-	pF
C_{rss}	reverse transfer capacitance		-	225	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5.6 Ω; T_j = 25 °C; I_D = 25 A	-	23	-	ns
t_r	rise time		-	90	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
t_f	fall time		-	33	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 13	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C	-	37	-	ns
Q_r	recovered charge		-	33	-	nC



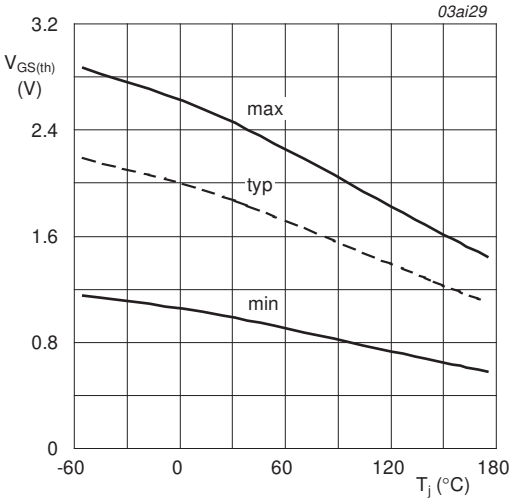
$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



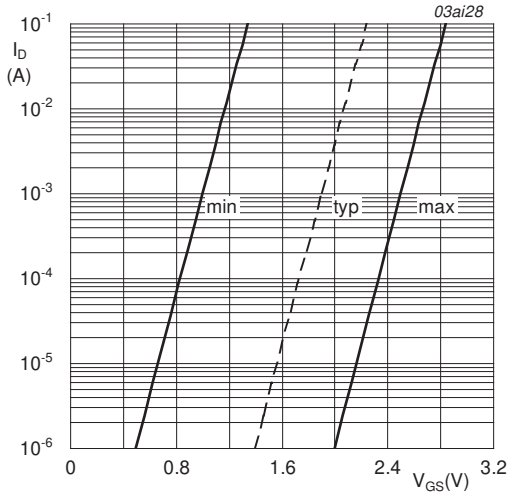
$T_j = 25°C \text{ and } 175°C; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



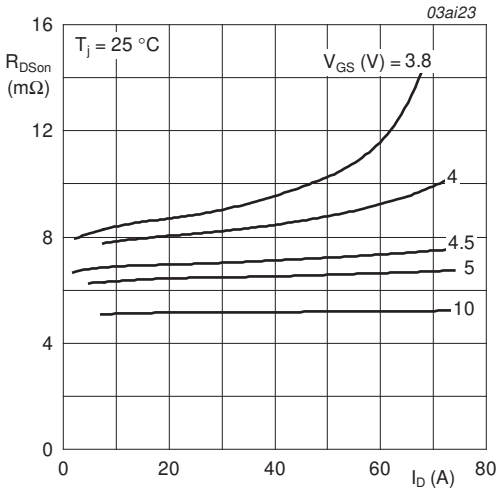
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



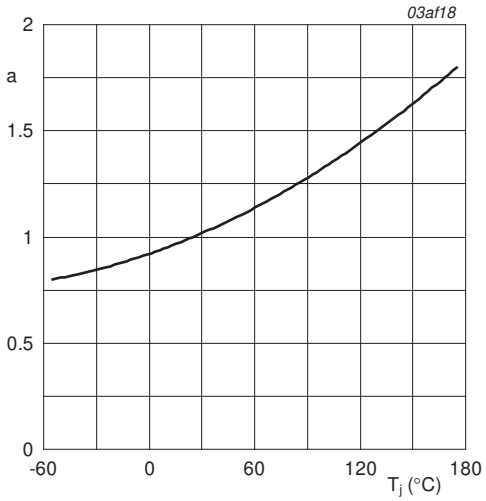
$T_j = 25°C; V_{DS} = 5V$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



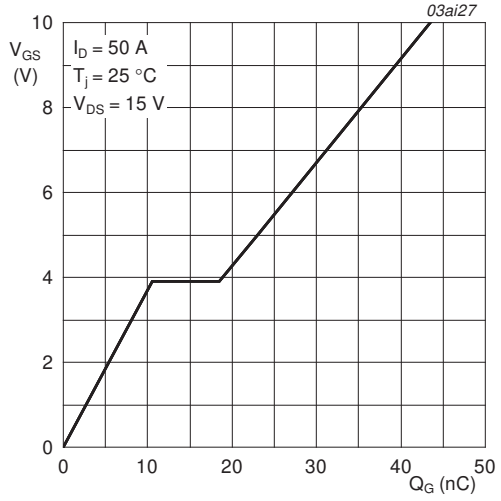
$T_j = 25°C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



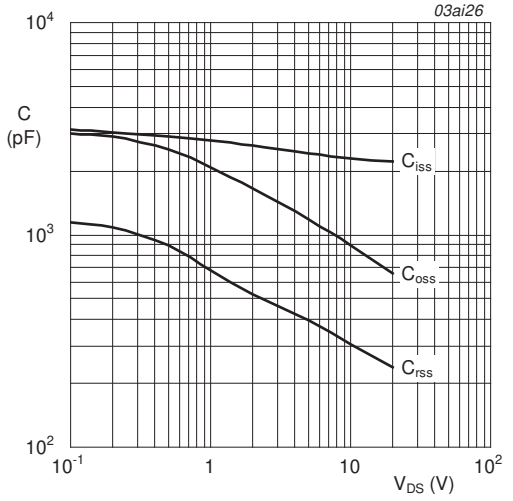
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



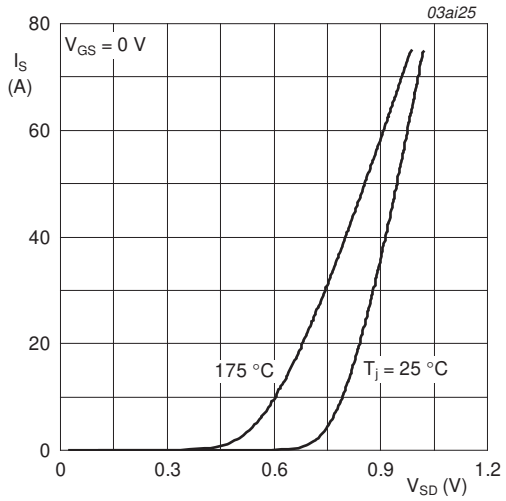
$I_D = 50A; V_{DS} = 15V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

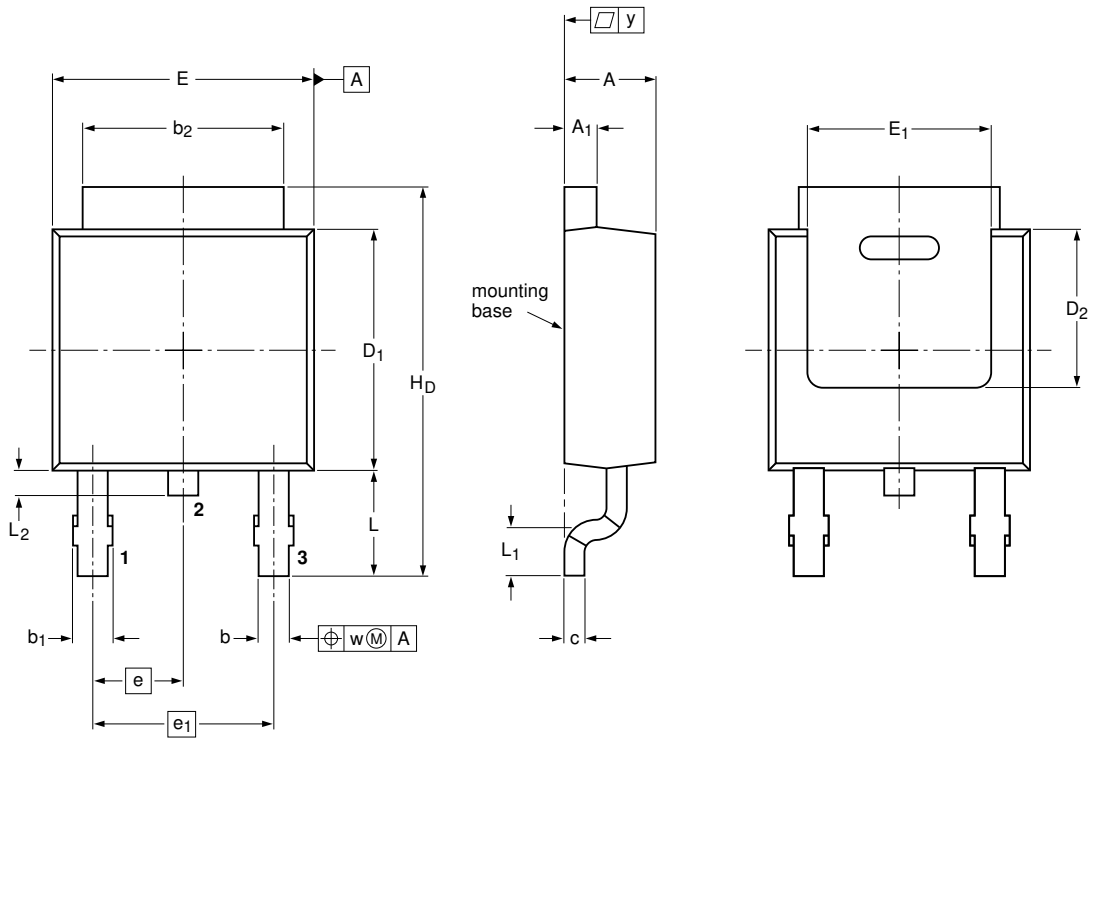


$T_j = 25°C$ and $175°C; V_{GS} = 0V$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 14. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD101NQ03LT v.5	20111031	Product data sheet	-	PHD101NQ03LT v.4
Modifications:	• Various changes to content.			
PHD101NQ03LT v.4	20090609	Product data sheet	-	PHD101NQ03LT v.3

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: salesaddresses@nxp.com

11. Contents

For more information, please visit: http://www.nxp.com
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