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PHM18NQ15T

TrenchMOS™ standard level FET

Rev. 02 — 20 August 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- SOT96 (SO-8) footprint compatible
- Low thermal resistance
- Surface mounted package
- Low profile.

1.3 Applications

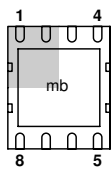
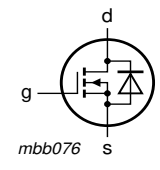
- DC-to-DC converter primary side switch
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 150 \text{ V}$
- $I_D \leq 19 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DSon} \leq 75 \text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT685-1 (QLPAK), simplified outline and symbol

| Pin | Description | Simplified outline | Symbol |
|---------|--|--|--|
| 1,2,3 | source (s) |  <p>Bottom view <small>MBL585</small></p> |  <p><small>mbb076</small></p> |
| 4 | gate (g) | | |
| 5,6,7,8 | drain (d) | | |
| mb | mounting base; connected to drain (d) | | |

SOT685-1 (QLPAK)

[1] Shaded area indicates pin 1 identifier.



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3. Ordering information

Table 2: Ordering information

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| PHM18NQ15T | QLPAK | HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; 6 x 5 x 0.85 mm | SOT685-1 |

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

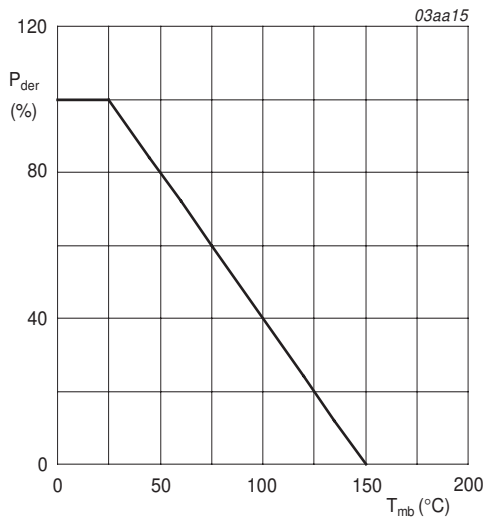
| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------|--|-----|----------|------|
| V_{DS} | drain-source voltage (DC) | $25\text{ °C} \leq T_j \leq 150\text{ °C}$ | - | 150 | V |
| V_{DGR} | drain-gate voltage (DC) | $25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 150 | V |
| V_{GS} | gate-source voltage (DC) | | - | ± 20 | V |
| I_D | drain current (DC) | $T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3 | - | 19 | A |
| | | $T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 | - | 12 | A |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3 | - | 76 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Figure 1 | - | 62.5 | W |
| T_{stg} | storage temperature | | -55 | +150 | °C |
| T_j | junction temperature | | -55 | +150 | °C |

Source-drain diode

| | | | | | |
|----------|-------------------------------------|--|---|----|---|
| I_S | source (diode forward) current (DC) | $T_{mb} = 25\text{ °C}$ | - | 19 | A |
| I_{SM} | peak source (diode forward) current | $T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ | - | 60 | A |

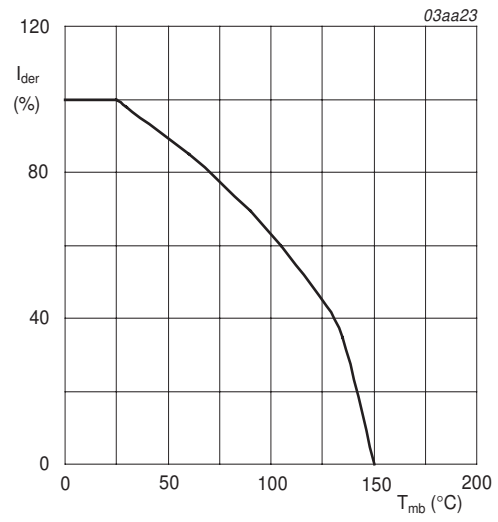
Avalanche ruggedness

| | | | | | |
|---------------|--|---|---|-----|----|
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D = 9.9\text{ A}$; $t_p = 0.16\text{ ms}$; $V_{DD} \leq 150\text{ V}$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$ | - | 170 | mJ |
|---------------|--|---|---|-----|----|



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

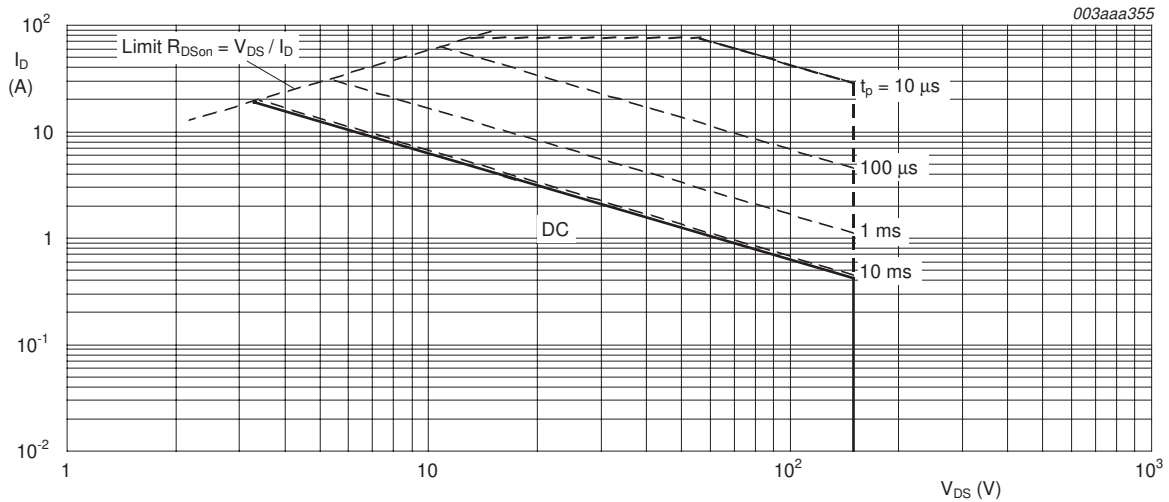
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 2 | K/W |

5.1 Transient thermal impedance

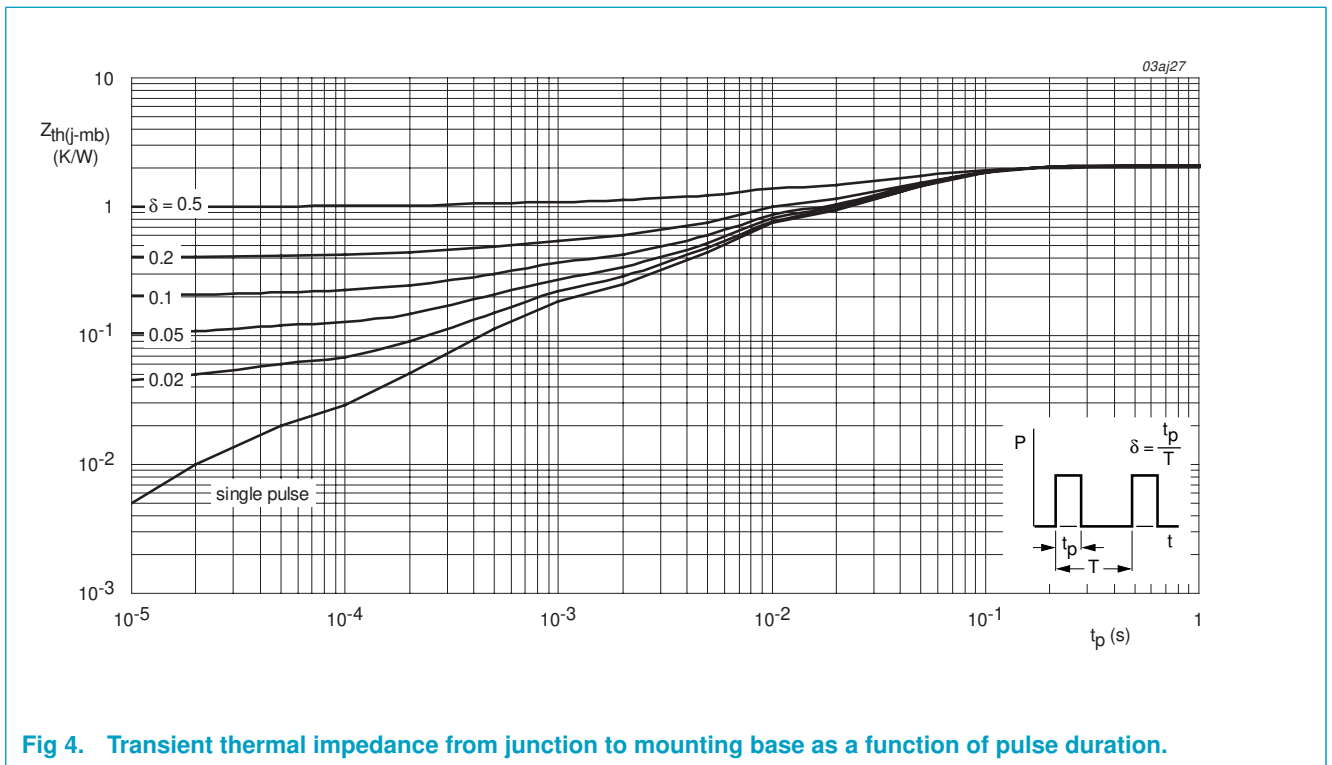


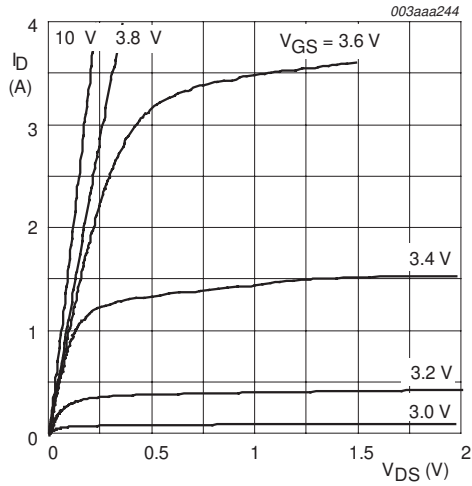
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

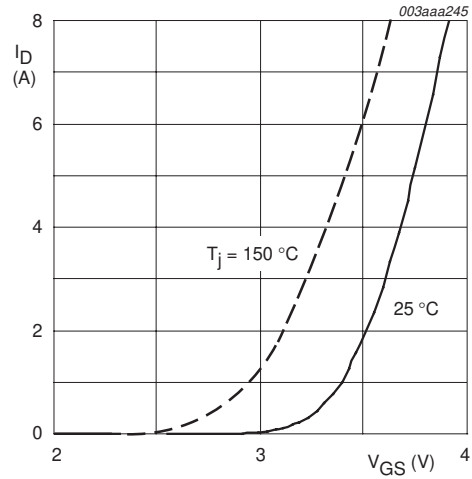
$T_j = 25\text{ °C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------------|---|---------------|-----------------|-----------------|--|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = -55\text{ °C}$ | 150 134 | - - | - - | V V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ $T_j = -55\text{ °C}$ | 2 1.2 - | 3 - - | 4 - 4.4 | V V V |
| I_{DSS} | drain-source leakage current | $V_{DS} = 120\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ | - - - | - - - | 1 100 | μA μA |
| I_{GSS} | gate-source leakage current | $V_{GS} = \pm 10\ \text{V}$; $V_{DS} = 0\ \text{V}$ | - | 10 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\ \text{V}$; $I_D = 12\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ $V_{GS} = 5\ \text{V}$; $I_D = 3\ \text{A}$; Figure 7 and 8 | - - - | 56 129 60 | 75 173 80 | m Ω m Ω m Ω |
| Dynamic characteristics | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D = 5\ \text{A}$; $V_{DD} = 75\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 13 | - | 26.4 | - | nC |
| Q_{gs} | gate-source charge | | - | 3.9 | - | nC |
| Q_{gd} | gate-drain (Miller) charge | | - | 8.8 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 12 | - | 1150 | - | pF |
| C_{oss} | output capacitance | | - | 187 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 61 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD} = 75\ \text{V}$; $I_D = 5\ \text{A}$; $V_{GS} = 10\ \text{V}$; $R_G = 6\ \Omega$ | - | 12 | - | ns |
| t_r | rise time | | - | 11 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 35 | - | ns |
| t_f | fall time | | - | 18 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain (diode forward) voltage | $I_S = 5\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 11 | - | 0.76 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 5\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_R = 90\ \text{V}$; $V_{GS} = 0\ \text{V}$ | - | 87 | - | ns |
| Q_r | recovered charge | | - | 162 | - | nC |



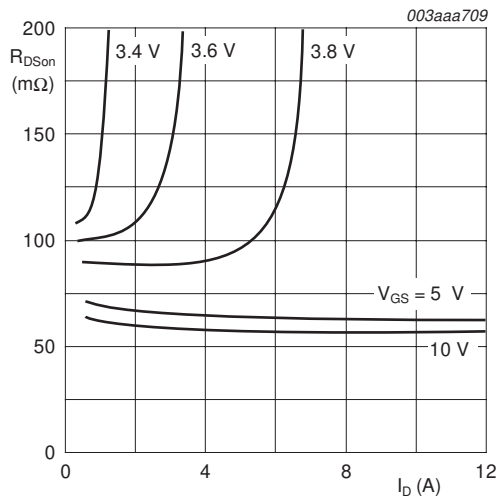
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



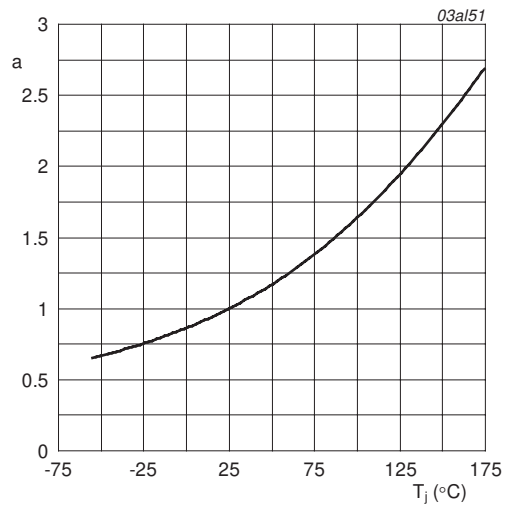
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



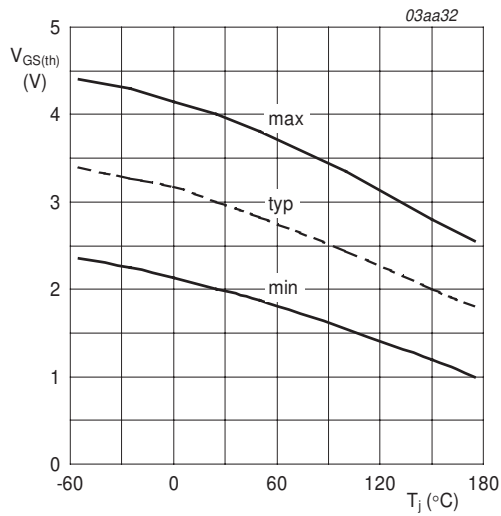
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



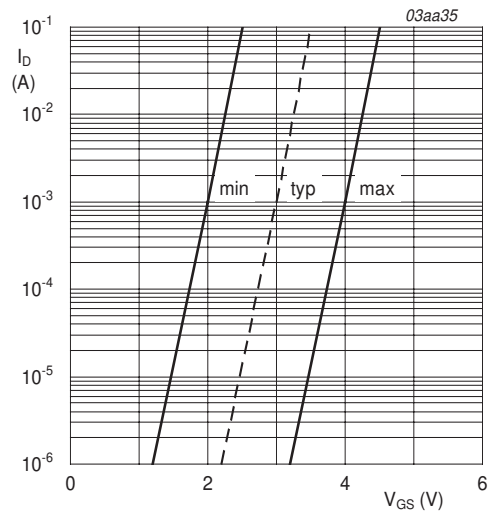
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



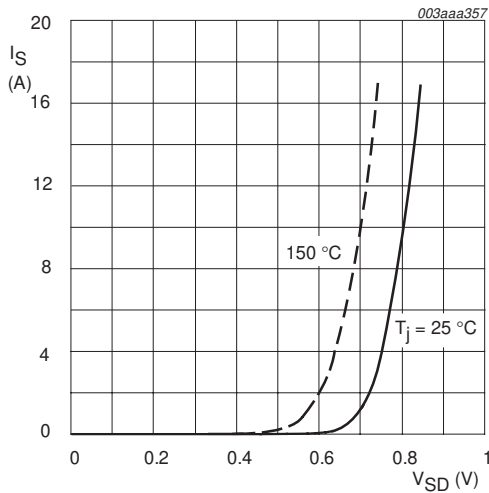
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



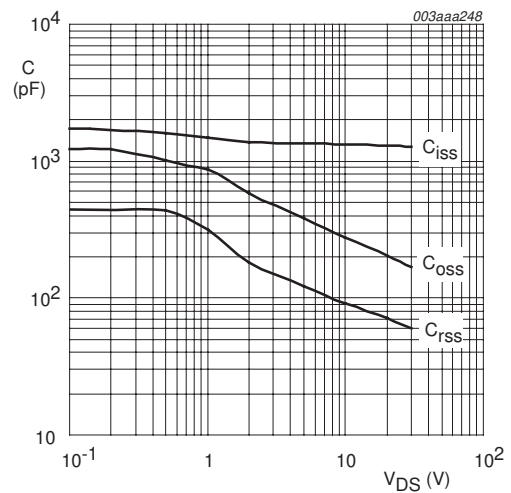
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



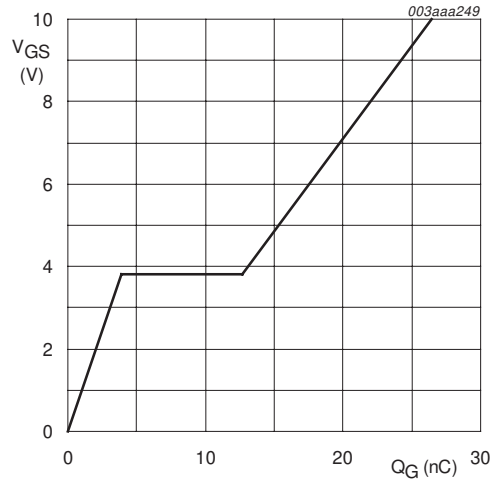
$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$I_D = 5\text{ A}; V_{DD} = 75\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 6 x 5 x 0.85 mm

SOT685-1

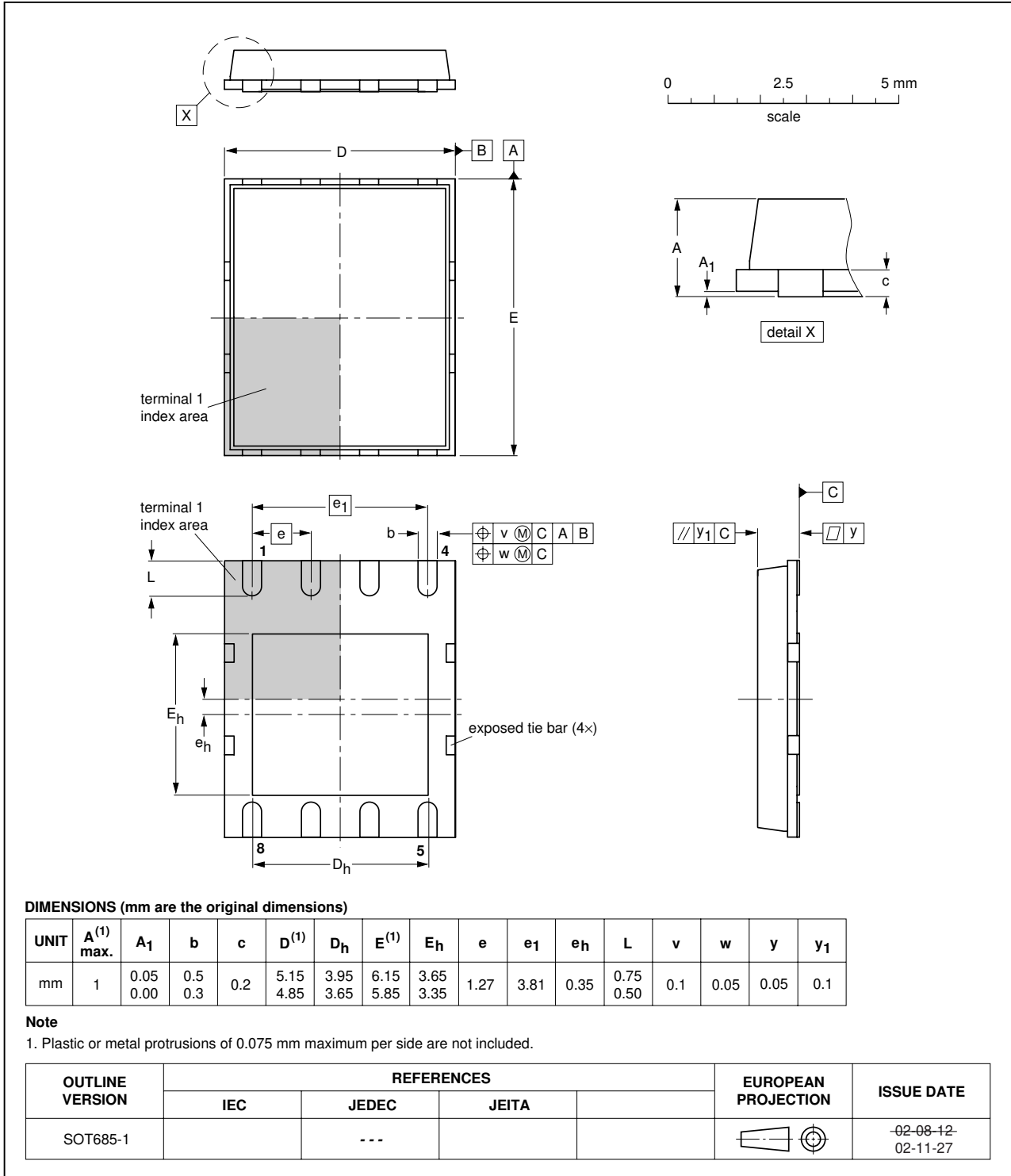


Fig 14. SOT685-1 (QLPAK).

8. Revision history

Table 6: Revision history

| Rev | Date | CPCN | Description |
|-----|----------|------|--|
| 02 | 20040820 | - | Product data (9397 750 13865) Modifications: <ul style="list-style-type: none">• Section 1.4 “Quick reference data” I_D data revised.• Section 3 “Ordering information” added to data sheet.• Table 3 “Limiting values” Avalanche ruggedness data added. I_D and I_{DM} data revised.• Figure 3 “Safe operating area; continuous and peak drain currents as a function of drain-source voltage.” revised.• Table 5 “Characteristics” Q_r data added, $Q_{g(tot)}$, Q_{gs} and Q_{gd} data corrected.• Figure 7 “Drain-source on-state resistance as a function of drain current; typical values.” revised. |
| 01 | 20030130 | - | Preliminary data (9397 750 10877) |

9. Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2][3]} | Definition |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contents

| | | |
|-----------|--------------------------------------|-----------|
| 1 | Product profile | 1 |
| 1.1 | Description | 1 |
| 1.2 | Features | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| 2 | Pinning information | 1 |
| 3 | Ordering information | 2 |
| 4 | Limiting values | 2 |
| 5 | Thermal characteristics | 4 |
| 5.1 | Transient thermal impedance | 4 |
| 6 | Characteristics | 5 |
| 7 | Package outline | 9 |
| 8 | Revision history | 10 |
| 9 | Data sheet status | 11 |
| 10 | Definitions | 11 |
| 11 | Disclaimers | 11 |
| 12 | Trademarks | 11 |

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