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Kind regards,

Team Nexperia



# PHPT610030NK

NPN/NPN high power double bipolar transistor

20 October 2014

Product data sheet

## 1. General description

NPN/NPN high power double bipolar transistor in a SOT1205 (LFPAK56D) Surface-Mounted Device (SMD) power plastic package.

PNP/PNP complement: PHPT610030PK.

NPN/PNP complement: PHPT610030NPK.

## 2. Features and benefits

- High thermal power dissipation capability
- Suitable for high temperature applications up to 175 °C
- Reduced Printed-Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

## 3. Applications

- Motor control
- Power management
- Load switch
- Linear mode voltage regulator
- Backlighting applications
- Relay replacement

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{CE0}$	collector-emitter voltage	open base	-	-	100	V
$I_C$	collector current		-	-	3	A
<b>Per transistor</b>						
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 3\text{ A}$ ; $I_B = 0.3\text{ A}$ ; pulsed; $t_p \leq 300\ \mu\text{s}$ ; $\delta \leq 0.02$ ; $T_{amb} = 25\text{ °C}$	-	75	110	m $\Omega$

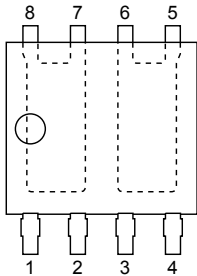
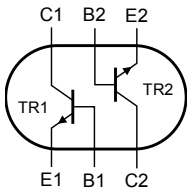


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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>LFPAK56D (SOT1205)</p>	 <p>sym140</p>
2	B1	base TR1		
3	E2	emitter TR2		
4	B2	base TR2		
5	C2	collector TR2		
6	C2	collector TR2		
7	C1	collector TR1		
8	C1	collector TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHPT610030NK	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PHPT610030NK	10030NK

## 8. Limiting values

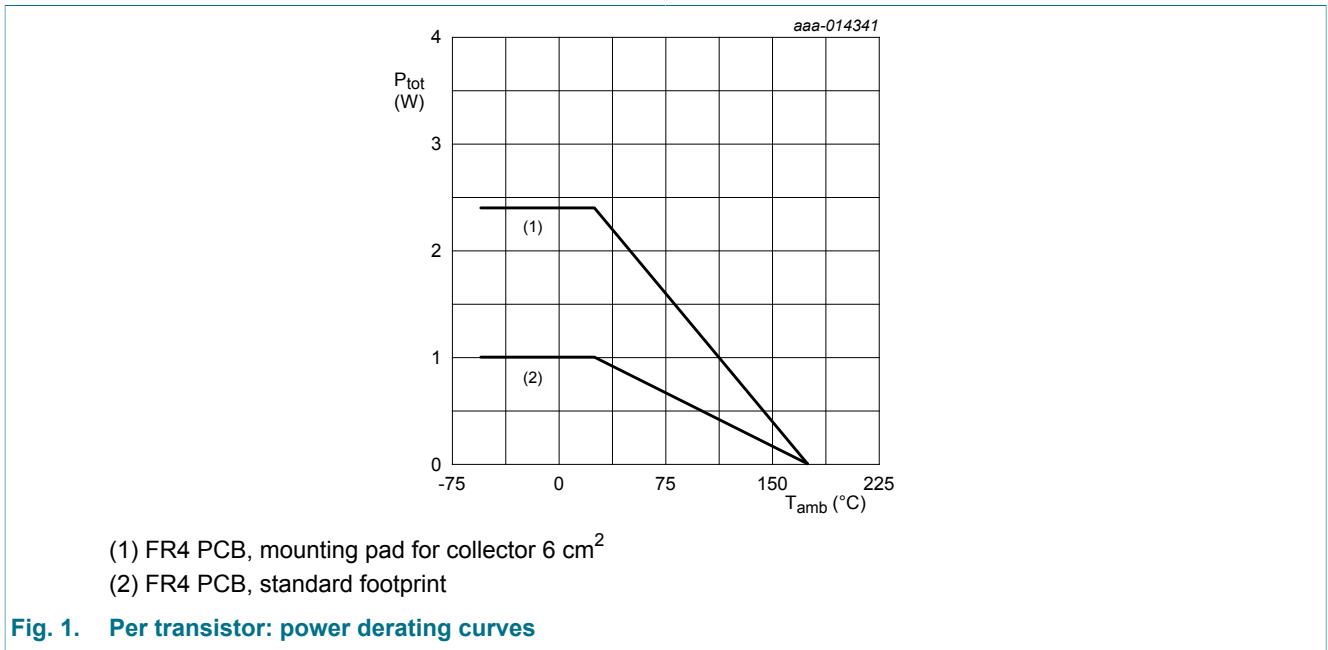
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor</b>					
$V_{CBO}$	collector-base voltage	open emitter	-	100	V
$V_{CEO}$	collector-emitter voltage	open base	-	100	V
$V_{EBO}$	emitter-base voltage	open collector	-	7	V
$I_C$	collector current		-	3	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	8	A
$I_B$	base current		-	0.5	A

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	1	W
			[2]	-	2.4	W
			[3]	-	25	W
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	1.25	W
			[4]	-	5	W
			[2]	-	3	W
T <sub>j</sub>	junction temperature			-	175	°C
T <sub>stg</sub>	storage temperature			-65	175	°C
T <sub>amb</sub>	ambient temperature			-55	175	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [3] Power dissipation from junction to mounting base.
- [4] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

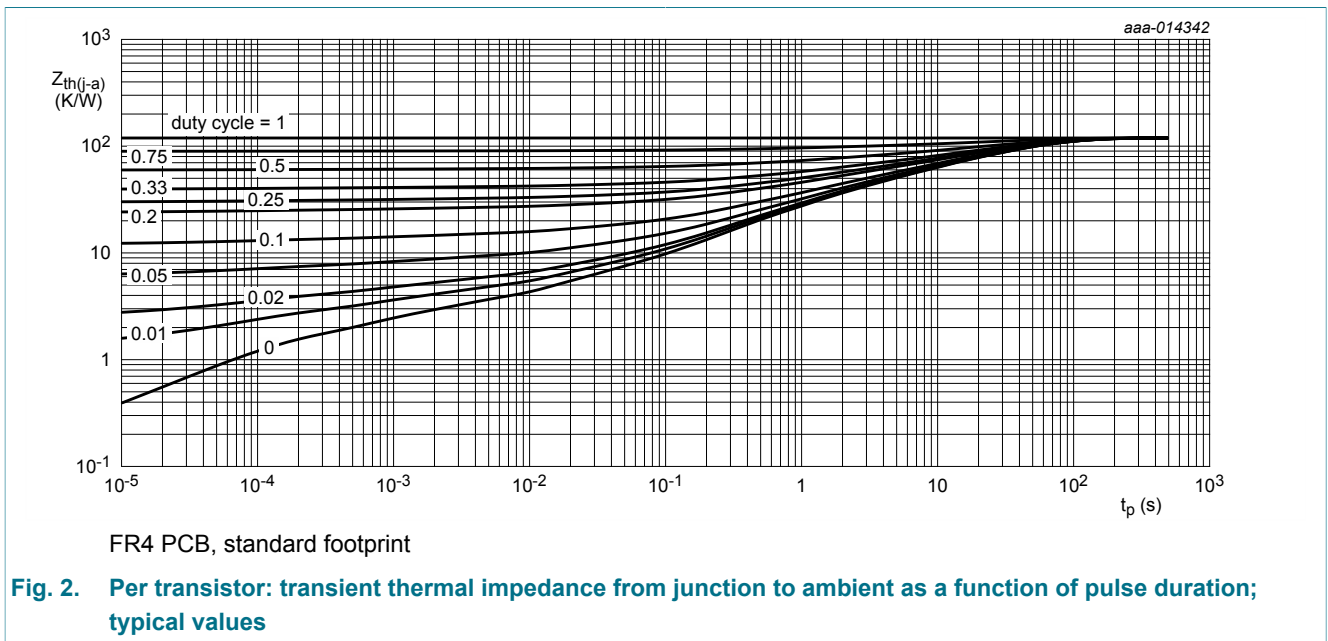


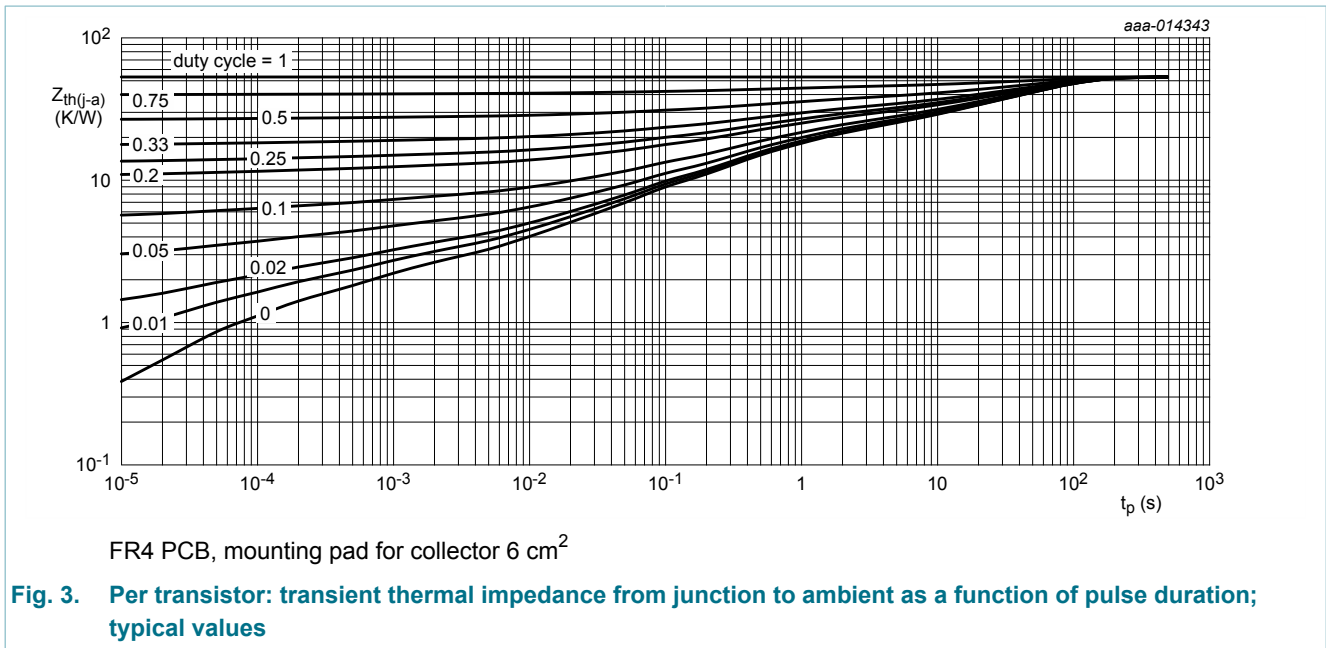
### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	150	K/W
			[2]	-	-	62.5	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	-	6	K/W
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	120	K/W
			[2]	-	-	50	K/W
			[3]	-	-	30	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.



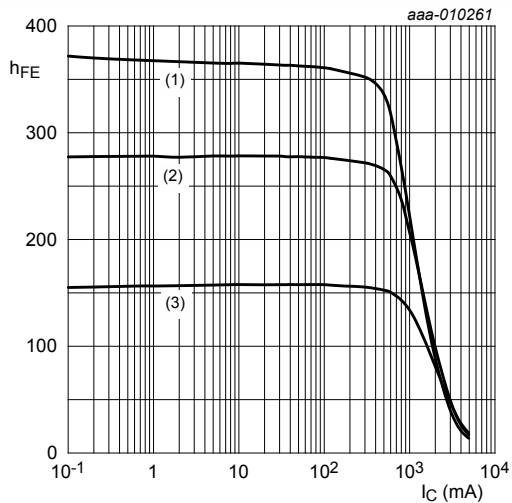


## 10. Characteristics

Table 7. Characteristics

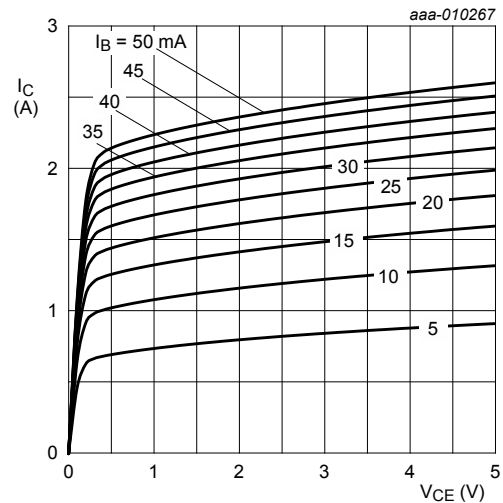
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 80 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
		V <sub>CB</sub> = 80 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	50	μA
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 80 V; V <sub>BE</sub> = 0 V; T <sub>amb</sub> = 25 °C	-	-	100	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 7 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 10 V; I <sub>C</sub> = 500 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	150	250	-	
		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 1 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	80	250	-	
		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 2 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	20	100	-	
		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 3 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	10	40	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	90	150	mV
		I <sub>C</sub> = 3 A; I <sub>B</sub> = 300 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	225	330	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 3\text{ A}; I_B = 0.3\text{ A};$ pulsed; $t_p \leq 300\ \mu\text{s};$ $\delta \leq 0.02; T_{amb} = 25\text{ }^\circ\text{C}$	-	75	110	m $\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 50\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ }^\circ\text{C}$	-	0.86	1	V
		$I_C = 2\text{ A}; I_B = 200\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ }^\circ\text{C}$	-	1	1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = 2\text{ V}; I_C = 0.1\text{ A};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ }^\circ\text{C}$	-	0.67	0.85	V
$t_d$	delay time	$V_{CC} = 12.5\text{ V}; I_C = 1\text{ A}; I_{Bon} = 50\text{ mA};$ $I_{Boff} = -50\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	20	-	ns
$t_r$	rise time		-	300	-	ns
$t_{on}$	turn-on time		-	320	-	ns
$t_s$	storage time		-	830	-	ns
$t_f$	fall time		-	470	-	ns
$t_{off}$	turn-off time		-	1300	-	ns
$f_T$	transition frequency		$V_{CE} = 10\text{ V}; I_C = 100\text{ mA}; f = 100\text{ MHz};$ $T_{amb} = 25\text{ }^\circ\text{C}$	-	140	-
$C_C$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	11	-	pF



$V_{CE} = 10\text{ V}$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

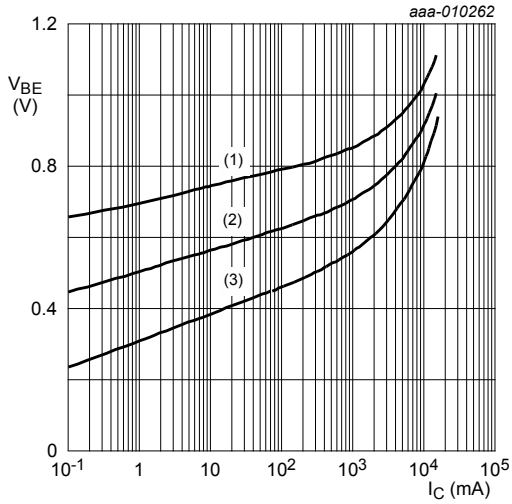
**Fig. 4. DC current gain as a function of collector current; typical values**



$T_{amb} = 25\text{ }^\circ\text{C}$

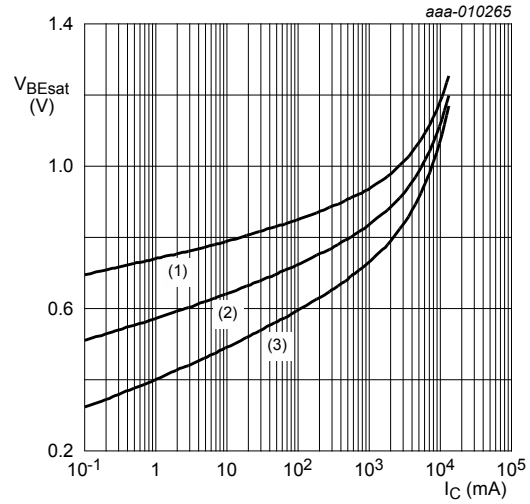
**Fig. 5. Collector current as a function of collector-emitter voltage; typical values**





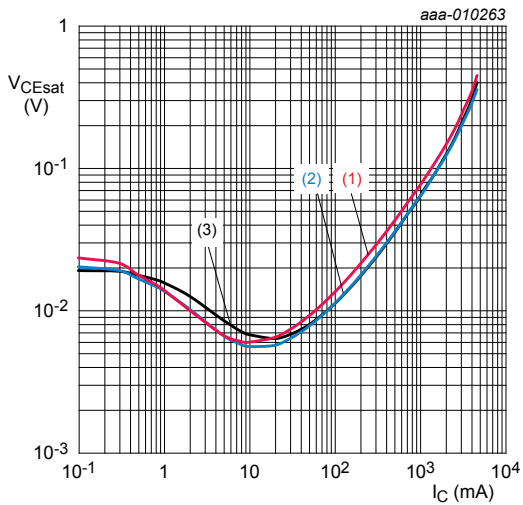
$V_{CE} = 2\text{ V}$   
 (1)  $T_{amb} = -55\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

**Fig. 6. Base-emitter voltage as a function of collector current; typical values**



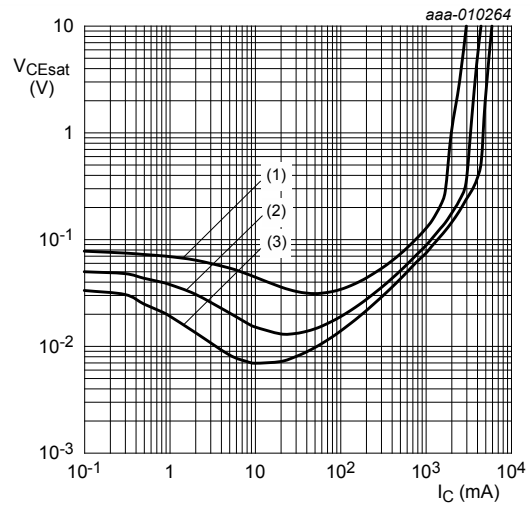
$I_C/I_B = 20$   
 (1)  $T_{amb} = -55\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

**Fig. 7. Base-emitter saturation voltage as a function of collector current; typical values**



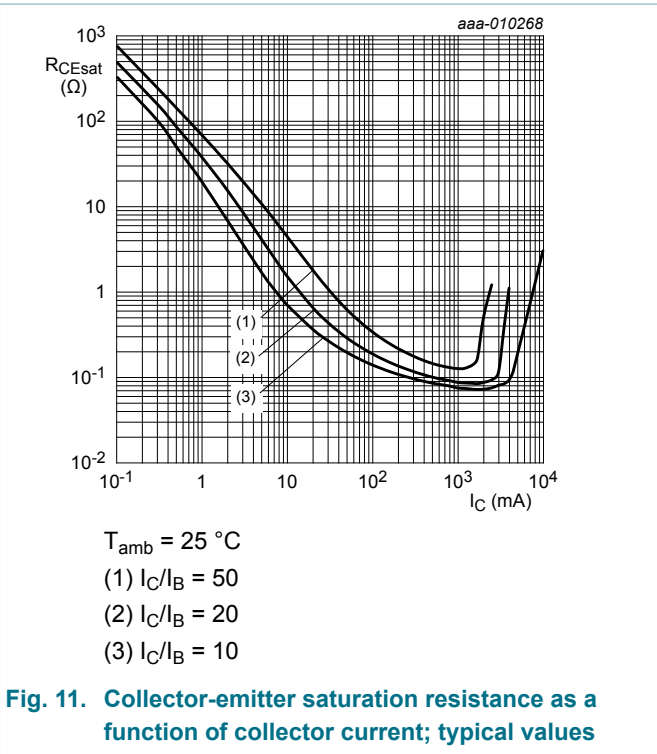
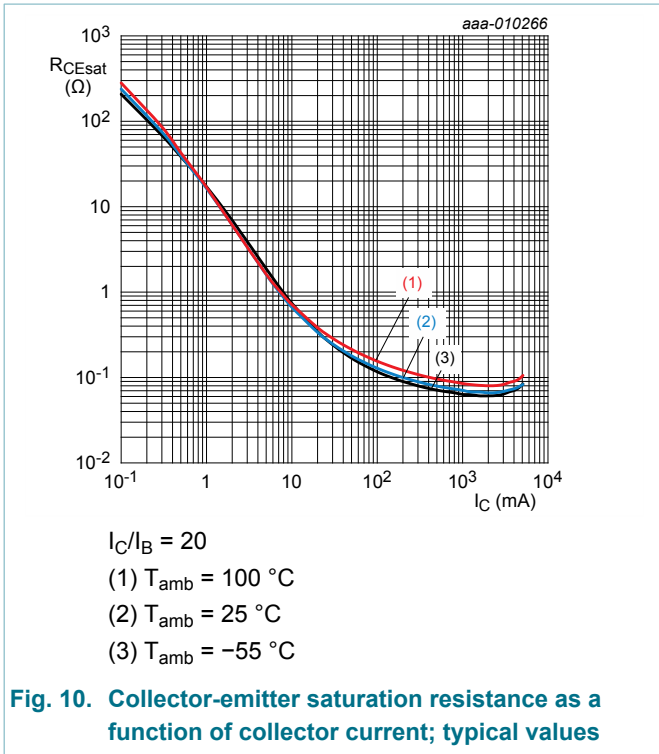
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

**Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values**



$T_{amb} = 25\text{ }^\circ\text{C}$   
 (1)  $I_C/I_B = 50$   
 (2)  $I_C/I_B = 20$   
 (3)  $I_C/I_B = 10$

**Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values**



### 11. Test information

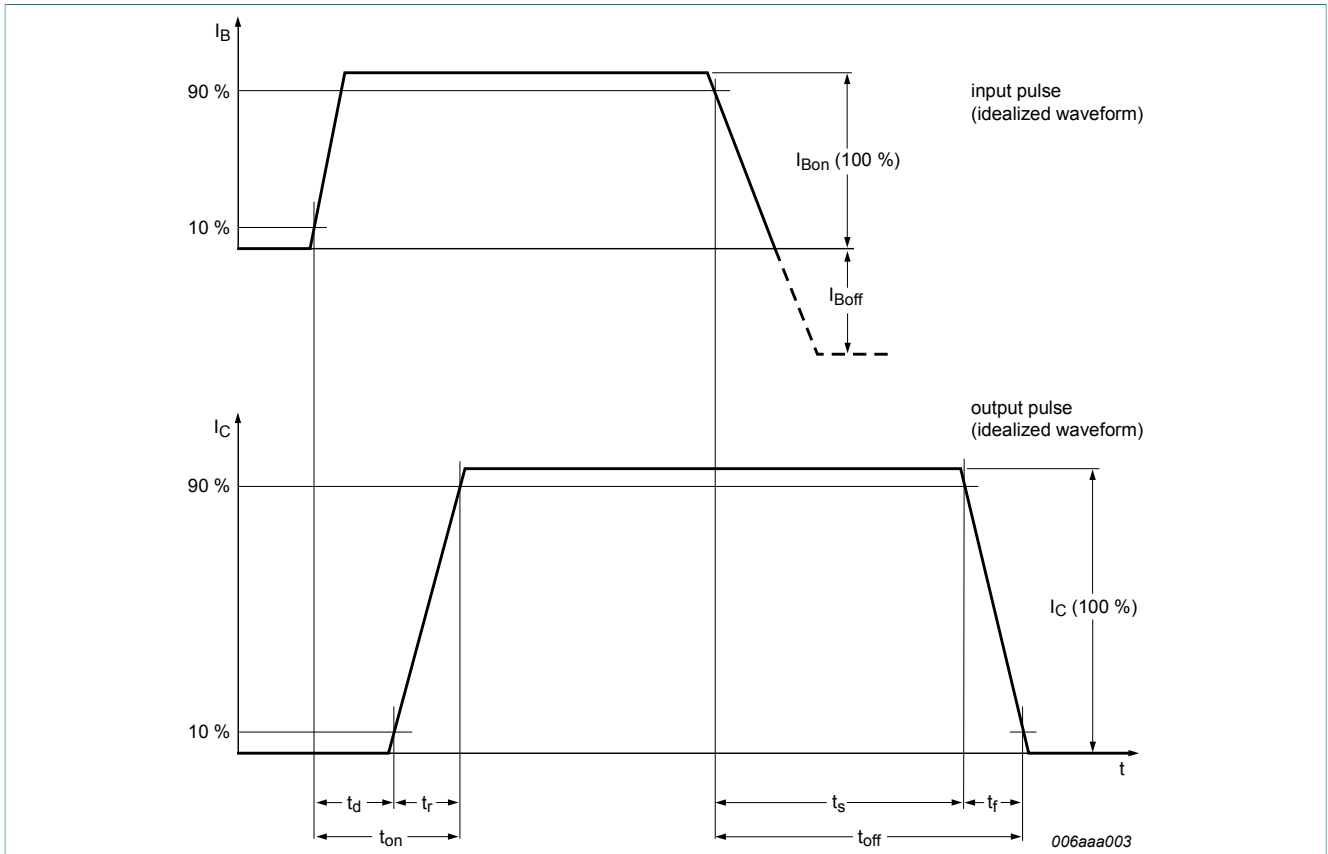


Fig. 12. BISS transistor switching time definition

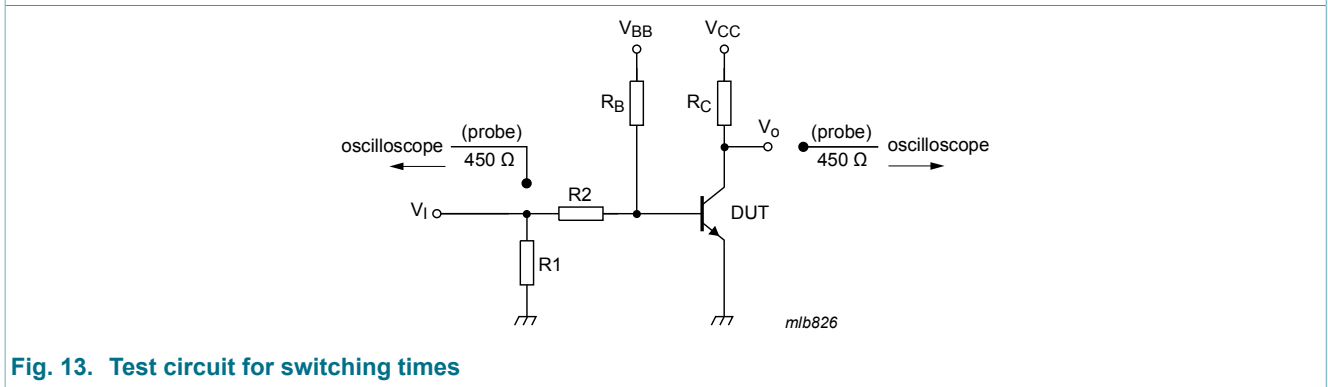


Fig. 13. Test circuit for switching times

#### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

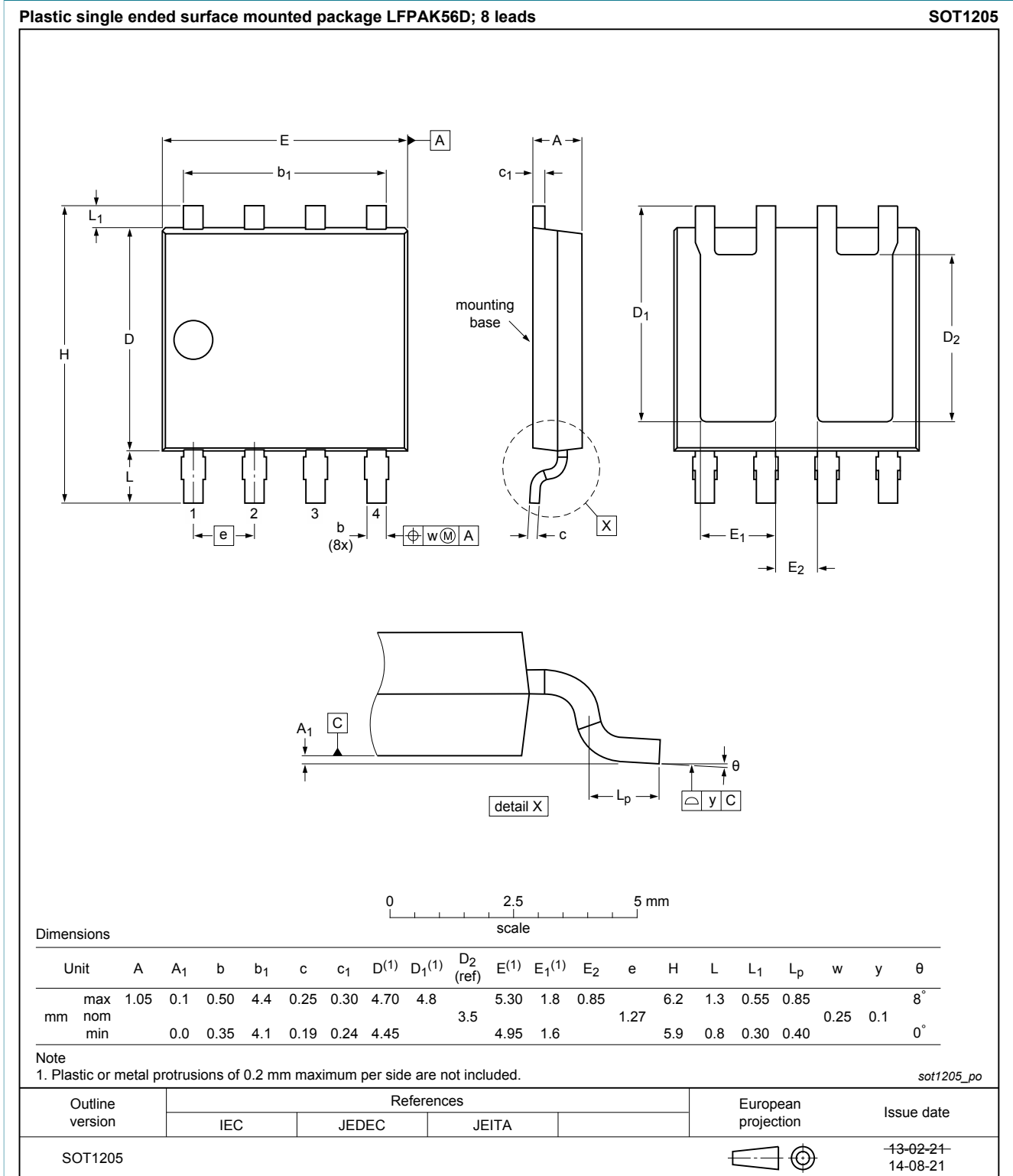


Fig. 14. Package outline LFAK56D (SOT1205)

### 13. Soldering

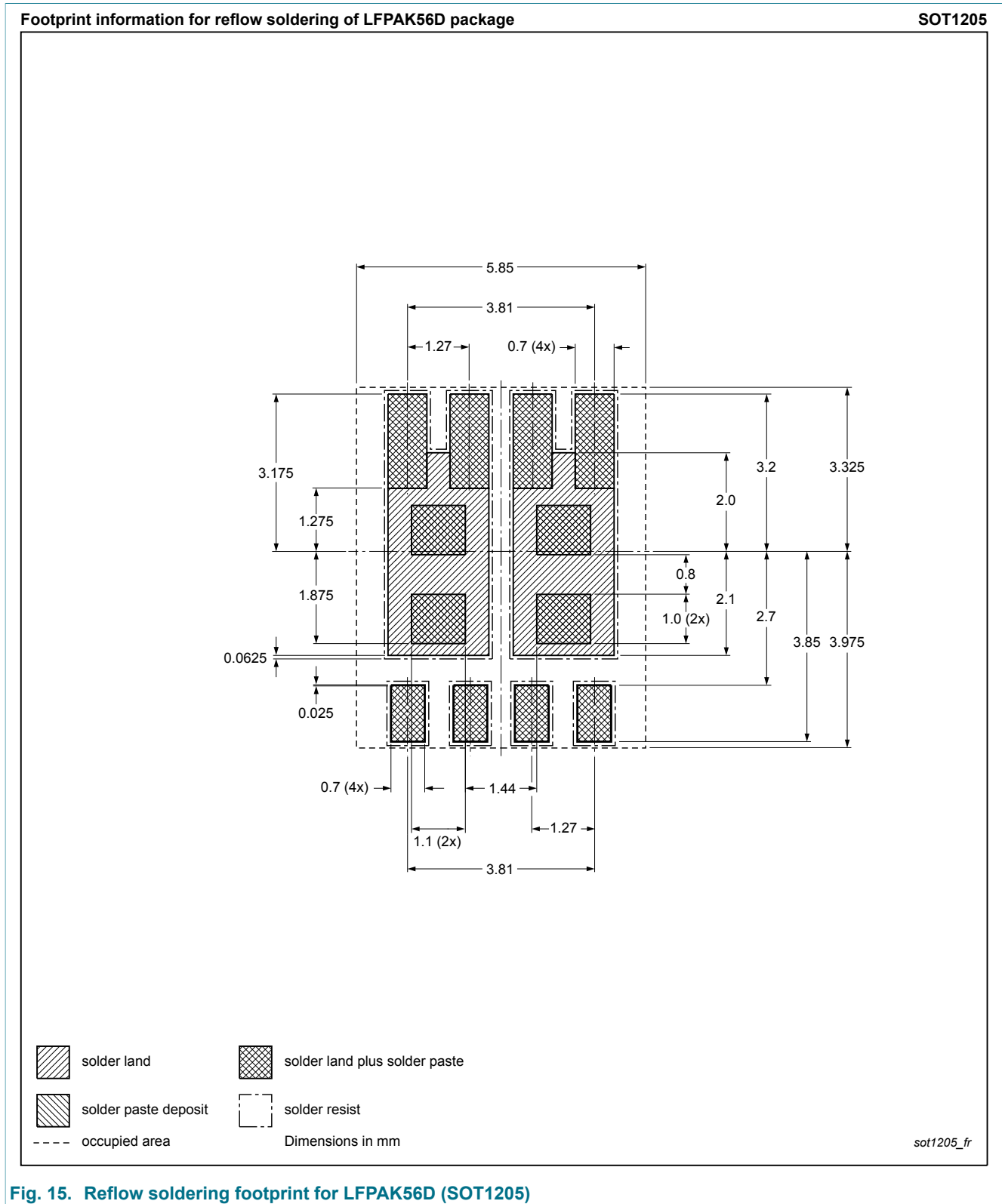


Fig. 15. Reflow soldering footprint for LFPAK56D (SOT1205)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT610030NK v.1	20141020	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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