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PHY1076-01
125Mbps to 2.7Gbps Laser Driver/ Post Amp with Digital Diagnostics

Features

- Multi-rate from 125Mbps to 2.7Gbps
- Laser driver output stage with 70mA max modulation drive and 100mA bias current
- Programmable mean power control loop
- Temperature compensated modulation current
- Integrated limiting amplifier with selectable swing CML output
- Programmable receiver low pass filter
- Integrated Loss Of Signal function
- Digital diagnostic mode compliant with SFF-8472 using an external MCU
- Stand-alone mode where device parameters are loaded from an external EEPROM
- -40°C to +95°C ambient operating range
- 36pin 6mm x 6mm QFN package
- Eye safety logic

Applications

Fibre Channel 1x, 2x
Gigabit Ethernet, SONET/SDH
OC-3, OC-12, OC-48

Description

The PHY1076-01 is a combined Laser driver and limiting amplifier with support for Digital Diagnostic Monitoring for use within small form factor modules for Fibre Channel, GbE and SONET/SDH applications.

The transmitter integrates a high speed output stage with programmable bias and modulation currents, controlled through a 2-wire serial interface. The mean power control loop allows connection in common anode configuration.

A Loss Of Signal (LOS) detector is included with detection based on either the receiver photo detector average current or received signal modulation amplitude.

When used in digital diagnostics mode the integrated A/D converters measuring temperature, TX Bias, Supply Voltage, RX Signal Strength and Mean Power are read via a 2-wire serial interface. An external Microcontroller Unit (MCU) is used for calibrating real time diagnostic monitors and alarm generation.

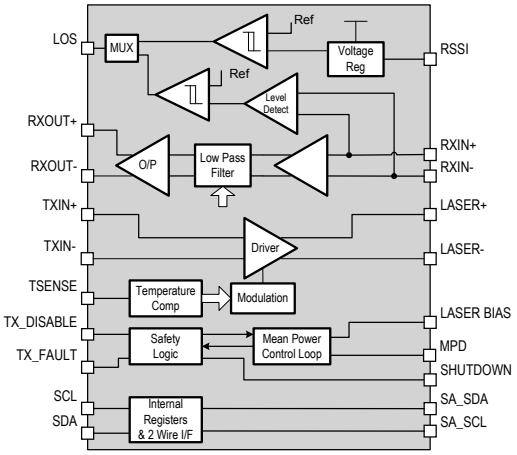

Figure 1 - Outline Block Diagram

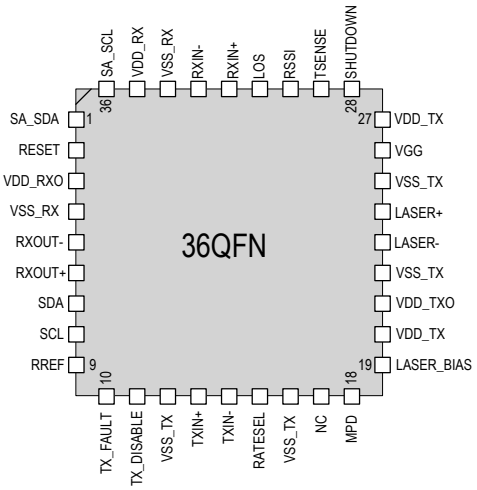

Figure 2 - Device Pin Out (Top View)

19-5684; Rev 9/12

Table of Contents

1. Ordering Information

Please refer to the Packaging section for test and package location ordering code definitions.

Part Number	Description	Package
PHY1076-01QD-RR	Enhanced 2.7G LASER driver and Post Amp	QFN36, 6mmx6mm in Tape and Reel, RoHS compliant (*see Figure 41)*
PHY1076-01QS-RR **NOT FOR USE IN NEW DESIGNS**	Enhanced 2.7G LASER driver and Post Amp	QFN36, 6mmx6mm in Tape and Reel, RoHS (*see Figure 41)*

2. Pin Description

Pin No	Name	Direction	Type	Description
1	SA_SDA[1,4]	I/O	LVTTL	2-wire serial interface. Connects to EEPROM in stand-alone mode
2	RESET	I/P	CMOS	Reset
3	VDD_RXO[2]		Power	Limiting amplifier output power supply
4	VSS_RX[3]		Ground	Receiver section ground connection
5	RXOUT-	O/P	CML	Limiting amplifier differential serial data output.
6	RXOUT+	O/P	CML	Limiting amplifier differential serial data output.
7	SDA[4]	I/O	LVTTL	2-wire serial data interface. Used in Digital Diagnostics Mode.
8	SCL[4]	I/P	LVTTL	2-wire serial interface clock. Used in Digital Diagnostics Mode.
9	RREF	I/P	Analog	Connect to Ground through a 10k resistor
10	TX_FAULT	O/P	LVTTL (open collector)	Transmit fail alarm. A logic 1 indicates a fault in the transmission system. Requires external pull up for SFP MSA compliance
11	TX_DISABLE[4]	I/P	LVTTL	Output disable (active high). Disables Laser drive. On chip 8k pull up
12	VSS_TX[3]		Ground	Transmission circuitry ground connection
13	TXIN+	I/P	CML	Differential Laser driver input from host
14	TXIN-	I/P	CML	Differential Laser driver input from host
15	RATESEL	I/P	LVTTL	Toggles between two low pass filter characteristics. External 30k pull down resistor required for SFP MSA compliance
16	VSS_TX[3]		Ground	Transmission circuitry ground connection
17	NC			No connection. Leave open circuit
18	MPD	I/P	Analog	Monitor photodiode input
19	LASER_BIAS	O/P	Analog	Laser bias current output
20	VDD_TX[2]		Power	Transmission circuitry power supply connection
21	VDD_TXO[2]		Power	Transmission circuitry power supply connection
22	VSS_TX[3]		Ground	Transmission circuitry ground connection
23	LASER-	O/P	High speed	Laser differential driver output

24	LASER+	O/P	High speed	Laser differential driver output
25	VSS_TX[3]		Ground	Transmission circuitry ground connection
26	VGG		Ground	Ground substrate connection
27	VDD_TX[2]		Power	Transmission circuitry power supply connection
28	SHUTDOWN	O/P	CMOS	Gate drive for optional Laser shutdown FET switch
29	TSENSE	I/P	Analog	External temperature sensing transistor connection
30	RSSI	I/P	Analog	Receive signal strength indicator & regulated supply for Rx photodiode
31	LOS	O/P	LVTTL (open collector)	Loss of signal output. Requires external pull up for SFP MSA compliance
32	RXIN+	I/P	CML	Limiting amplifier differential serial data input
33	RXIN-	I/P	CML	Limiting amplifier differential serial data input
34	VSS_RX[3]		Ground	Receiver ground connection
35	VDD_RX[2]		Power	Limiting amp power supply
36	SA_SCL[1,4]	I/P	LVTTL	EEPROM 2-wire serial interface clock
-	PADDLE		Ground	Ground / Thermal Paddle

1 Used in stand-alone mode only
2 All VDDs are internally connected by back-to-back protection diodes. VDDs should not be powered up independently.
3 All VSSs are internally connected to the IC substrate connection.
4 Internally pulled high with an 8kΩ pull-up resistor.

3. Key Specifications

3.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage		- 0.5		+6.5	V
Voltage on any pin		VSS - 0.5		VDD + 0.5	V
Storage Temperature				150	°C
Soldering Temperature	For 25 seconds			260	°C
Junction Temperature				140	°C
ESD	Human Body Model	2			kV

Under absolute maximum rating conditions device not guaranteed to meet specifications; permanent damage may be incurred by operating beyond these limits.

3.2. Continuous Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	Continuous operation	2.97	3.3	3.63	V
Current consumption	Idd = Iddo + (Km*Imod) + (Kb*Ibias)				mA
Current Consumption (Iddo)	High Swing, OMA LOS, Vref = 113 2448Mbps Filter 155Mbps Filter			 118 110	mA
Current consumption (Km)				0.536	
Current consumption (Kb)				0.075	
Operating temperature	Ambient Still Air, Max Bias and Modulation Current	-40	25	+95	°C

3.3. Receiver

3.3.1. Receive Limiting Amplifier

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sensitivity		Differential, BER=1*10^{-12} (125 - 2.125Gbps)		5	7.5	mVpp
Max Differential Input		TJ within spec	1200			mVpp
Input Return Loss		Differential, f<2GHz, device powered on		10		dB
Output Return Loss		Differential, f<2GHz, device powered on		10		dB
Low Frequency Cutoff		High pass 3dB point for RX system		15		kHz
Differential Output Swing		High swing mode Low swing mode	800 400		1100 520	mVpp
Total Jitter, Tj		Measured over RX input voltage range 125Mbps - 2.7Gbps			100	mUI pp
Duty Cycle Distortion		125Mbps - 2.7Gbps	40		60	%
Output Resistance		RXOUT+/- Single ended to VDD_RXO	40	50	60	Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Impedance		Differential RXIN+ to RXIN-, DC	85		115	Ω
Rate select change time	t_ratesel	Using RATESEL pin			5	μs
Output Rise and Fall Times (20%-80%)		155 Mbps filter, slow CMLslew = '1' , low swing		200	300	ps
		155 Mbps filter, fast CMLslew = '0', low swing		192	300	
		155 Mbps filter, slow CMLslew = '1' , high swing		261	400	ps
		155 Mbps filter, fast CMLslew = '0', high swing		253	400	
		2488 Mbps filter, slow CMLslew = '1' , low swing		71	100	ps
		2488 Mbps filter, fast CMLslew = '0', low swing		63	90	
		2488 Mbps filter, slow CMLslew = '1', high swing		96	120	ps
		2488 Mbps filter, fast CMLslew = '0', high swing		83	110	

3.3.2. RSSI Indicator and Rx PD Regulator

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Voltage on RSSI pin		Ireg=2mA (10nF & 100Ω minimum load)	2.4			V
Current sourced by RSSI pin		Measured using Rx Power ADC	0		2000	μA

3.3.3. Receive Photocurrent LOS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RSSI LOS assert time					10	μs
RSSI LOS de-assert time					40	μs
Electrical Hysteresis		$20\log_{10}$ (RSSIdeassert / RSSIassert)	2		4	dB
RSSI LOS assert level range		Set by AVG_LOS_set, Address F4h	4.0		411	μA

3.3.4. OMA LOS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OMA LOS assert time	t_loss_on				100	μs
OMA LOS de-assert time	t_loss_off				20	μs
Electrical Hysteresis		$20\log_{10}$ (Vdeassert / Vassert)	2.5		5.5	dB
OMA LOS assert level		Set by OMA_LOS_set, Address F3h	10		50	mV

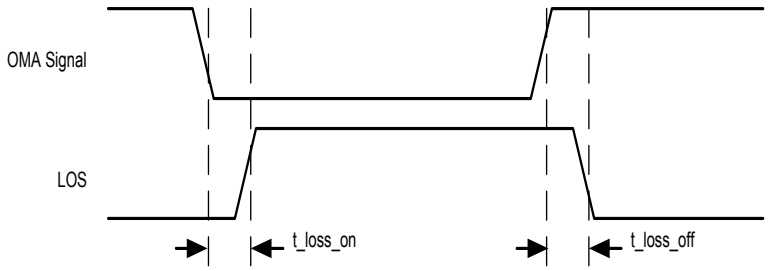

Figure 3 - OMA LOS Detection

3.4. Transmitter

3.4.1. Transmitter Inputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-Speed Data Input Signal Voltage[1]		Differential, AC-coupled, from 125Mbps to 2.7Gbps	200		2400	mVpp
High-Speed Data Input Impedance		Differential, DC	80	100	120	Ω
Input Return Loss		Differential, f<2GHz, device powered on		10		dB
Input common mode return loss		Both inputs shorted together, measured using 25Ω □source termination, 100MHz – 2.5GHz		10		dB

3.4.2. Laser Driver

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Modulation Current	I_{mod}		7		70	mA
Electrical 20% to 80% rise / fall time		Measured using 50Ω□effective termination, AC and DC coupled applications		55	65	ps
Total Jitter contribution		Measured over modulation current range			100	mUI pp
Laser output compliance range		Allowed voltage for Laser driver output pins in dynamic operation, referenced to ground (VSS_TX).	600			mV
Bias current output compliance		Minimum allowed voltage for pin LASER_BIAS, referenced to ground (VSS_TX)	300			mV

3.4.3. Laser Mean Power Control Loop

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Current			0.5		100	mA
Bias current off		Transmitter disabled			10	μA
Max current at MPD pin		Sink current			2.6	mA
Turn on/off overshoot		Bias current overshoot, Loop_BW=1			15	%
APC -3dB Loop Bandwidth	f_{Loop_BW}	Loop_BW = “0” Loop_BW = “1”		5 15		kHz
Bias loop settling time	t_settle	Loop_BW = “0” Loop_BW = “1”		5 500		ms μs

3.4.4. Eye Safety Internal Fixed Limits

Operation outside these limits causes a TX_FAULT to be asserted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High supply voltage assert limit	V_{eyeHa}		3.75		4.10	V
High supply voltage de-assert limit	V_{eyeHd}		3.65		4.05	V
High Supply Hysteresis			0.05		0.15	V
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Low supply voltage assert limit	V_{eyeLa}		2.70		2.95	V
Low supply voltage de-assert limit	V_{eyeLd}		2.75		2.95	V
Low Supply Hysteresis			0.01		0.15	V
RREF pin voltage limit		RREF voltage applied to pin after calibration	0.9		1.1	V

3.4.5. Fault Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Time to initialize	t_init	From power on or application of Vcc>2.97V during plug in			300	ms
Hard TX_DISABLE assert time	t_off	Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal			2	μs
Hard TX_DISABLE negate time	t_on	Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal			800	μs
Hard TX_FAULT assert time	t_fault	Time from fault to TX_FAULT on			100	μs
TX_DISABLE pulse width	t_reset	Time TX_DISABLE must be held high to reset TX_FAULT	5			μs
TX_FAULT deassert time	t_faultdass	Time to deassert TX_FAULT after TX_DISABLE			300	ms

3.4.6. Diagnostic Timing Diagrams

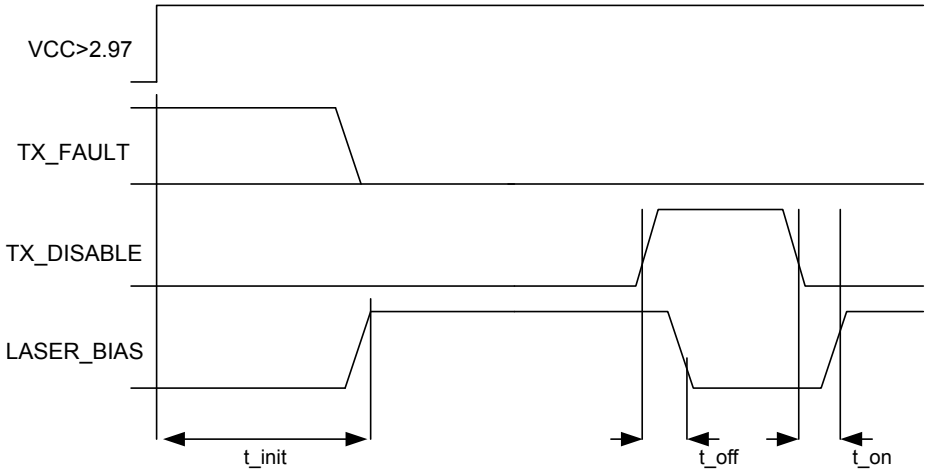

Figure 4 - Device turn on

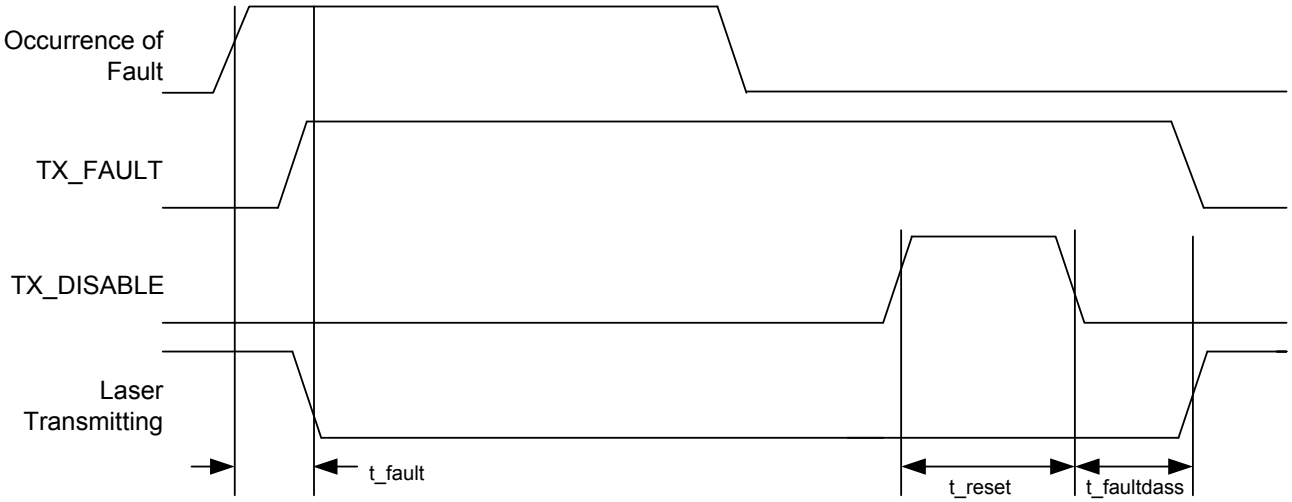

Figure 5 - Fault detection

3.5. 2-Wire Serial Interface

3.5.1. AC Electrical Characteristics

Parameter	Symbol	Comment	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}		0		100	kHz
LOW period of the SCL clock	t_{LOW}		4.7		–	µs
HIGH period of the SCL clock	t_{HIGH}		4.0		–	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7		–	µs
Hold time (repeated) START condition	$t_{HD:STA}$		4.0		–	µs
Data hold time	$t_{HD:DAT}$		0		3.45	µs
Data set-up time	$t_{SU:DAT}$		250		–	ns
Rise time of both SDA and SCL signals	t_R		–		1000	ns
Fall time of both SDA and SCL signals	t_F		–		300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0		–	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7		–	µs
Output fall time from VIHmin to VILmax	t_{of}	10pF < C_b(1) < 400pF	0		250	ns
Capacitance for each I/O pin	C_i	See note 1	–		10	pF

1 C_b = capacitance of a single bus line in pF.

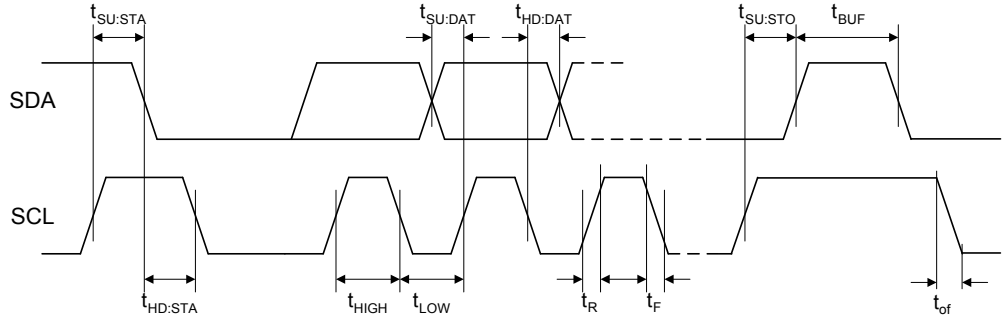

Figure 6 - SDA and SCL bus timing

3.5.2. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level input voltage	V_{IL}		- 0.5		0.3 V_{DD}	V
High level input voltage	V_{IH}		0.7 V_{DD}		V_{DD} + 0.5	V
Low level O/P voltage	V_{OL}	3 mA sink current	0		0.4	V
I/P current each I/O pin	I_i	$0.1V_{DD} < V_i < 0.9V_{DD}$	-10		10	mA

3.5.3. DC Characteristics: TX_FAULT; TX_DISABLE;LOS

Parameter		Comment	Min	Typ	Max	Unit
LVTTL Voltage Out High		External 4.7k to 10k pull-up	Host VCC - 0.5		Host VCC + 0.3	V
LVTTL Voltage Out Low		External 4.7k to 10k pull-up	0		0.5	V
LVTTL Voltage In High		Internal pull-up	2.0		VDD + 0.3	V
LVTTL Voltage In Low		Internal pull-up	0		0.8	V
R pull-up		Internal pull-up	6		10	kΩ

3.6. Typical Operating Characteristics

3.6.1. Electrical Receiver Eye Diagrams (3.3V; Ta = 25°C; PRBS 2^{7-1})

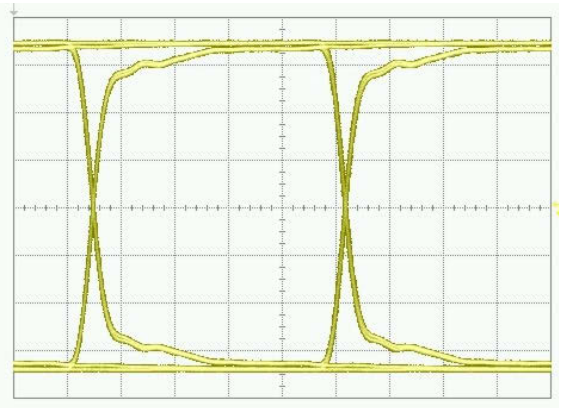

Figure 7 - 2.125Gbps High swing mode

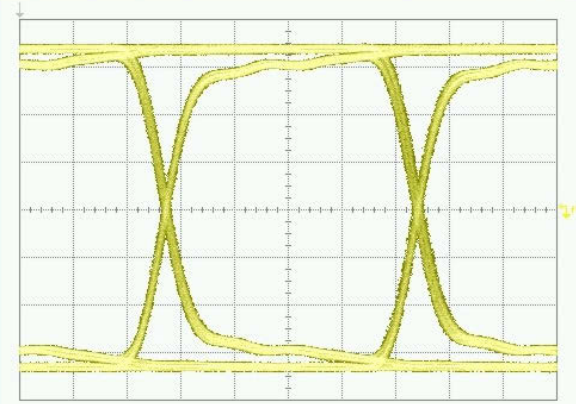

Figure 8 - 1.065Gbps High swing mode

3.6.2. Optical Transmit Eye Diagrams (3.3V; Ta = 25°C; PRBS 2^{23-1})

Transmitter setup with P_{mean} = -3.5dBm; E.R. =10dB

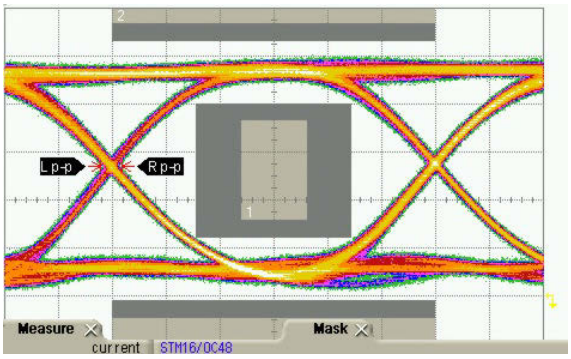

Figure 9 – 2.5 Gbps; STM16/OC48 Filter and mask

4. Functional Description

4.1. Overview

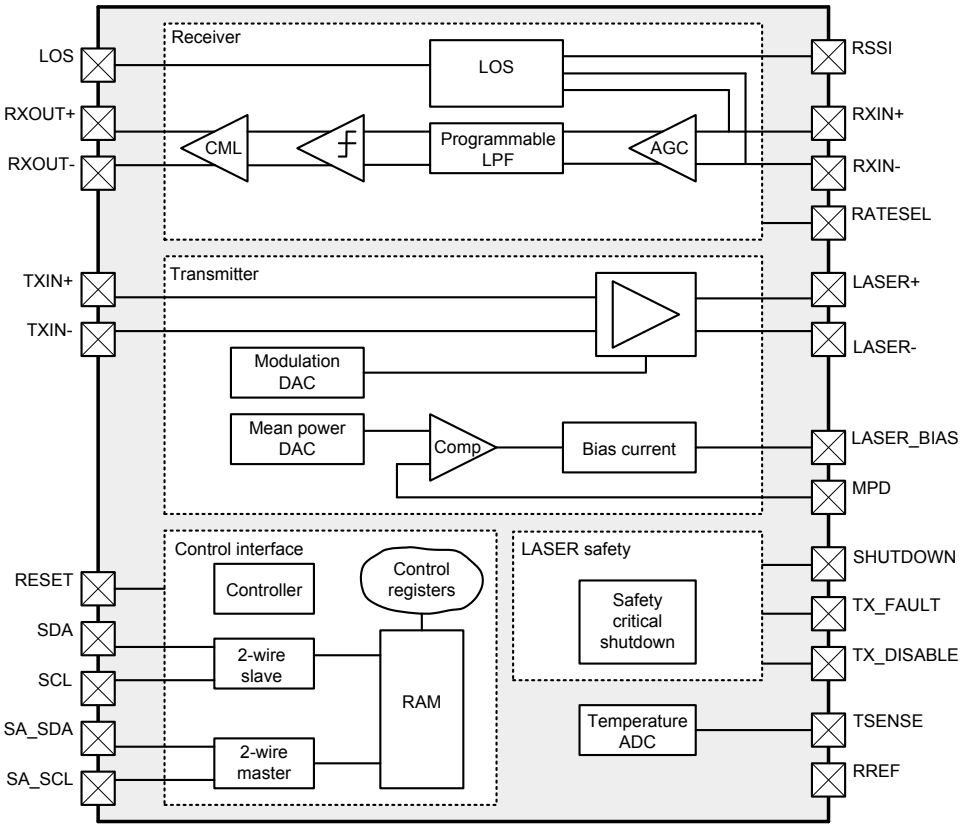

Figure 10 - Top-level block diagram of the PHY1076-01

4.2. Receiver Features

The receiver input is designed to be AC-coupled to the transimpedance amplifier, with internal 100Ω differential termination. The AGC amplifier is followed by a low-pass filter with programmable cut-off frequency, enabling the PHY1076-01 receiver to support six discrete data rates in the range 125 Mbps to 2.7 Gbps.

The filter output is followed by a limiting stage. For minimum duty cycle distortion, DC feedback from the limiter output is used for offset cancellation.

The output CML buffer completes the receiver chain, delivering the output at pins RXOUT+ and RXOUT-. The output edge rate is dependent on the programmable filter setting. Additionally, the output swing is programmable to satisfy different interface requirements (e.g. CML, AC-coupled LVPECL compatible).

The PHY1076-01 includes a regulator to deliver a controlled voltage to the receiver photodiode cathode at the RSSI pin. The current at RSSI is digitized for use in measuring the received signal strength. This signal can also be used to generate a Loss of Signal (LOS) alarm, with a pre-set hysteresis for assert and de-assert levels. The LOS assert threshold can be adjusted using the LOSS LEVEL DAC.

Alternatively, the LOS alarm can be programmed to detect the amplitude of the AC signal, the Optical Modulation Amplitude (OMA) at the receiver input. The OMA LOS assert threshold can be adjusted using the RX AMP DAC.

4.2.1. Input Stage Configuration

The differential RXIN inputs from the ROSA can be terminated to a common mode voltage. This should be used for all recommended application frequencies of the PHY1076-01, where the inputs are AC coupled. The common mode voltage should be connected by setting **RX_dccouple** = '0' (E8h **rxControl0** bit 3).

4.2.2. Rate Selection

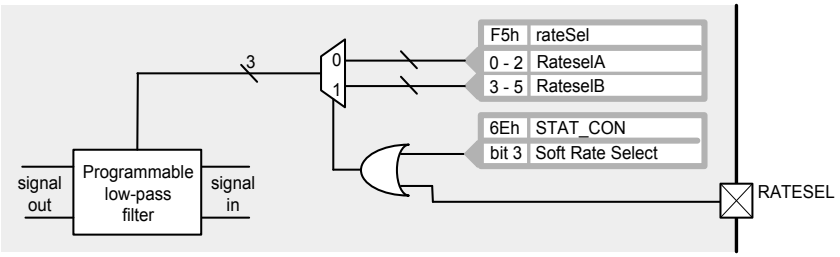

Figure 11 - Low pass filter rate selection

A programmable low pass filter provides band limiting in the received signal path. The filter bandwidth is set to 0.75 x signal data rate for optimum signal to noise performance and is controlled by a 3-bit control word as shown in Table 1.

The rate selection register, **rateSel**, stores two 3-bit codes for controlling the filter; code A in bits 0 to 2, and code B in bits 3 to 5. The selection between the two codes is determined by the RATESEL pin and the **Soft Rate Select** bit as shown in Figure 11. Thus, the RATESEL pin can be used to switch between two pre-selected rates.

The **rateSel** register is unique in that it is directly accessible from the 2-wire serial slave interface. Write accesses are routed to both the register in hardware and the RAM. Read accesses read the **rateSel** value from the hardware. This enables the PHY1076-01 to respond more quickly to updates of this register. This also means that during the intialization sequence, the bandwidth of the receiver can be set up before the **dsfail** alarm is cleared (see Section 5.2.2). This feature does not exist in the 2-wire serial master interface. When loading registers from EEPROM, **rateSel** is loaded via RAM in the same way as all other registers.

Bit			Data Rate
2	1	0	
0	0	0	125/155 Mbps
0	0	1	622 Mbps
0	1	0	1062 Mbps
0	1	1	1250 Mbps
1	0	0	2125 Mbps
1	0	1	2488 Mbps
1	1	0	No Filter
1	1	1	N/A

Table 1 - Signal data rates supported by the low pass filter

4.2.3. CML Output Stage Configuration

The CML output stage has two slew rate settings. For maximum receiver eye opening set **CMLslew** = '0' (E8h **rxControl0** bit 0). To minimize emitted radiation set **CMLslew** = '1'. The slew rates are defined in the table of Parametric Performance characteristics for the Receive limiting amplifier (Section 3.3.1).

The signal swing can also be adjusted. Set **HiLoSwing** = '1' (E9h **rxControl1** bit 1) for higher amplitude differential output swing as defined in the table in section 3.3.1. Set **HiLoSwing** = '0' for lower amplitude output swing.

4.2.4. Loss Of Signal

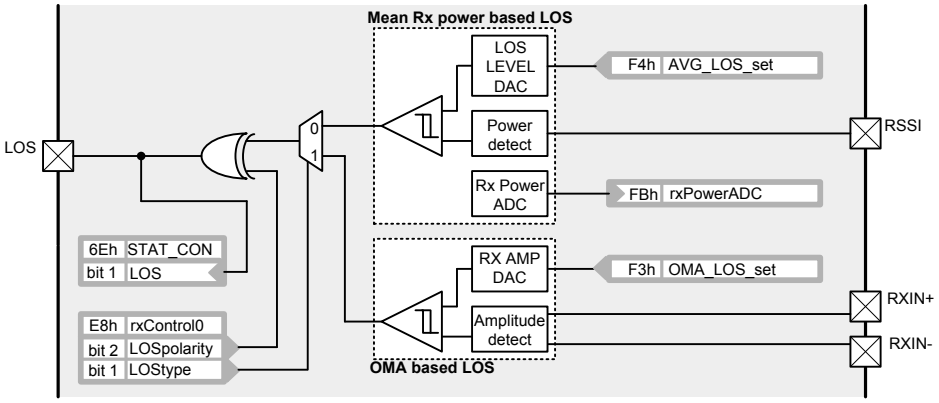

Figure 12 - Control of the LOS pin

Loss of signal (LOS) is determined in one of two ways. If **LOStype** = '1' then the optical modulation amplitude (OMA) method is selected. The signal amplitude measured at RXIN+/- is compared against a threshold level set by the **OMA_LOS_set** register. If the OMA does not exceed the threshold then the LOS pin and consequently the **LOS** bit in **STAT_CON** will be asserted.

If **LOStype** = '0' then the mean received power based method is selected. The signal power detected on the receiver signal strength indicator (RSSI) pin is compared against a threshold level set by **AVG_LOS_set**. If the RSSI does not exceed the threshold then the LOS pin and LOS bit are asserted.

The polarity of the LOS pin is controlled by **LOSpolarity**. If **LOSpolarity** = '0' then LOS is set high during a loss of signal condition. Conversely, if **LOSpolarity** = '1' then LOS is set high when a signal is detected.

Register	DAC	Step Size	Threshold Range
AVG_LOS_set	LOS LEVEL DAC (8 bits)	For Codes 00h – 1Fh Step Size =1.3μA±0.4μA For Codes 1Fh – 7Eh Step Size = 4.6μA±1.0μA	0μA to 31μA 31μA to 411μA
OMA_LOS_set	RX AMP DAC (8 bits)	Use Codes 28h to C8h Step Size = 250μV (nominal DAC range = 0mV to 64mV)	10mV to 50mV

Table 2 - LOS DAC characteristics

For measurement of RSSI, which is used by SFF-8472 Digital Diagnostics Monitoring, the PHY1076-01 can be connected as shown in Figure 13, sourcing the photodiode bias current. This shows a PHY1093 TIA interfacing to the PHY1076-01. The photodiode used is biased using the regulated output of the PHY1076-01, providing a stable and low noise bias for the photodiode. The PHY1076-01 measures the photodiode current and generates a report of received signal strength via an on board A-D converter.

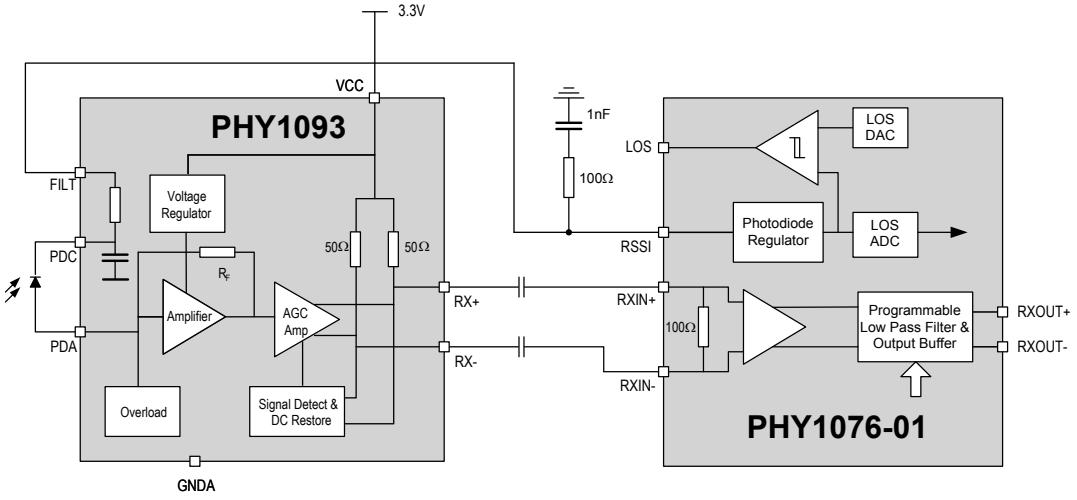

Figure 13 - Connection to TIA for RSSI method of LOS detection

In some cases the TIA may produce an output current which is proportional to the Received Signal Strength. In this case the application circuit shown in Figure 14 should be used. The current I_{RSSI} is mirrored using a dual NPN transistor as shown. This sinks an output current from the PHY1076-01 which can then be measured using the on chip ADC.

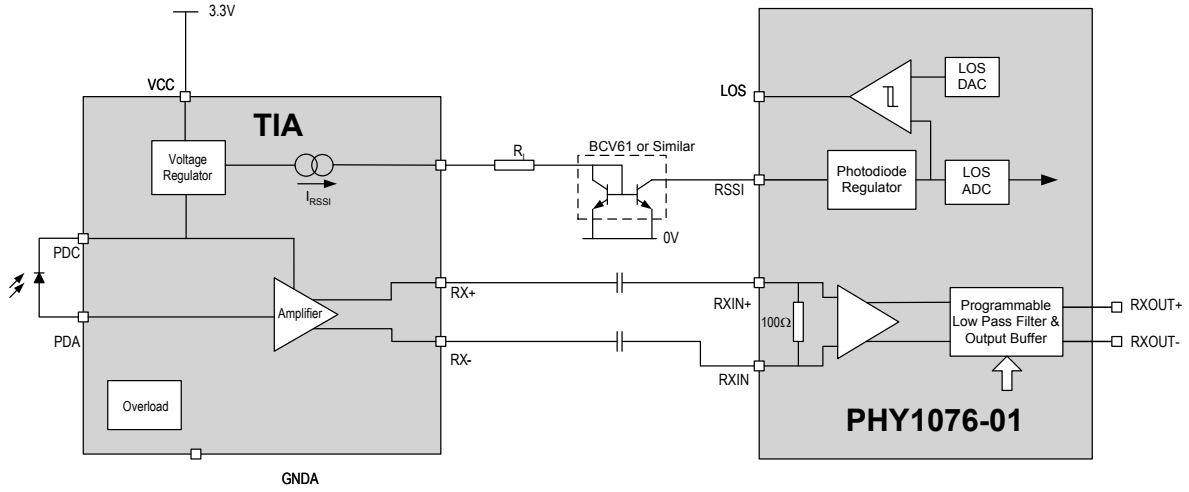

Figure 14 - Connection to TIA with integrated RSSI output

4.3. Transmitter Features

The transmitter input buffer provides the necessary drive to the Laser driver output stage. It is designed to be AC-coupled, with an internal 100Ω differential termination.

The Laser driver output is designed to drive Lasers in common-anode configuration, using either AC or DC coupling. The driver circuit delivers a maximum peak to peak modulation current of 70mA. The maximum current delivered in DC-coupled mode is dependent on the Laser impedance. The voltage swing must remain in the compliance range of the output stage as specified in section 3.4.2.

The PHY1076-01 Laser driver operates with an analog mean-power control loop, which is digitally programmed using the Mean Power DAC. Modulation current is controlled by a Laser modulation DAC with the characteristics shown in Table 3. The modulation DAC has a 375µA/bit resolution which suggests an upper limit of 96mA at full scale, however the modulation output stage is rated to 70mA only for jitter compliance. To satisfy the digital diagnostics requirements, the mean power, as represented by the monitor photocurrent, is measured using the MPD current monitor analogue to digital converter (Tx Power ADC). The bias current ADC (Tx Bias ADC) samples the Laser bias current.

Register	DAC	Step Size	Rated Range
tx_power_set	Mean Power DAC (8 bits)	11µA±1.0µA (Actual DAC range 0µA to 3060µA)	0 to 3mA
modulationDACDefault	Laser modulation DAC[1] (8 bits)	363µA±50µA (Actual DAC range is 0mA to 93mA)	7mA to 70mA

1 Range of modulation current measured at LASER+/- (jitter within spec)

Table 3 - Characteristics of the modulation and bias current DACs

4.3.1. Bias Current Control

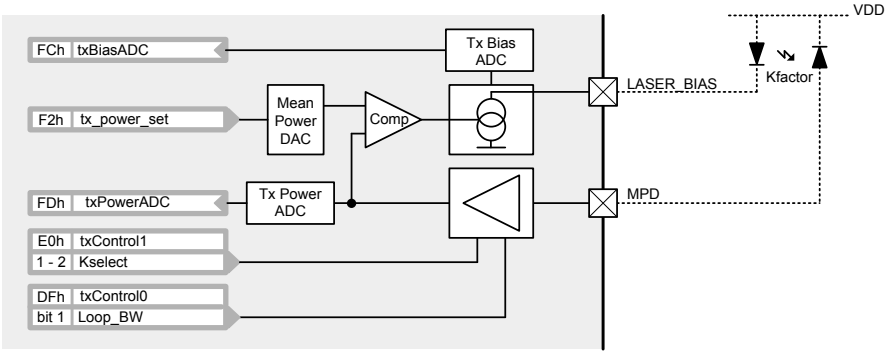

Figure 15 - Control registers affecting the APC loop

The Laser bias current is controlled by the mean-power control loop in which the current from the monitor photodiode in the TOSA is compared with a reference current controlled by **tx_power_set**. Note: the comparator is sensitive to large step changes in the value written to **tx_power_set** (or a small step change at low values). This can cause the safety critical shutdown module to assert a TX_FAULT, as will writing zero to **tx_power_set**.

Loop bandwidth and Kselect are used to optimize APC loop dynamics providing stability of the mean power control and the required transmitter start up time. These settings are affected by the coupling coefficient (Kfactor) between the Laser and monitor photodiode. The **Kselect** bits shown in Table 4 should be used as a guide for the set-up. For example, for a TOSA with Kfactor of 1/100 (Laser bias current = 50mA, monitor diode current = 0.5mA) set **Kselect** = “01”.

Table 4 shows Kselect values that can be chosen to meet the start-up time and APC loop stability requirements:

Coupling coefficient	Kselect value	
	1	**0**
N/A	0	0
1/500 – 1/50	0	1
1/50 – 1/25	1	0
1/25 – 1/8	1	1

Table 4 – Kselect guide for the APC loop

The bandwidth of the control loop response can be controlled with **Loop_BW**. For a critically damped loop, set **Loop_BW** to '0'. For a more rapid response, set **Loop_BW** to '1'. The frequency response of the loop is detailed in section 3.4.3 Laser Mean Power Control Loop.

4.3.2. Modulation Current Control

The modulation current can be controlled in two ways:

Set **ModLUTdisab** (DFh **txControl0** bit5) to '1' to directly access the modulation DAC. Then, adjust modulation current by writing to **modulationDACDefault** (D5h).

Set **ModLUTdisab** to '0' to enable the modulation current vs. temperature look-up table (LUT) in the PHY1076-01. The 45 byte LUT is indexed by the value in **temperatureADC** (FEh), where Index is given by:

Index = (**temperatureADC** x 45) / 255

and the index rounds down to the lower temperature. When the LUT is switched from the enabled to disabled state, the last control value from the LUT will persist. On disabling the LUT the modulation DAC will not revert back to a value previously written to **modulationDACDefault**. A new value must be explicitly written to **modulationDACDefault** once the LUT has been disabled.

On power up the modulation DAC will not be programmed with the value uploaded from the EEPROM and will default to taking the value from the LUT for the measured temperature.

4.3.3. Laser Driver Setup

There is a trimming network on the output driver which adjusts the time constant for output damping on LASER ± . It is controlled by the value in **txDriverCap** (F6h) which is used to set the value of the time constant as shown in Table 5 based on the number of RC networks turned on. Set **txDriverCap** to '00' for no damping and fastest edges. It is possible to enable combinations by programming **txDriverCap** with values that set more than one bit high. e.g. **txDriverCap** = 07h enables RxC/2 + RxC + Rx2C.

txDriverCap	Time constant (RC=34ps)
Bit 0	RxC/2
Bit 1	RxC
Bit 2	Rx2C
Bit 3	Rx3C
Bit 4	Rx4C
Bits 5 to 7	Not used

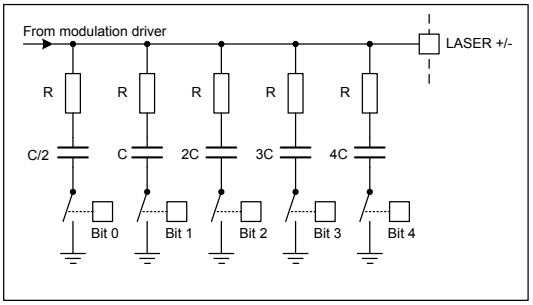

Table 5 -Time constant selection for the Tx output damping network.

4.4. Laser Safety Features

The Laser safety circuitry monitors the device for potential faults. If a fault is detected, the safety logic turns off the transmitter bias and modulation currents and indicates the fault condition at pin TX_FAULT.

The Laser output driver can be disabled in one of four ways:

1. The TX_DISABLE pin is taken high.
2. The internal safety critical shutdown circuitry detects a fault with
    a. the APC loop or bias current
    b. power supply 2.7V>VDD or VDD>3.9V
    c. RREF shorted to Ground, VDD or open circuit
3. The **Soft Tx Disable** bit in **STAT_CON** is asserted
4. The watchdog timer times out, indicating that communication with the host/MCU has been interrupted.

In all cases the modulation current and the current to the LASER_BIAS pin will be disabled, and the SHUTDOWN pin will be asserted. The purpose of the SHUTDOWN pin is to provide a means by which the Laser can be isolated from VDD (common anode configuration) when an electrical fault is detected. In cases 2 and 4, TX_FAULT will also be set.

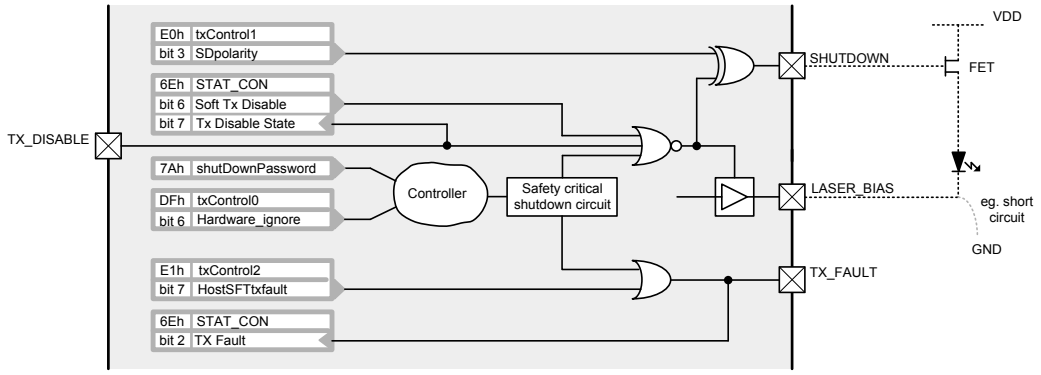

Figure 16 - TX_FAULT and SHUTDOWN pin control logic

4.4.1. PHY1076-01 Fault Management

The safety critical shutdown circuit will shutdown and isolate the Laser if it senses a fault with the bias current, the supply voltage or the reference voltage.

For example, consider a Laser arranged in common anode configuration. The Laser cathode connects to the LASER_BIAS pin and the anode connects to VDD. If a short circuit to Ground occurs on the route between the cathode and LASER_BIAS then the safety critical shutdown circuit will switch off the bias current. However, this will not protect the Laser as a current path from VDD to ground still exists. A FET device can provide the required isolation when switched off by the SHUTDOWN pin as shown in Figure 16. The SHUTDOWN pin is controlled by the same signal which switches off the bias current. The SHUTDOWN pin output response to faults and polarity setting is shown in Table 6.

The safety critical shutdown circuit can be disabled in software by setting **Hardware_ignore** = '1', and entering the value 42h to the **shutDownPassword** register. In this case the Laser will not be disabled when a fault is detected; however, a TX_FAULT will still be reported. **This feature should be used with great caution as the eye safety features of the device will be disabled.** The PHY1076-01 will respond to TX_DISABLE being set even if **Hardware_ignore** is set.

Power supply and RREF faults result in the TX_FAULT latching and the laser being disabled momentarily. Once the fault condition is removed the laser will be reactivated, however the TX_FAULT output must be cleared by toggling TX_DISABLE (or **Soft Tx Disable**). An APC loop fault results in the TX_FAULT latching and the laser being disabled. TX_DISABLE (or **Soft Tx Disable**) must be pulsed high as shown in Figure 5 to remove this latching condition and reactivate the laser. When the Laser is turned on, during

power up or after a fault, there will be a short period during which the bias control loop is allowed to settle (t_settle, see Section 3.4.3) before the safety control loop circuit is enabled.

Fault Status	SDpolarity (TxControl2, Bit 3)	SHUTDOWN Pin Voltage
No Fault	0	High
	1	Low
Fault	0	Low
	1	High

Table 6 – Shutdown Output Voltage under Fault/No Fault conditions

4.4.2. MCU and Host Fault Management

The MCU is responsible for maintaining and reporting alarms and warnings in accordance with the SFF-8472 specification. When an alarm is triggered, the MCU must set **HostSFTtxfault** = '1'. This will cause the PHY1076-01 to report a fault on the TX_FAULT pin and in the **STAT_CON** register. The PHY1076-01 will not disable the Laser at this point. The MCU or the host could disable the Laser when a **TX Fault** is detected in **STAT_CON** by asserting **Soft Tx Disable**.

4.4.3. Watchdog

A watchdog is implemented by the PHY1076-01 to monitor the activity of the attached MCU in digital diagnostics mode. When **WatchdogEn** (E1h **txControl2** bit0) is set to '1', the PHY1076-01's watchdog feature is enabled. The MCU is required to increment the **Watchdog[0:5]** counter (E1h **txControl2**) at least every 100ms. If no change is detected in the counter, the PHY1076-01 will disable the Laser and will assert TX_FAULT. The Laser will be re-enabled, and TX_FAULT de-asserted when either the watchdog counter is incremented, or the watchdog feature is disabled by writing '0' to **WatchdogEn**. On power up the watchdog feature is disabled.

4.5. Tsense Temperature Sensor

The temperature is determined by measuring the ΔV_{BE} across an external transistor connected to the TSENSE pin. The transistor can be any standard npn silicon transistor with a beta > 100 connected in diode mode (base and collector tied together). It is recommended to use a BC847B or similar.

Calibration and averaging of the temperature sensor readings using an external microcontroller are required to optimize the accuracy. Once optimized, the PHY1076-01 can report temperature to SFF8472 requirements over the recommended operating conditions.

The temperature sensor operating range and corresponding TSENSE input levels are shown in Table 7.

	Symbol	Unit	Minimum	Maximum
Temperature	t	°C	-70	+115
TSENSE delta input voltage	ΔV_{BE}	mV	50	100

Table 7 – Temperature sensor operating range

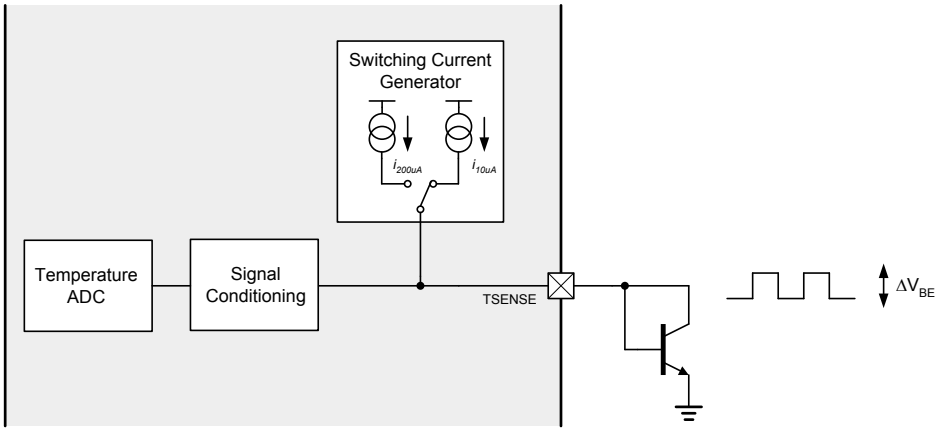

Figure 17 – Temperature sensor functional block diagram

5. Control Interface

The PHY1076-01 can be operated in one of two modes as dictated by the design of the module. The PHY1076-01 will identify the mode by attempting to read from its 2-wire serial EEPROM interface (See section 5.4) on power up. If no EEPROM is present then diagnostic mode is inferred.

In digital diagnostics mode, the Micro Controller Unit (MCU) and EEPROM (Address A0h) present an SFF-8472 compliant interface to the host. The MCU provides read/write access to all registers in the A2h registers map, calculates digital diagnostics monitor values and maintains alarms and warnings. The MCU must initialize the PHY1076-01 control registers from EEPROM, relay control information to the PHY1076-01, and fetch status information in real time.

In stand-alone mode, the PHY1076-01 is initialized directly from an external 4 kbit (8 x 512 bit) Serial EEPROM. Serial ID information as specified in the SFP MSA is accessible via the 2-wire serial interface. This mode supports temperature compensation of modulation current using a look-up table stored in EEPROM.

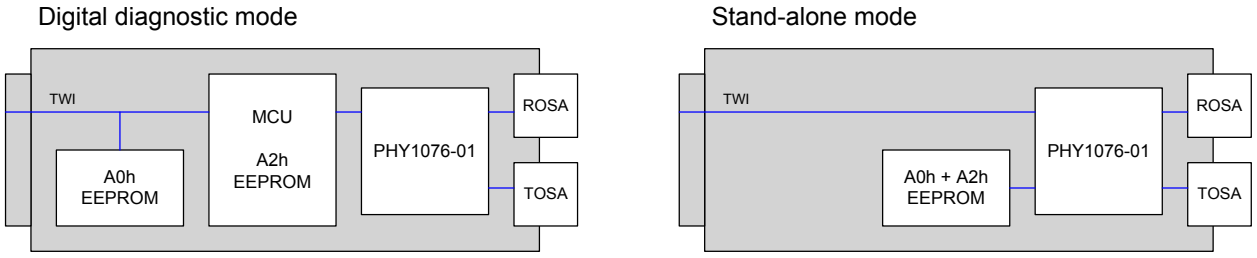

Figure 18 - Optical transceiver module configurations

5.1. Memory Map

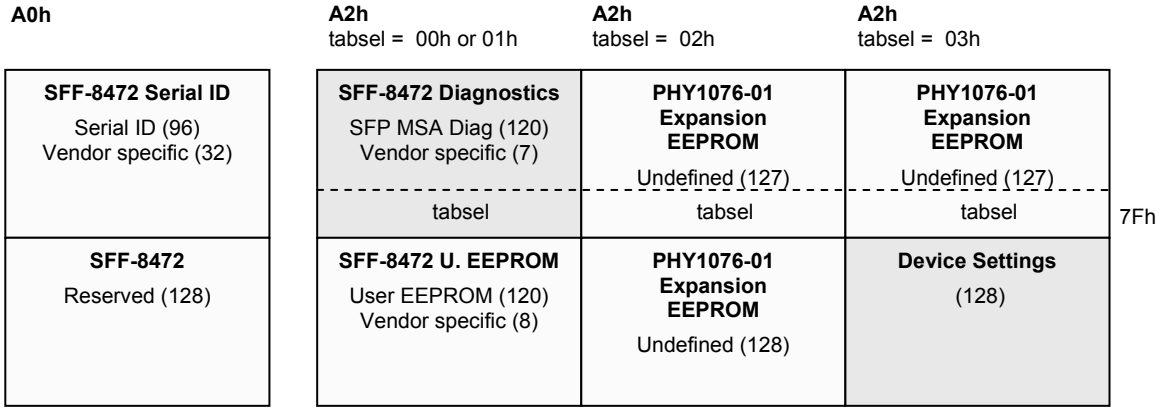

Figure 19 - Memory map for a 2G SFP or SFF transceiver module containing a PHY1076-01 device

Figure 19 shows the memory map of a module containing a PHY1076-01. An 8 kbit memory space is a natural step up from the minimum 4 kbit memory space required for SFF-8472 compliance, providing additional space in which to map the Device Settings registers of the PHY1076-01.

The internal RAM of the PHY1076-01 implements the SFF-8472 Diagnostics table and the Device Settings table. Selection between tables is achieved using the **tableSelect** (tabsel) register located at address offset 7Fh. To access the Diagnostics table, first write 00h to tabsel. To access the Device Settings table, first write 03h to tabsel.

Tabsel is effectively write-only because to write to tabsel has the effect of switching to a different register table. Thus, reading tabsel will not yield the value which was previously written.

5.2. Operation

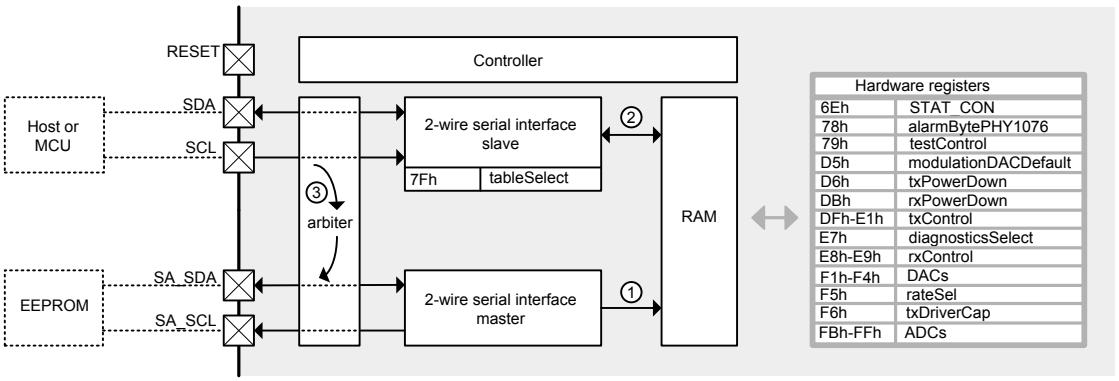

Figure 20 - Serial interfaces to RAM and the on-chip controller

5.2.1. Data Transfer Mechanisms

Three distinct data paths are identified in Figure 20.

When the PHY1076-01 comes out of reset, the 2-wire serial slave interface is disabled. Only path 1 is active. The controller instructs the 2-wire serial master interface to attempt to transfer A2h register tables (SFF-8472 diagnostics and device settings) from the external EEPROM to RAM. If this is successful then the PHY1076-01 will operate in stand-alone mode. If the transfer fails, then the **dsfail** and **eerxfail** alarm bits in the **alarmBytePHY1076** (78h) register will be set and the PHY1076-01 will operate in diagnostics mode. Regardless of the outcome, when the EEPROM read process is complete the controller enables the 2-wire serial slave interface. The 2-wire serial master interface is then no longer used.

The 2-wire serial slave interface has slave address A2h. In diagnostics mode, the host or external MCU uses the 2-wire serial slave interface to write to or read from copies of the device settings held in RAM. When the boot sequence is complete, the controller transfers data between the RAM and the actual registers implemented in hardware periodically every 10ms.

In stand-alone mode the RAM space is not used once the boot sequence is complete. Reading from A2h will return zero.

Path 3 is a special case which supports modules designed for stand-alone mode, enabling them to be set up or re-configured via the 2-wire serial interface slave. The PHY1076-01 can be forced into diagnostic mode if the data integrity numbers in the EEPROM are deliberately erased (see section 5.4.2). This enables the host/MCU to access both the RAM (path 2) and the EEPROM (path 3). All accesses to the A0h address space are directed to the EEPROM only. Accesses to the A2h address space are examined as they arrive by the 2-wire serial slave module, which in turn instructs the arbitration logic. The destination for the transaction depends on the value of tabsel and the register address as shown in Table 8.

Access type	tabsel	Address range[1]	Destination memory
read	00	lower	RAM
read	03	upper	RAM
write	00	lower	RAM + EEPROM
write	00	upper	EEPROM
write	03	upper	RAM

1 Addresses 00h to 7Fh = lower. Addresses 80h to FFh = upper.

Table 8 - Destination of 2-wire serial interface transactions as a function of write protection, tabsel and address.

5.2.2. Device Initialisation Sequence

The Initialisation Sequence is illustrated in Figure 21. The **Data_Ready_Bar** bit in the **STAT_CON** register indicates when data from the ADCs may be read after power up. It is first set to '1' before the 2-wire serial slave interface is enabled to indicate that the PHY1076-01 is not ready. Once initialisation is complete and the ADC data is ready **Data_Ready_Bar** is cleared to '0'. This event can be used by the external host/MCU as a signal that the PHY1076-01 is ready for device settings to be uploaded from the MCU to the PHY1076-01 RAM. The PHY1076-01 will not enter the main diagnostic function loop until the upload is complete. This is initiated by the host/MCU clearing the **dsfail** and **eerxfail** bits in the **alarmBytePHY1076** (78h) register. When **dsfail** is cleared and the main loop is executed the contents of RAM will be transferred into the hardware registers of the PHY1076-01.

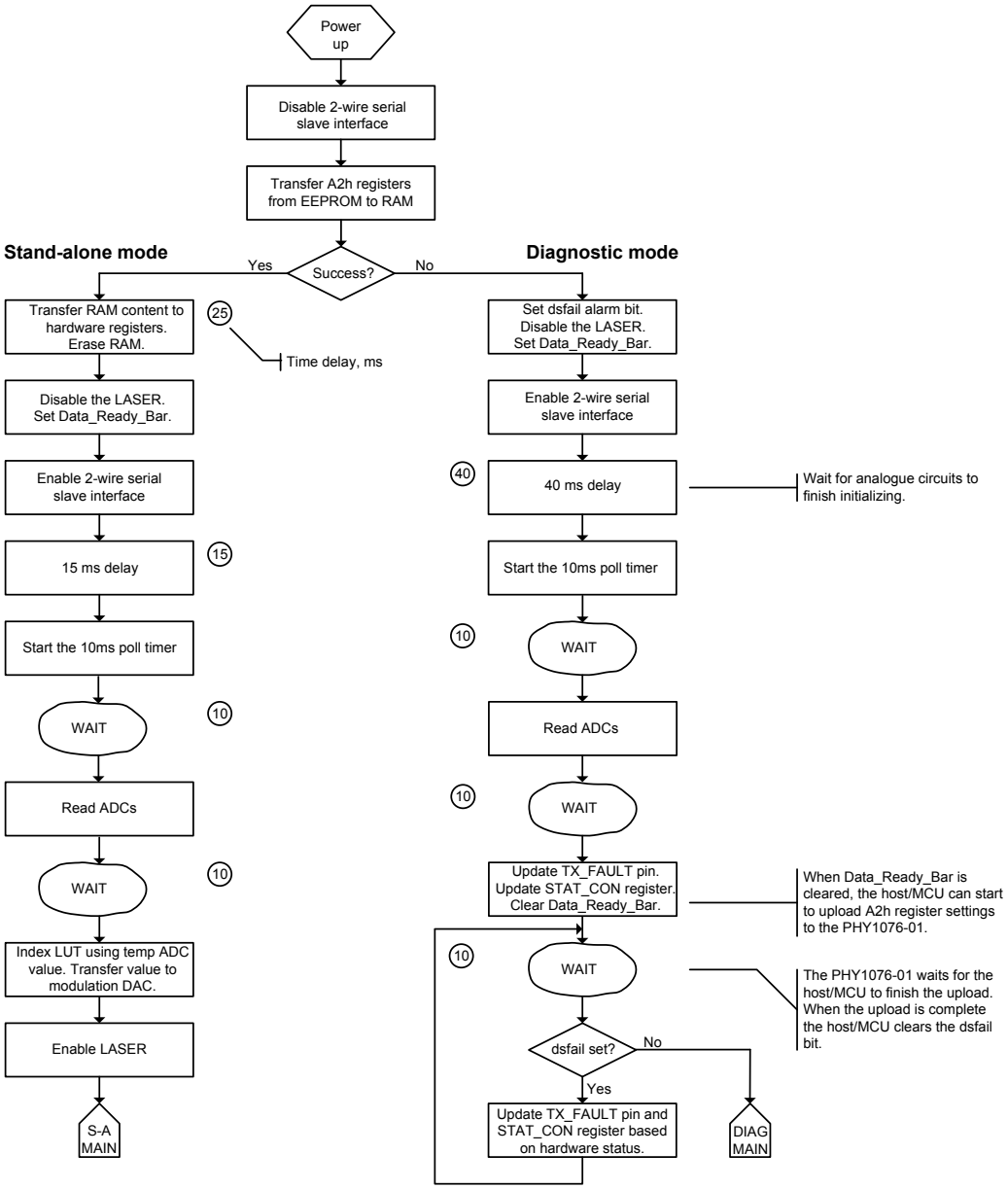

Figure 21 - PHY1076-01 initialisation sequence. Time delays for key stages are shown in ms.