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Cool-Power®
ZVS Switching Regulators
PI352x-00

30 – 60V_{IN} Cool-Power ZVS Buck Regulator

Product Description

The PI352x-00 is a family of high input voltage, wide input range DC-DC ZVS Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP).

The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI352x-00 series, increases point of load performance providing best in class power efficiency. The PI352x-00 requires only an external inductor, two voltage selection resistors and minimal capacitors to form a complete DC-DC switch mode buck regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3523-00-LGIZ	3.3V	2.2 – 4V	22A
PI3525-00-LGIZ	5.0V	4.0 – 6.5V	20A
PI3526-00-LGIZ	12V	6.5 – 14V	18A

Features & Benefits

- High Efficiency HV ZVS Buck Topology
- Wide input voltage range of 30 – 60V
- Power-up into pre-biased load ≤ 6.0V
- Parallel capable with single wire current sharing
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft start & tracking
- –40 to 120°C operating range (T_{INT})

Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Equipment

Package Information

- 10 x 14 x 2.6mm LGA SiP

Contents

Order Information

Product	Nominal Output	Rated I_{OUT}	Package	Transport Media
PI3523-00-LGIZ	3.3V	22A	10 x 14mm LGA	TRAY
PI3525-00-LGIZ	5.0V	20A	10 x 14mm LGA	TRAY
PI3526-00-LGIZ	12V	18A	10 x 14mm LGA	TRAY

Thermal, Storage and Handling Information

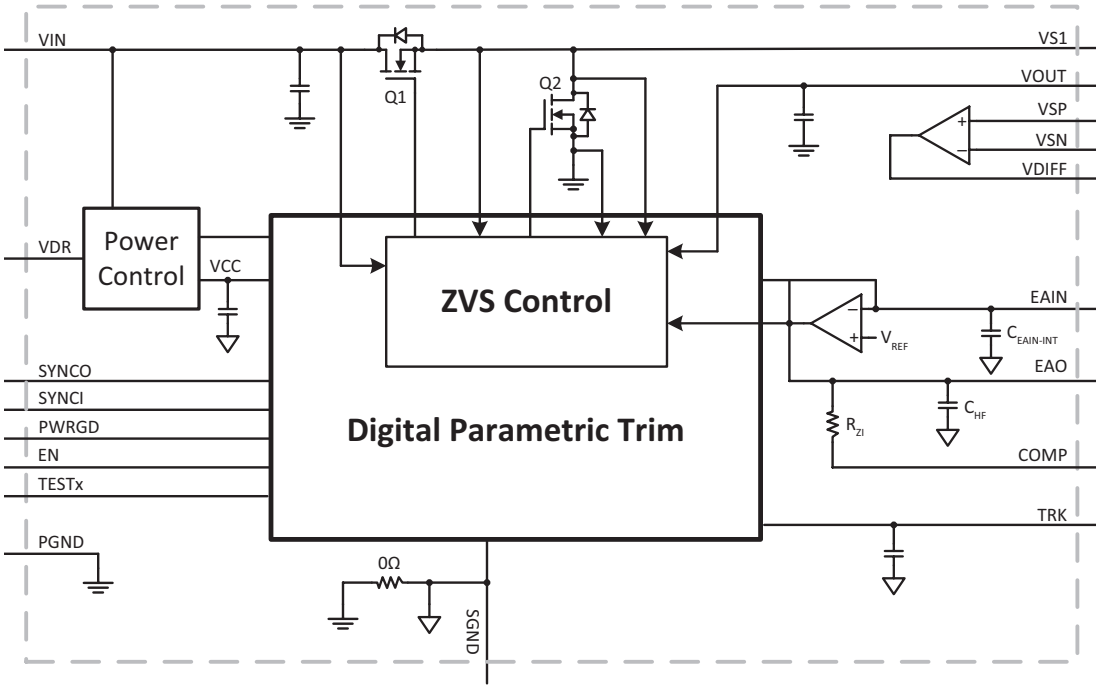
Name	Rating
Storage Temperature	–65 to 150°C
Internal Operating Temperature	–40 to 120°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3
ESD Rating, JESD22-A114F, JS-002-2014	2kV HBM; 1kV CDM, respectively

Absolute Maximum Ratings

Name	Rating
V_{IN}	–0.7 to 75V
VS1	$-0.7V_{DC}$ to 75V
V_{OUT}	–0.5 to 25V
SGND	±100mA
TRK	–0.3 to 5.5V, ±30mA
VDR, SYNCI, SYNCO, PWRGD, EN, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx	–0.3 to 5.5V, ±5mA

Notes: Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltages are referenced to PGND unless otherwise noted.

Functional Block Diagram

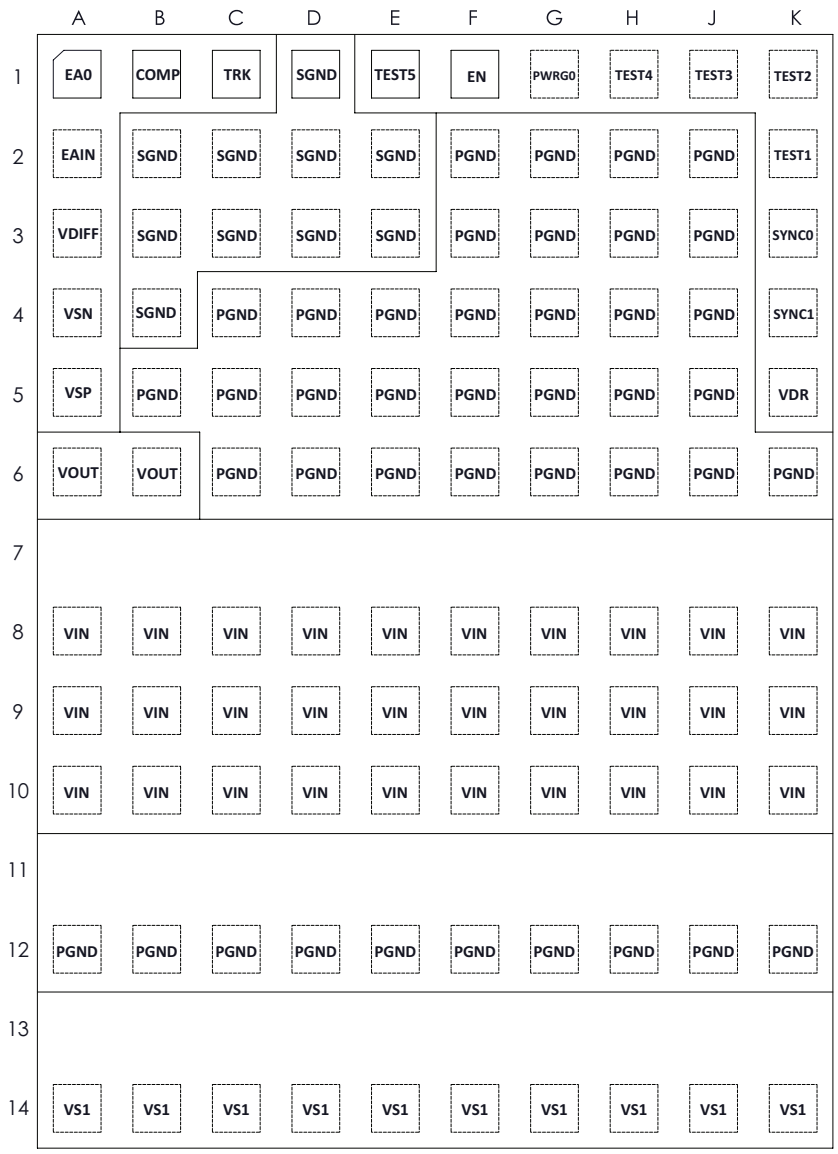


Simplified Block Diagram

Pin Description

Name	Location	I/O	Description
VS1	Block 1	Power	**Switching Node:** and ZVS sense for power switches.
VIN	Block 3	Power	**Input Voltage:** and sense for UVLO, OVLO and feed forward ramp.
VDR	5K	I/O	**Gate Driver VCC:** Internally generated 5.1V. May be used as a bias supply for low power external loads. See Application Description for important considerations.
SYNCI	4K	I	**Synchronization Input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use. The PI352x-00 family is not optimized for external synchronization functionality. Refer to Application Description of Parallel Operation for details.
SYNCO	3K	O	**Synchronization Output:** Outputs a high signal at the start of each clock cycle for the longer of ½ of the minimum period or the on time of the high side power MOSFET.
TEST1	2K	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST2	1K	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST3	1J	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST4	1H	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
TEST5	1E	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
PWRGD	1G	O	**Power Good:** High impedance when regulator is operating and V_{OUT} is in regulation. Otherwise pulls to SGND.
EN	1F	I/O	**Enable Input:** Regulator enable control. When asserted active or left floating: regulator is enabled. Otherwise regulator is disabled.
SGND	Block 5		**Signal Ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO communication returns. SGND and PGND are star connected within the regulator package.
TRK	1C	I	**Soft-Start and Track Input:** An external capacitor may be connected between TRK pin and SGND to increase the rise time of the internal reference during soft start.
COMP	1B	O	**Compensation Capacitor:** Connect capacitor for control loop dominant pole. See Error Amplifier section for details. A default C_{COMP} of 4.7nF is used in the example.
EAO	1A	O	**Error amp output:** External connection for additional compensation and current sharing.
EAIN	2A	I	**Error Amp Inverting Input:** Connection for the main V_{OUT} feedback divider tap.
VDIFF	3A	O	**Independent Amplifier Output:** Active only when module is enabled.
VSN	4A	I	**Independent Amplifier Inverting Input:** If unused connect in unity gain.
VSP	5A	I	**Independent Amplifier Non-Inverting Input:** If unused connect to SGND.
VOUT	6A,B	Power	**Direct V_{OUT} Connect:** for per-cycle internal clamp node and feed-forward ramp.
PGND	Block2	Power	**Power Ground:** V_{IN} and V_{OUT} power returns.

Package Pinout



PI332x & PI352x

TOP THROUGH VIEW OF PRODUCT

Pin Block Name	Group of pins
VIN	A8-10, B8-10, C8-10, D8-10, E8-10, F8-10, G8-10, H8-10, J8-10, K8-10
VS1	A14, B14, C14, D14, E14, F14, G14, H14, J14, K14
PGND	A12, B12, C12, D12, E12, F12, G12, H12, J12, K12
PGND	B5, C4-6, D4-6, E4-6, F2-6, G2-6, H2-6, J2-6, K6
VOUT	A6, B6
SGND	B2-4, C2-3, D1-3, E2-3

PI352x-00 Common Electrical Characteristics

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Amp						
Open Loop Gain			96	120	140	dB
Small Signal Gain-bandwidth			5	7	12	MHz
Input Offset				0.5	1	mV
Common Mode Input Range			–0.1		2.5	V
Differential Mode Input Range					2	V
Input Bias Current			–1		1	µA
Output Current			–1		1	mA
Maximum V_{OUT}		I_{VDIFF} = –1mA	4.85			V
Minimum V_{OUT}		I_{VDIFF} = –1mA			20	mV
Capacitive Load Range for Stability			0		50	pF
Slew Rate				11		V/µs
PWRGD						
V_{OUT} Rising Threshold	$V_{PG\_HI\%}$		78	84	90	% V_{OUT_DC}
V_{OUT} Falling Threshold	$V_{PG\_LO\%}$		75	81	87	% V_{OUT_DC}
PWRGD Output Low	V_{PG_SAT}	Sink = 4mA			0.4	V
VDR						
Voltage Set Point	V_{VDR}	V_{IN_DC} > 10V	4.9	5.05	5.2	V
External Loading	I_{VDR}	See Application Description for details	0		2	mA
Enable						
High Threshold	V_{EN_HI}		0.9	1.0	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Pull-Up Voltage Level for Source Current	V_{EN_PU}			2		V
Pull-Up Current	$I_{EN\_PU\_POS}$	V_{IN} > 8V, excluding t_{FR_DLY}		50		µA
Reliability						
MTBF		MIL-HDBK-217, 25°C, Ground Benign: GB		12.6		MHrs
		Telcordia SR-332, 25°C, Ground Benign: GB		96.9		MHrs

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.

PI3523-00 ($3.3V_{OUT}$) Electrical Characteristics

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, I_{OUT} = 22A		1.69		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		4.7		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75	1.2	mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		1.8		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Input capacitance, Internal	C_{IN_INT}	Effective value V_{IN} = 48V, 25°C		0.50		µF
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	2.2	3.3	4.0	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 2A < I_{OUT} < 22A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 20A, C_{OUT} = 8 x 100µF, 20MHz BW [d]		76		mVp-p
Output Current	I_{OUT_DC}	[e]	0		22	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 230nH inductor.		25.3		A
Maximum Array Size	$N_{PARALLEL}$	[b]			3	Modules
Output Current, array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [b] see applications section for details	0		[g]	A
Output Current, array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [b] see applications section for details	0		[g]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27.0	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO}		62	64.3		V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY}	0.90	1.17	1.60	V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		4.5	5.2		V

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.
[g] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3523-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[f] While in Discontinuous Conduction Mode (DCM) only, SYNCI grounded	470	500	530	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	–50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [c] [f]	250		550	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EAIN_OV}		50	80	110	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, Internal	C_{TRK_INT}			47		nF
Soft-Start Time	t_{SS}	C_{TRK_EXT} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		5.1		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.6		V
EAIN Capacitance, Internal	C_{EAIN_INT}			56		pF
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		6		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.
[g] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3523-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

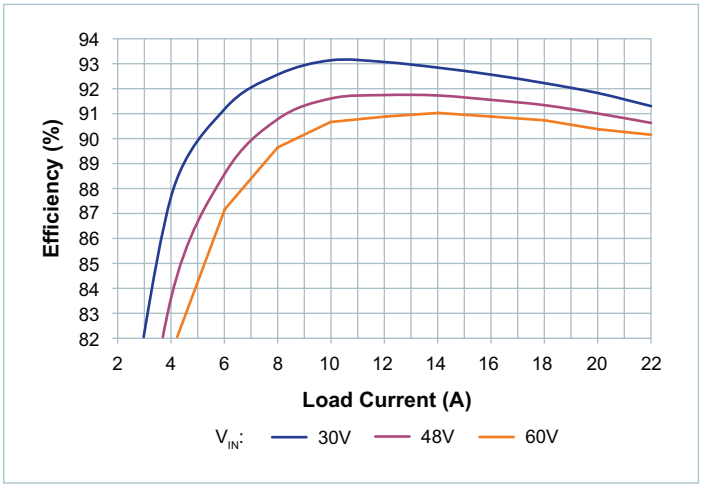


Figure 1 — *System Efficiency, Nominal Trim, Board Temperature = 25°C*

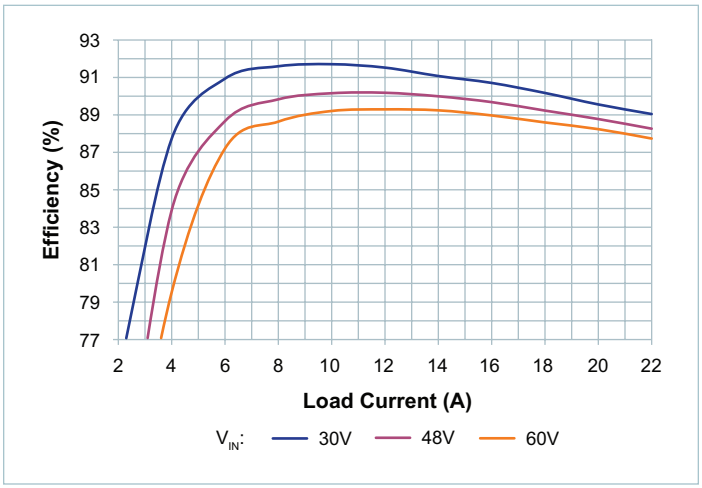


Figure 2 — *System Efficiency, Low Trim, Board Temperature = 25°C*

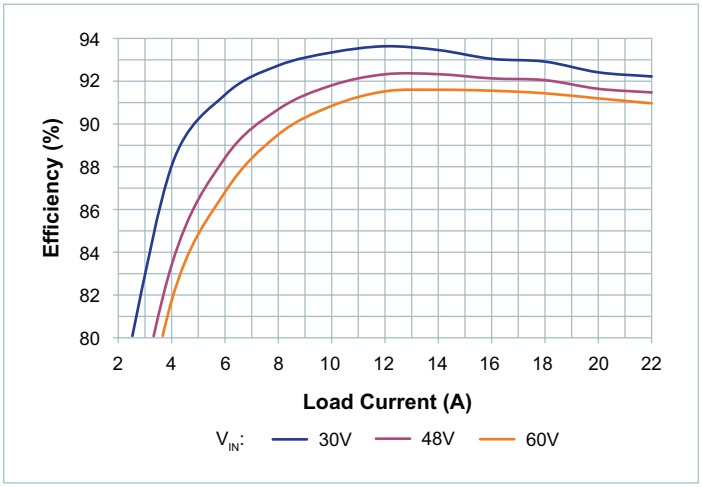


Figure 3 — *System Efficiency, High Trim, Board Temperature = 25°C*

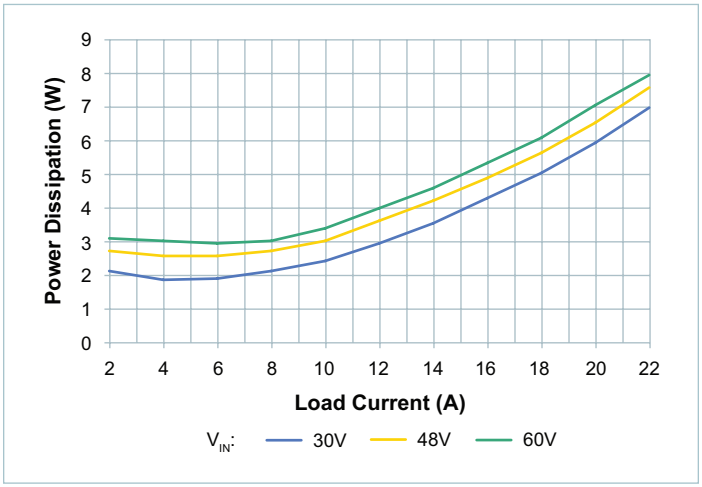


Figure 4 — *System Power Dissipation, Nominal Trim, Board Temperature = 25°C*

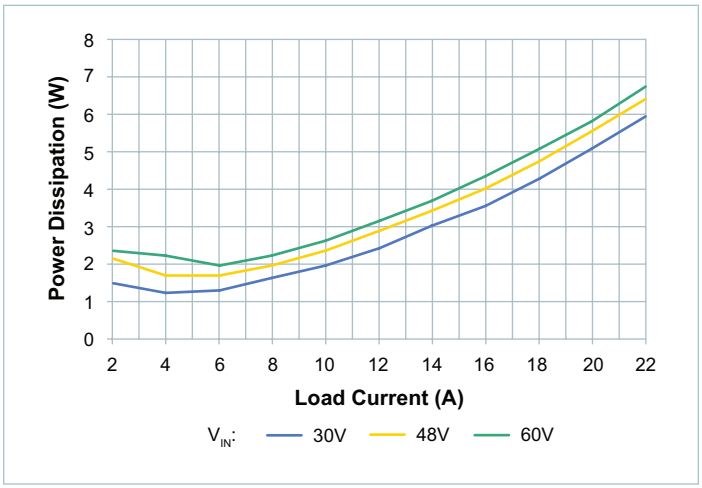


Figure 5 — *System Power Dissipation, Low Trim, Board Temperature = 25°C*

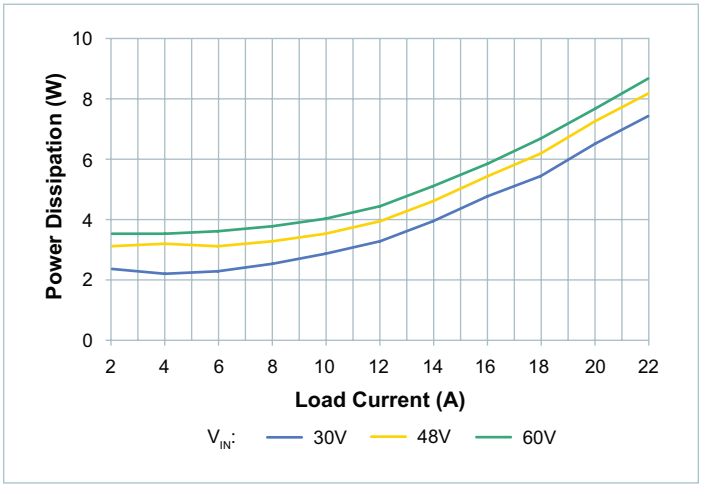


Figure 6 — *System Power Dissipation, High Trim, Board Temperature = 25°C*

PI3523-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

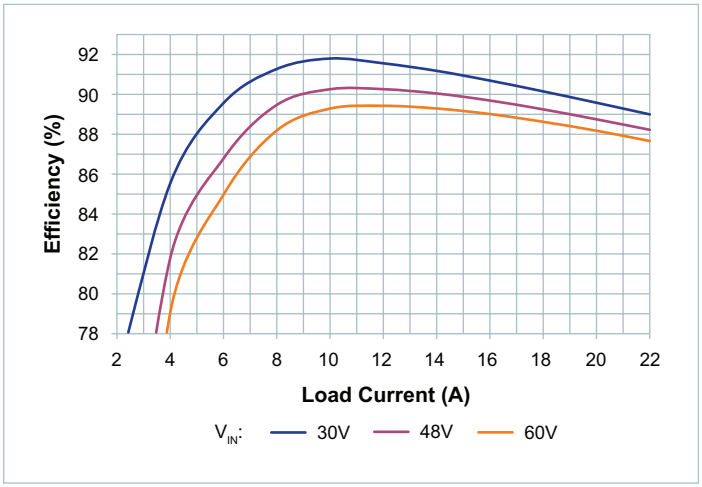


Figure 7 — *System Efficiency, Nominal Trim, Board Temperature = 100°C*

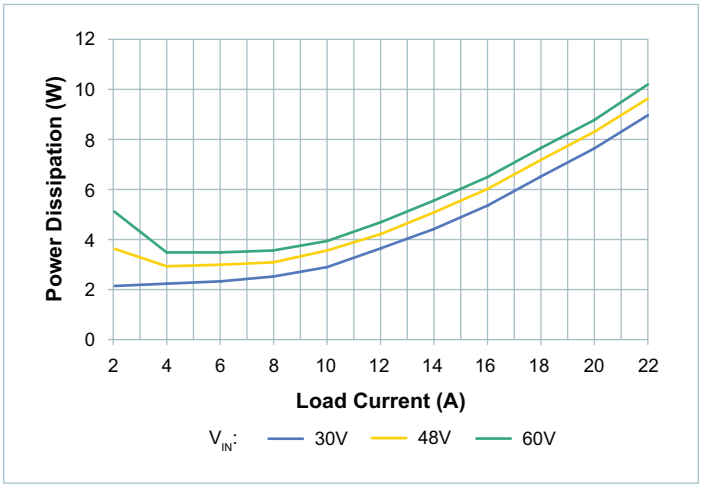


Figure 10 — *System Power Dissipation, Nominal Trim, Board Temperature = 100°C*

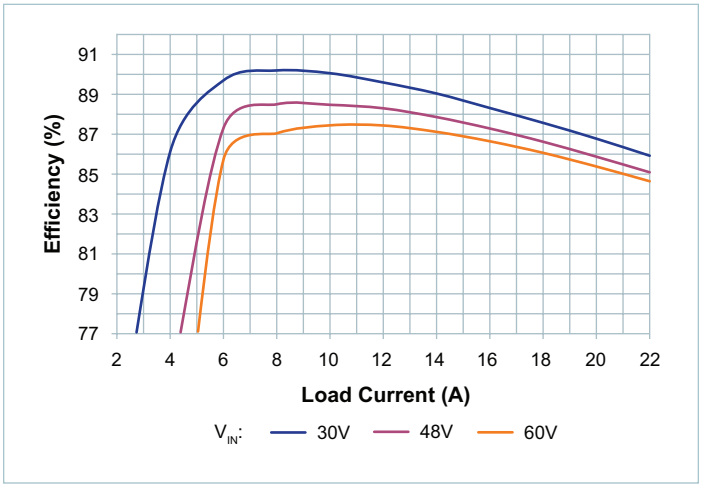


Figure 8 — *System Efficiency, Low Trim, Board Temperature = 100°C*

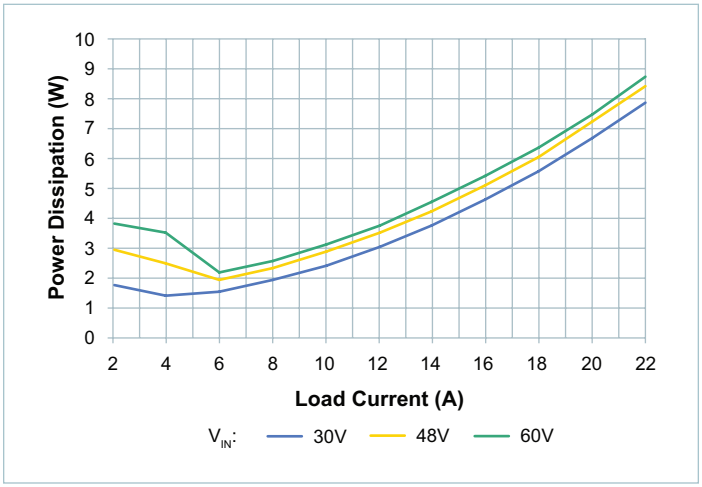


Figure 11 — *System Power Dissipation, Low Trim, Board Temperature = 100°C*

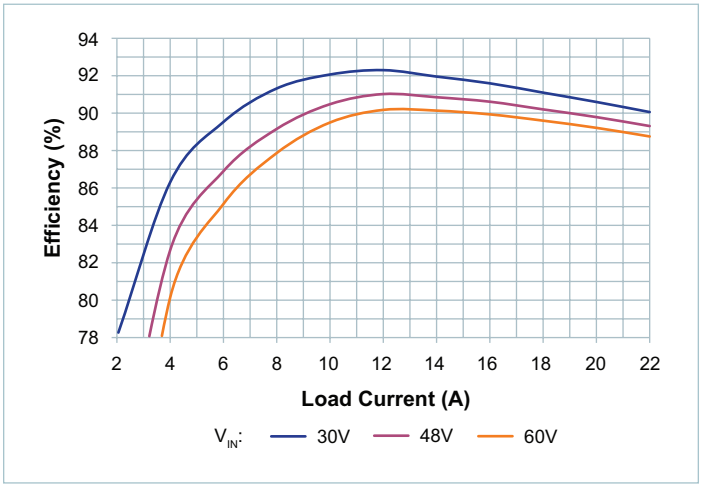


Figure 9 — *System Efficiency, High Trim, Board Temperature = 100°C*

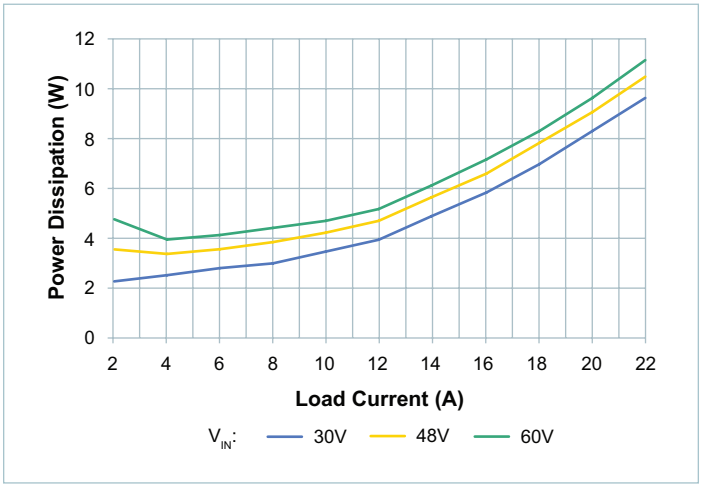


Figure 12 — *System Power Dissipation, High Trim, Board Temperature = 100°C*

PI3523-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

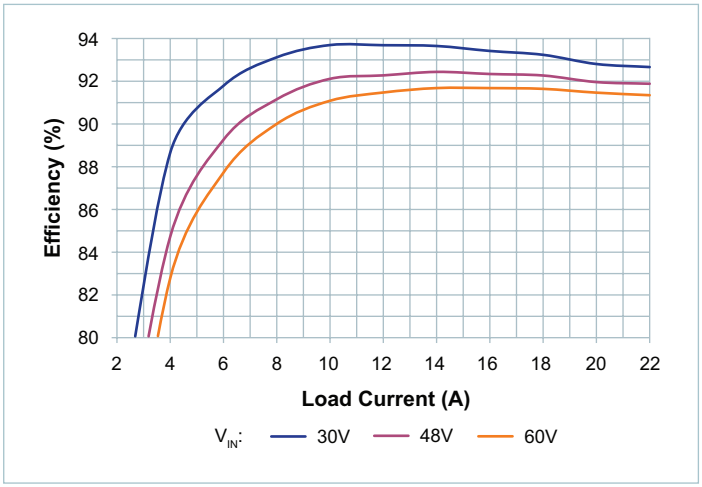


Figure 13 — *System Efficiency, Nominal Trim, Board Temperature = –40°C*

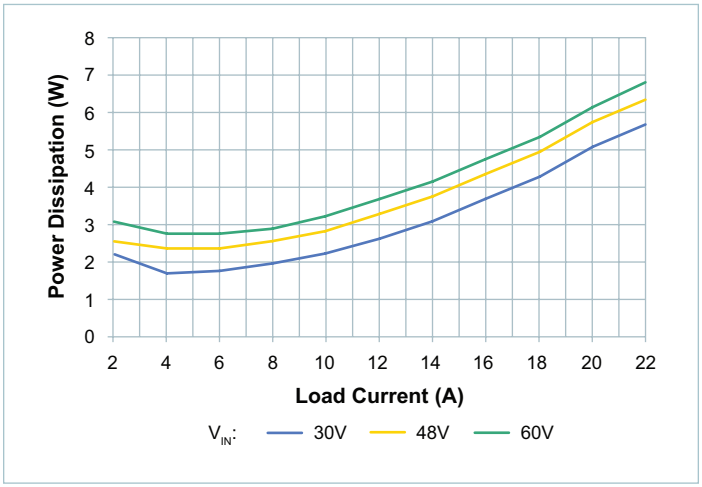


Figure 16 — *System Power Dissipation, Nominal Trim, Board Temperature = –40°C*

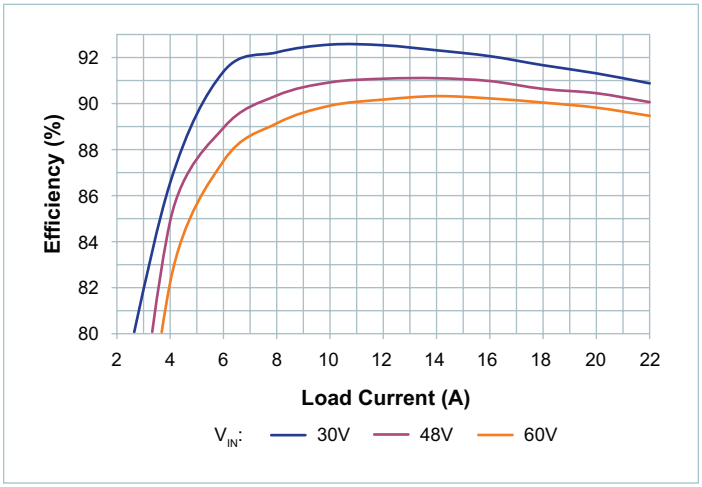


Figure 14 — *System Efficiency, Low Trim, Board Temperature = –40°C*

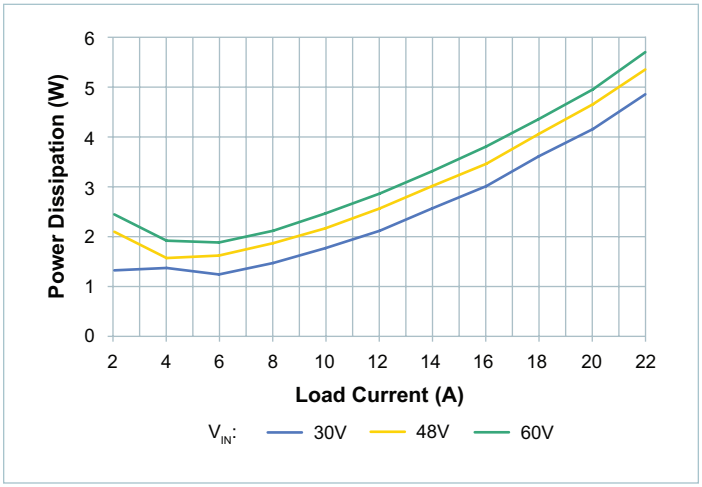


Figure 17 — *System Power Dissipation, Low Trim, Board Temperature = –40°C*

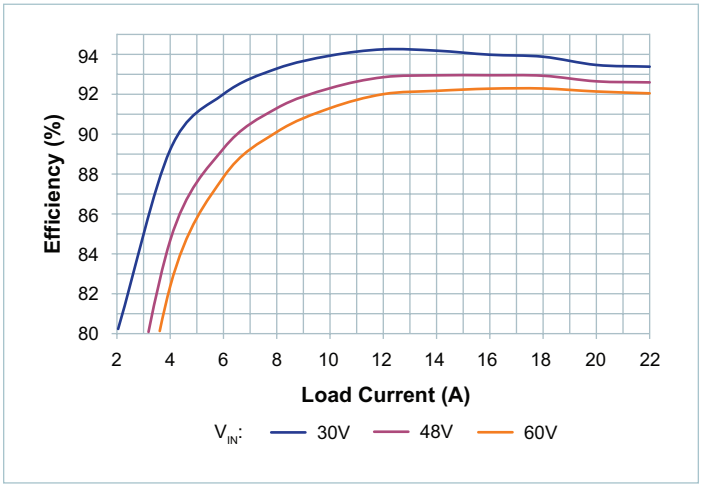


Figure 15 — *System Efficiency, High Trim, Board Temperature = –40°C*

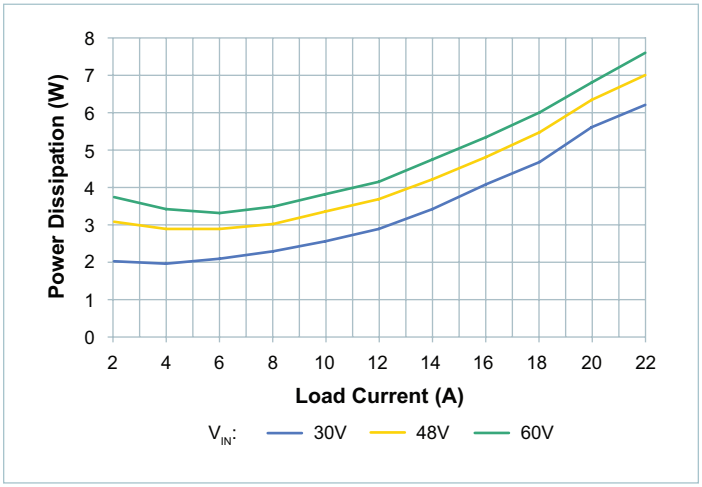


Figure 18 — *System Power Dissipation, High Trim, Board Temperature = –40°C*

PI3523-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

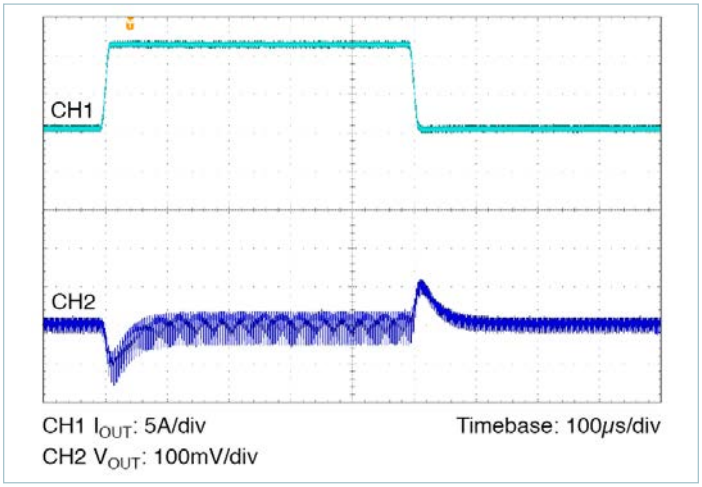


Figure 19 — *Transient Response: 50% to 100% load, at 1A/µs. Nominal Line, Nominal Trim, C_{OUT} = 8 x 100µF Ceramic*

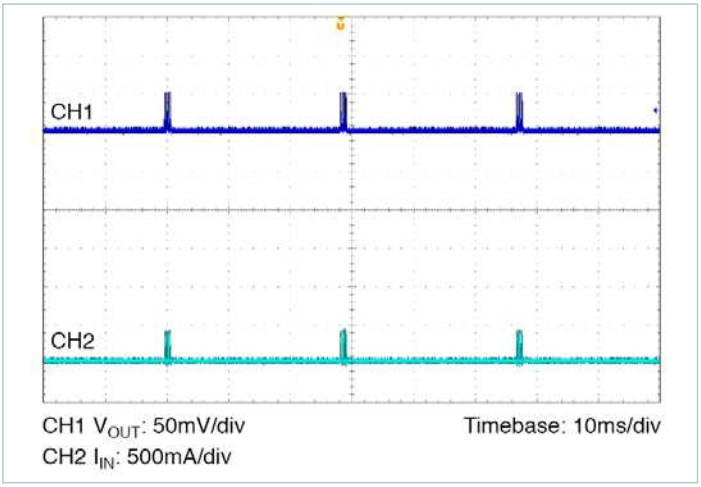


Figure 22 — *Output Short Circuit, Nominal Line*

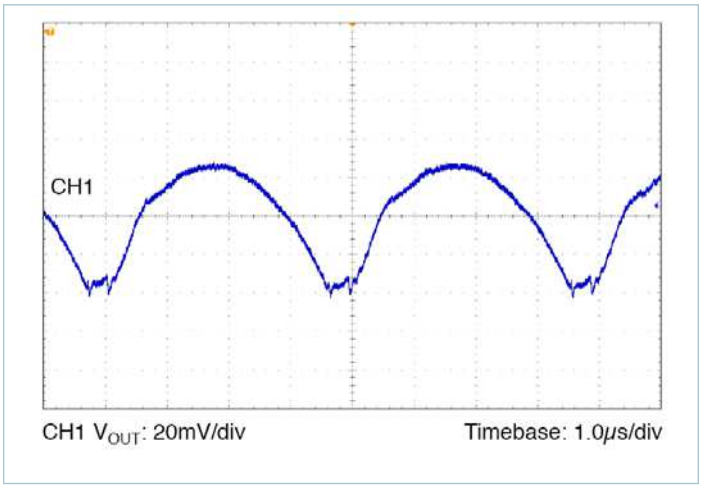


Figure 20 — *Output Voltage Ripple: Nominal Line, Nominal Trim, 100% load, C_{OUT} = 8 x 100µF Ceramic*

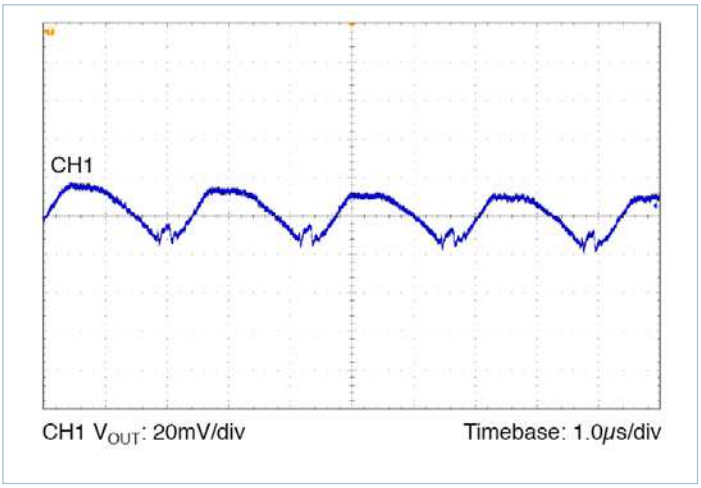


Figure 23 — *Output Voltage Ripple: Nominal Line, Nominal Trim, 50% load, C_{OUT} = 8 x 100µF Ceramic*

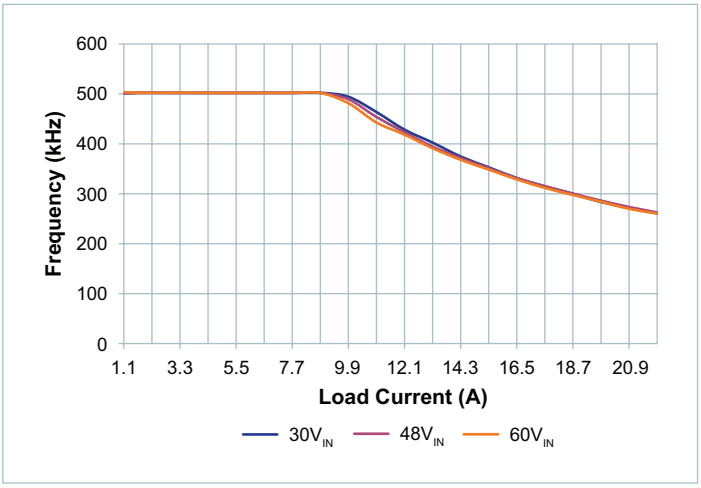


Figure 21 — *Switching Frequency vs. Load, Nominal Trim*

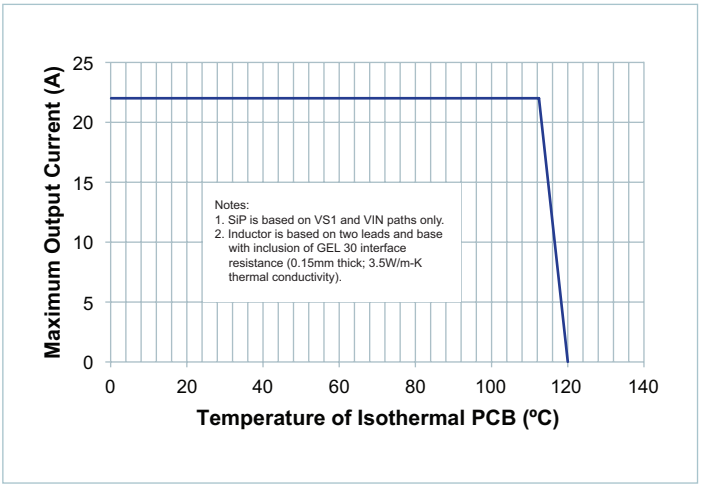


Figure 24 — *System Thermal Specified Operating Area: Max I_{OUT} at Nominal Trim vs. temperature at locations noted*

PI3523-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

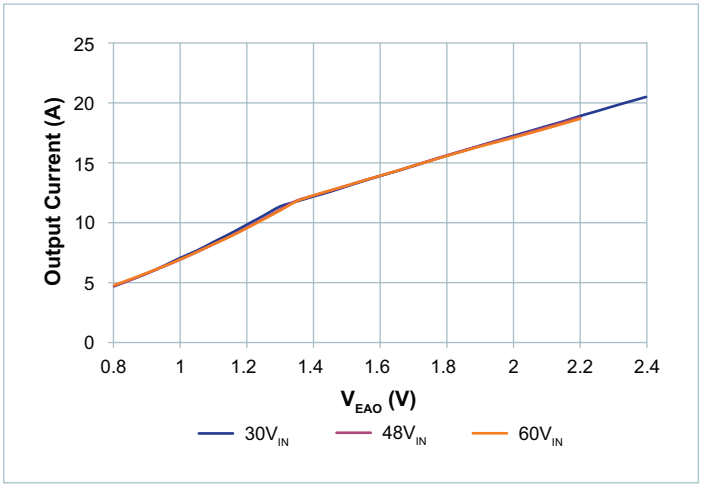


Figure 25 — *Output Current vs. V_{EAO}, Nominal Trim*

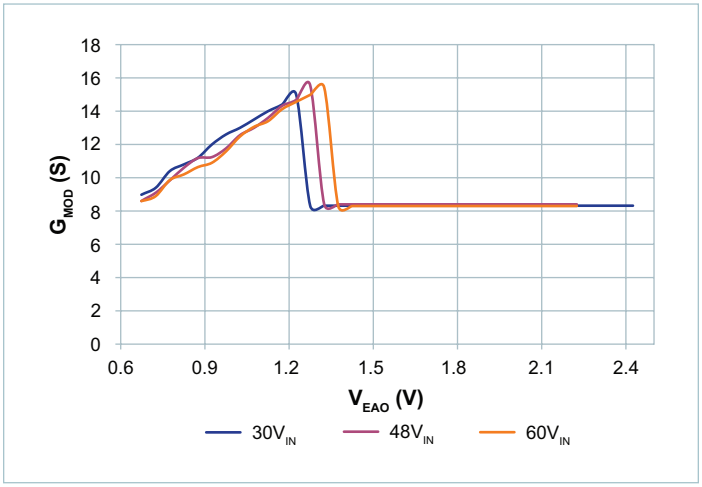


Figure 26 — *Small Signal Modulator Gain vs. V_{EAO}, Nominal Trim*

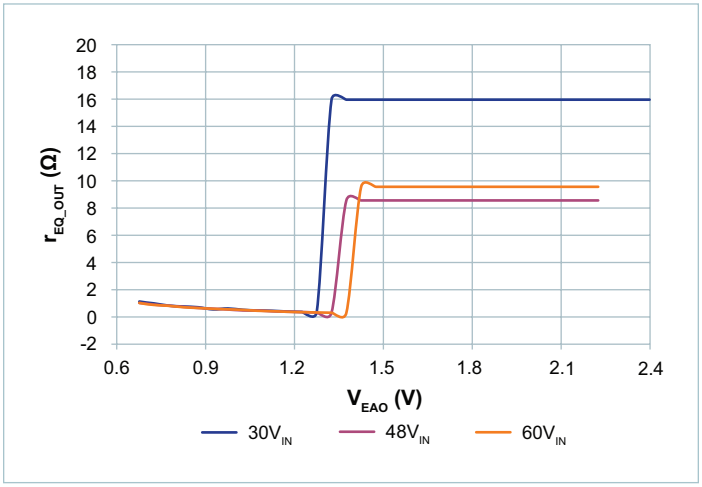


Figure 27 — *r_{EQ_OUT} vs V_{EAO}, Nominal Trim*

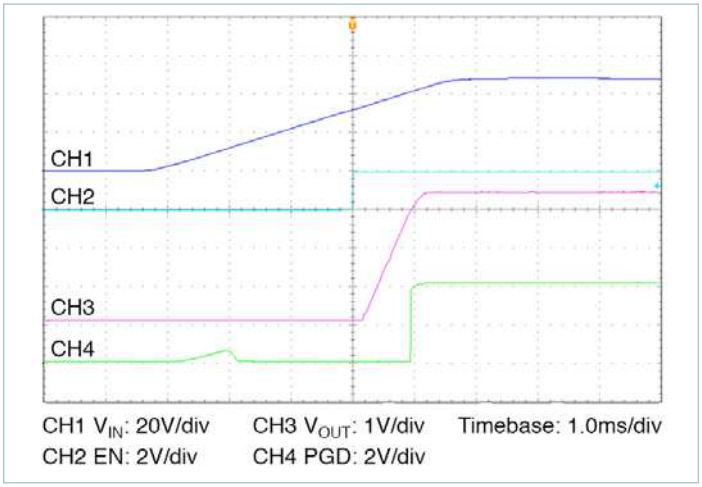


Figure 28 — *Start Up From V_{IN} Applied, Nominal Line, Nominal Trim, Typical Timing, PI3523*

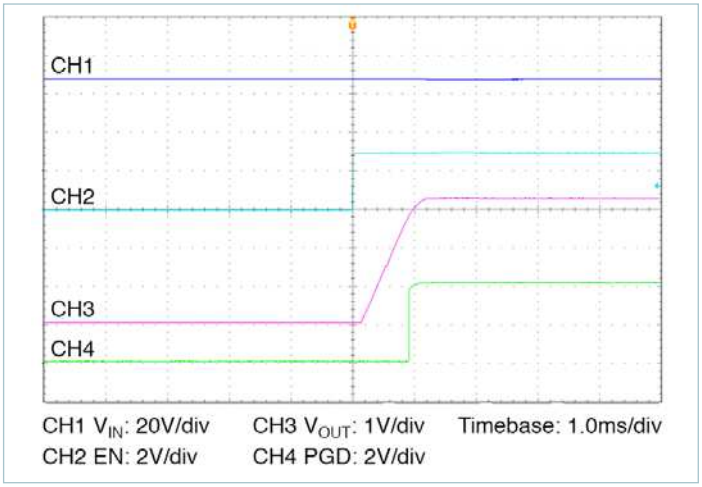


Figure 29 — *Start Up From EN, V_{IN} Pre-Applied, Nominal Line, Nominal Trim, Typical Timing, PI3523*

PI3525-00 (5.0V_{OUT}) Electrical Characteristics

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, I_{OUT} = 20A		2.28		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		2.3		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75	1.2	mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		2.5		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Input capacitance, Internal	C_{IN_INT}	Effective value V_{IN} = 48V, 25°C		0.50		µF
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	4.0	5.0	6.5	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 2A < I_{OUT} < 20A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 20A, C_{OUT} = 12 x 47µF, 20MHz BW [d]		75		mVp-p
Output Current	I_{OUT_DC}	[e]	0		20	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 230nH inductor.		23		A
Maximum Array Size	$N_{PARALLEL}$	[b]			3	Modules
Output Current, array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [b] see applications section for details	0		[g]	A
Output Current, array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [b] see applications section for details	0		[g]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27.0	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO}		62	64.3		V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY}	0.90	1.17	1.60	V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		6.7	7.5		V

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.
[g] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3525-00 (5.0V_{OUT}) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[f] While in Discontinuous Conduction Mode (DCM) only, SYNCI grounded	564	600	636	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	–50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [c] [f]	300		660	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EAIN_OV}		50	80	110	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, Internal	C_{TRK_INT}			47		nF
Soft-Start Time	t_{SS}	C_{TRK_EXT} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.8		V
EAIN Capacitance, Internal	C_{EAIN_INT}			56		pF
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		5		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.
[g] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3525-00 ($5V_{OUT}$) Electrical Characteristics (Cont.)

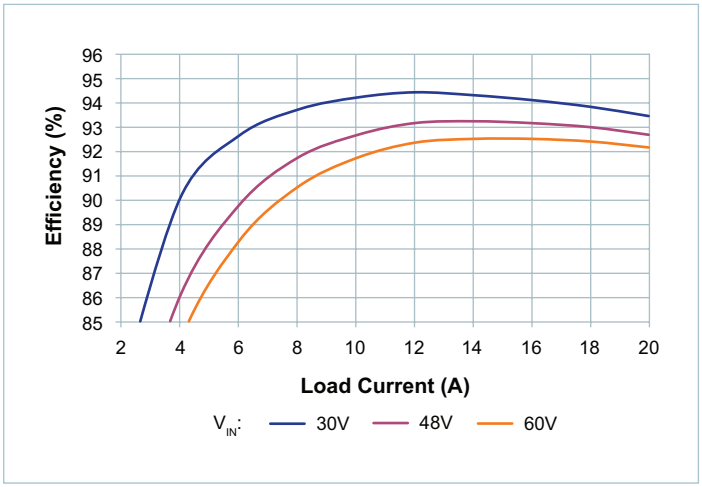


Figure 30 — *System Efficiency, Nominal Trim, Board Temperature = 25°C*

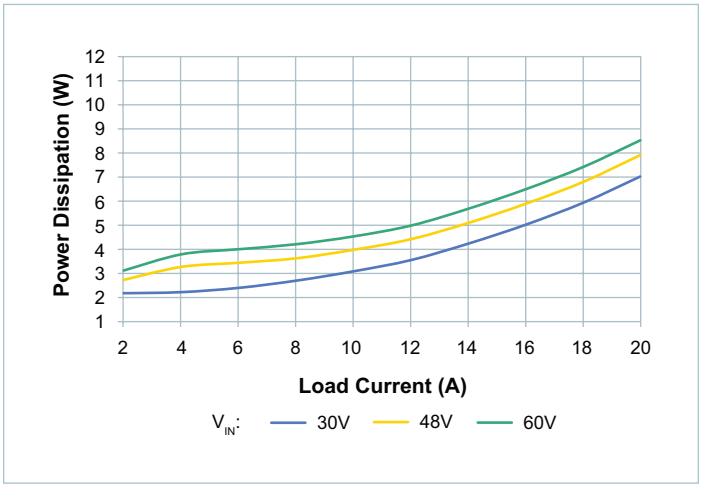


Figure 33 — *System Power Dissipation, Nominal Trim, Board Temperature = 25°C*

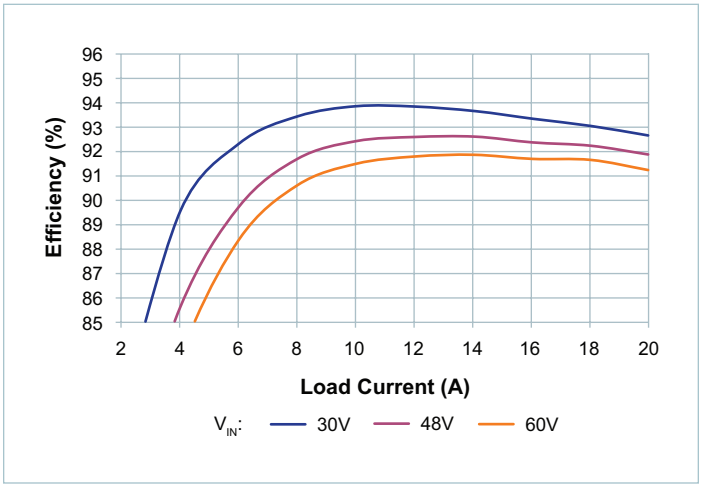


Figure 31 — *System Efficiency, Low Trim, Board Temperature = 25°C*

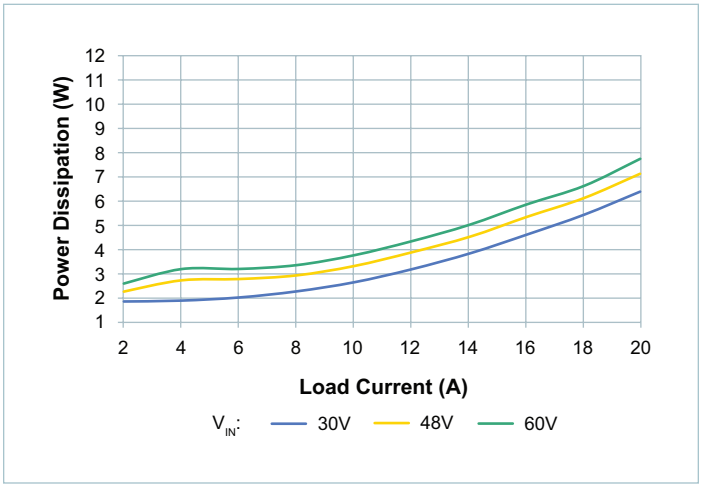


Figure 34 — *System Power Dissipation, Low Trim, Board Temperature = 25°C*

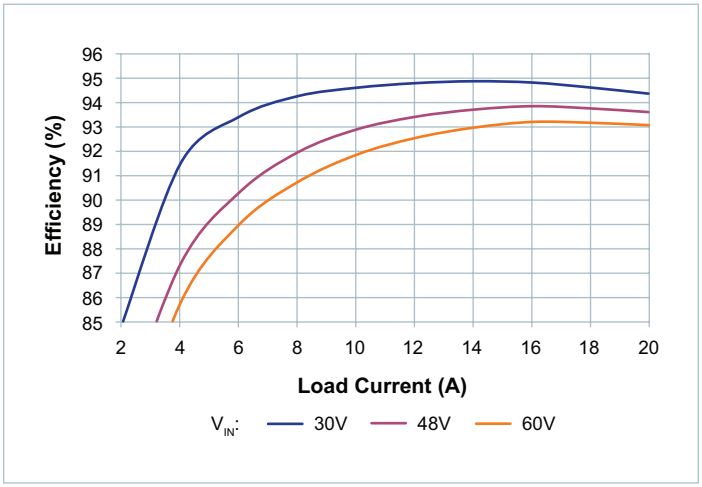


Figure 32 — *System Efficiency, High Trim, Board Temperature = 25°C*

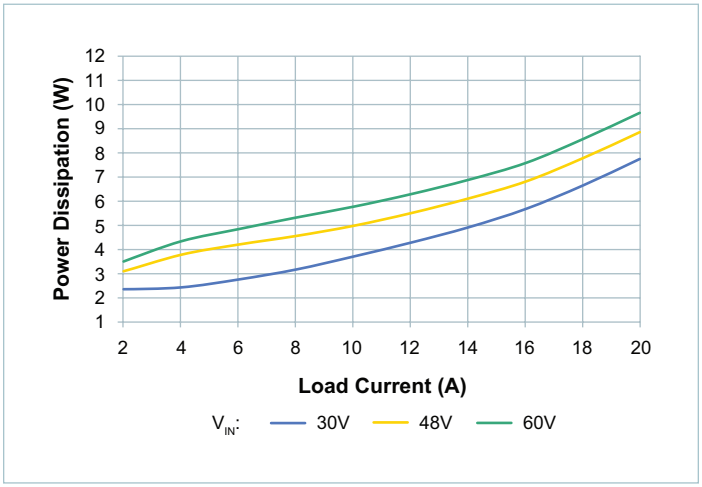


Figure 35 — *System Power Dissipation, High Trim, Board Temperature = 25°C*

PI3525-00 ($5V_{OUT}$) Electrical Characteristics (Cont.)

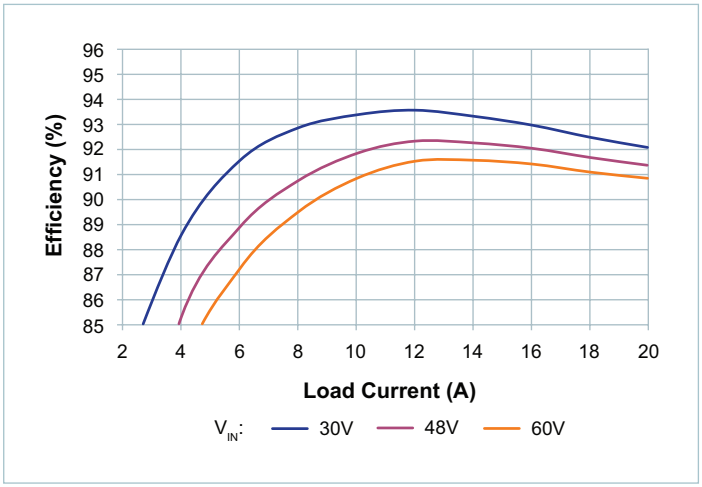


Figure 36 *— System Efficiency, Nominal Trim, Board Temperature = 90°C*

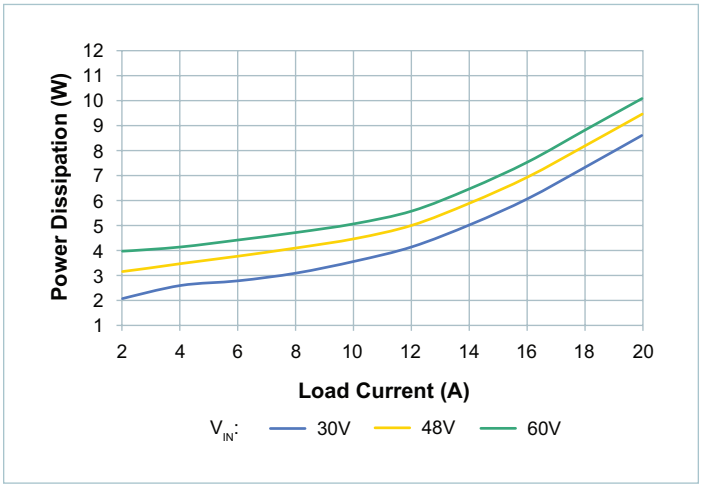


Figure 39 *— System Power Dissipation, Nominal Trim, Board Temperature = 90°C*

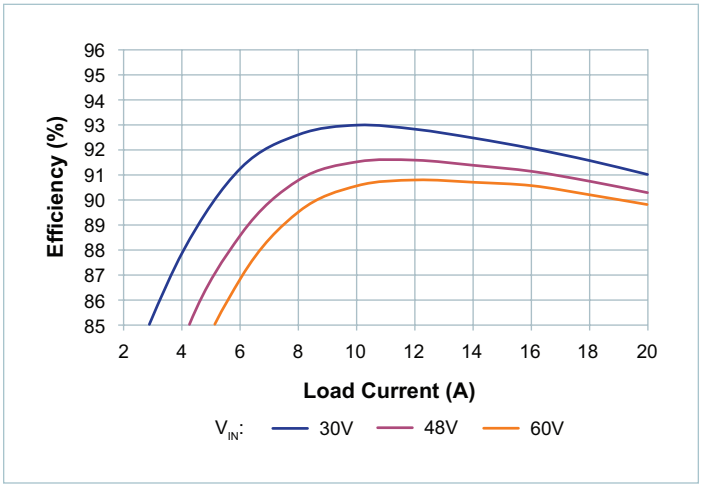


Figure 37 *— System Efficiency, Low Trim, Board Temperature = 90°C*

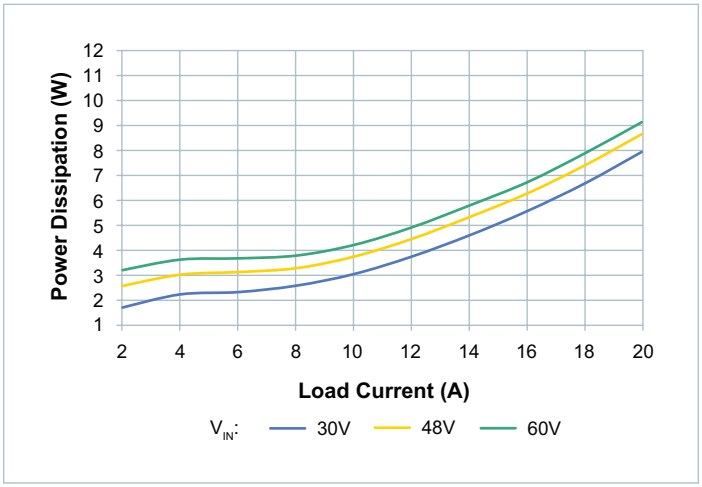


Figure 40 *— System Power Dissipation, Low Trim, Board Temperature = 90°C*

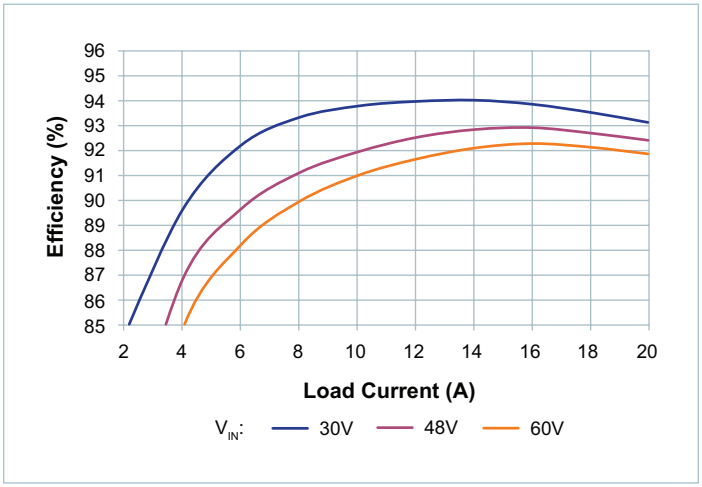


Figure 38 *— System Efficiency, High Trim, Board Temperature = 90°C*

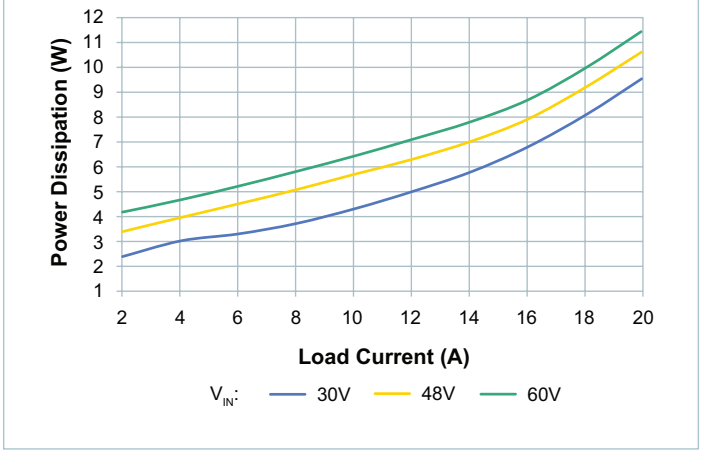


Figure 41 *— System Power Dissipation, High Trim, Board Temperature = 90°C*

PI3525-00 ($5V_{OUT}$) Electrical Characteristics (Cont.)

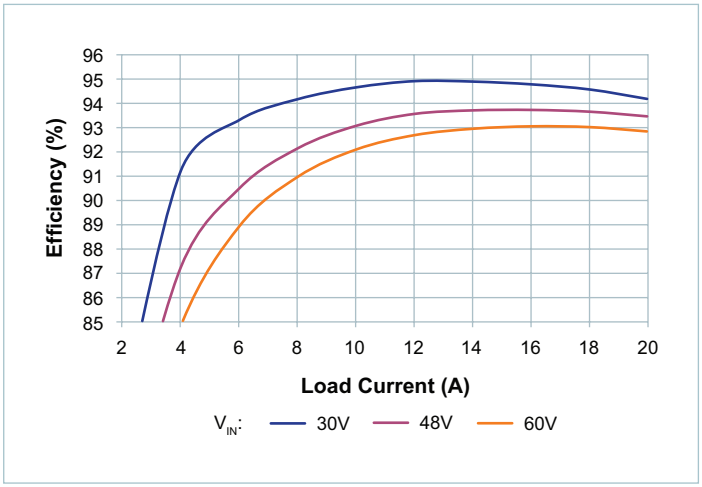


Figure 42 — *System Efficiency, Nominal Trim, Board Temperature = –40°C*

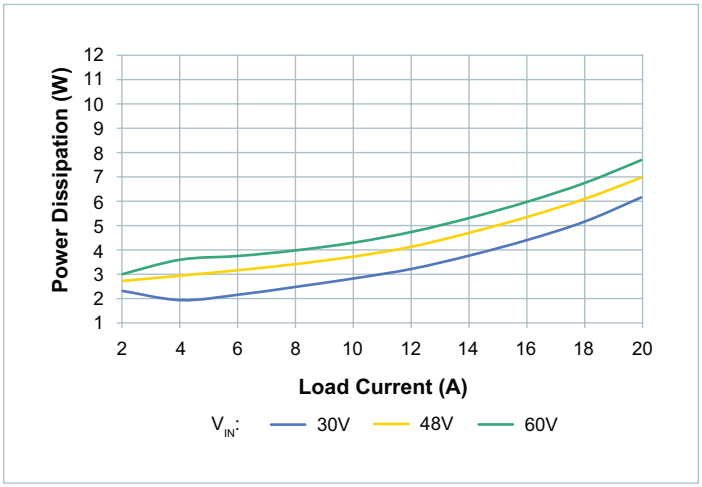


Figure 45 — *System Power Dissipation, Nominal Trim, Board Temperature = –40°C*

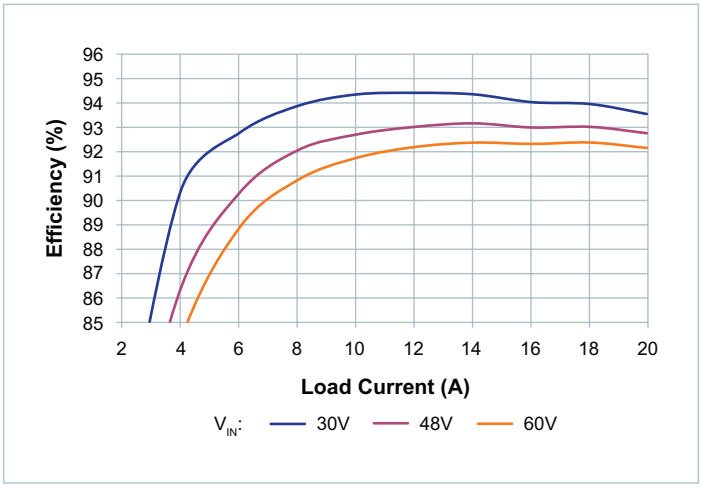


Figure 43 — *System Efficiency, Low Trim, Board Temperature = –40°C*

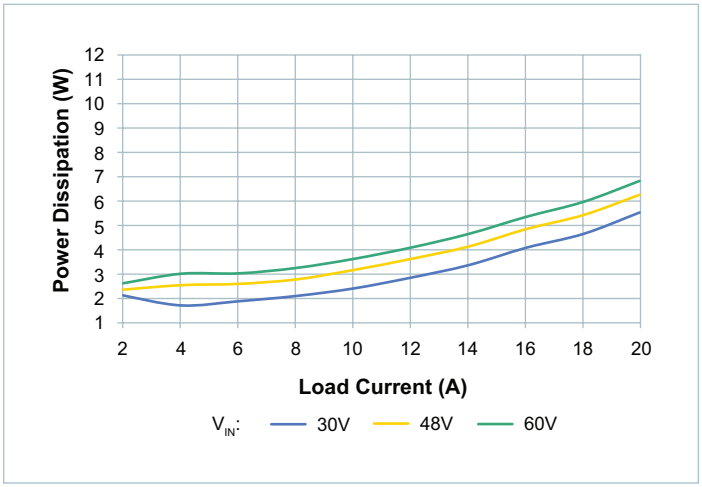


Figure 46 — *System Power Dissipation, Low Trim, Board Temperature = –40°C*

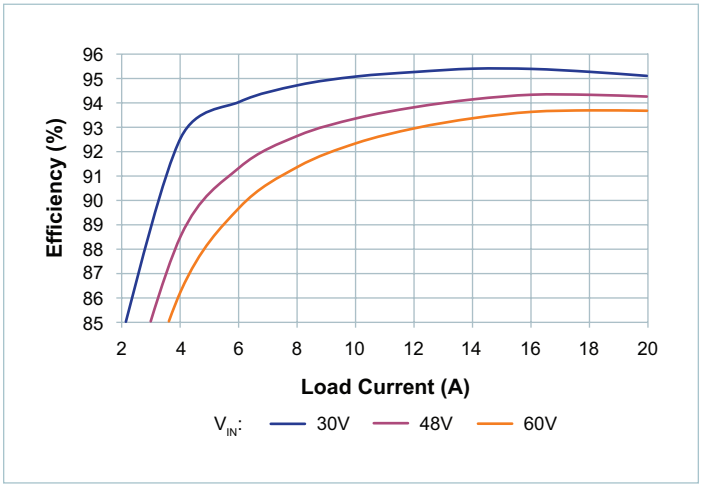


Figure 44 — *System Efficiency, High Trim, Board Temperature = –40°C*

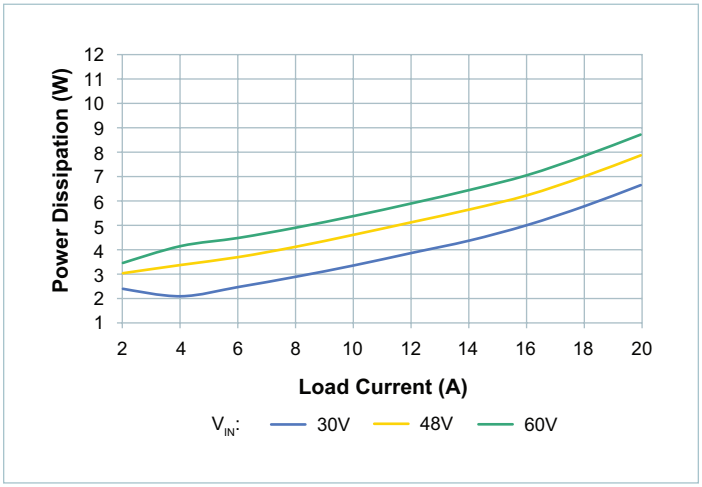


Figure 47 — *System Power Dissipation, High Trim, Board Temperature = –40°C*

PI3525-00 ($5V_{OUT}$) Electrical Characteristics (Cont.)

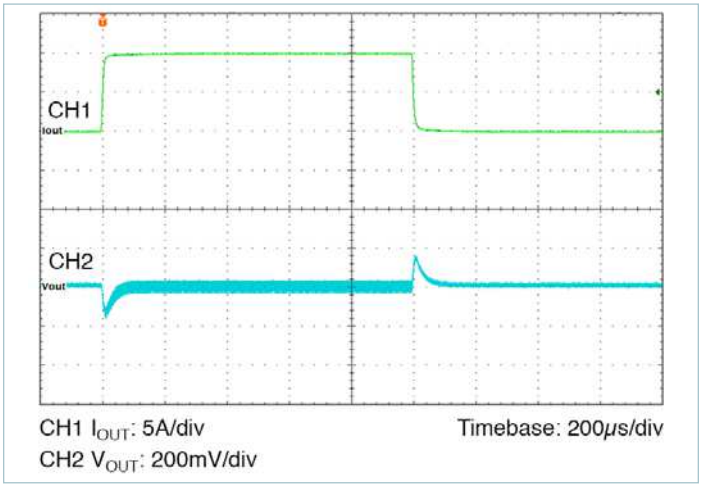


Figure 48 — *Transient Response: 50% to 100% load, at 1A/µs. Nominal Line, Nominal Trim, C_{OUT} = 12 x 47µF Ceramic*

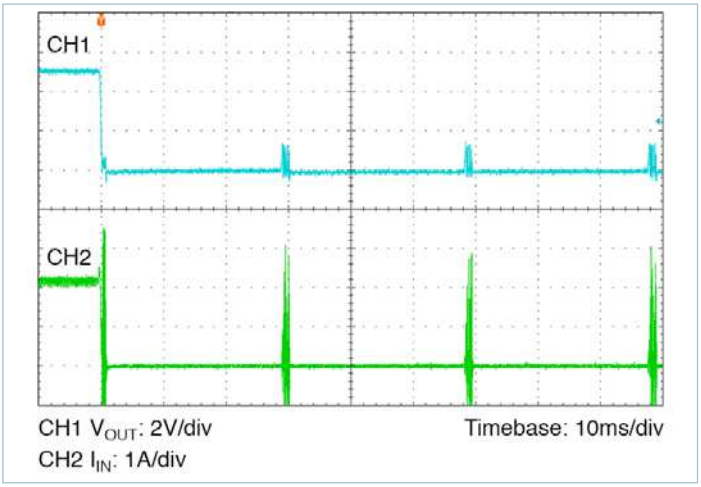


Figure 51 — *Output Short Circuit, Nominal Line*

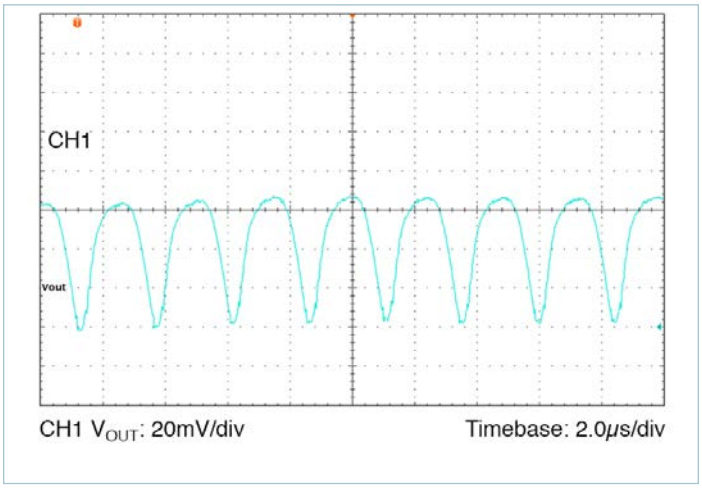


Figure 49 — *Output Voltage Ripple: Nominal Line, Nominal Trim, 100% load, C_{OUT} = 12 x 47µF Ceramic*

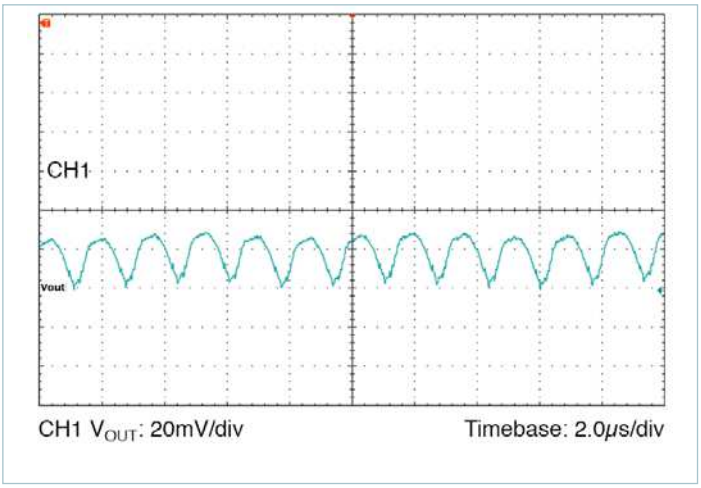


Figure 52 — *Output Voltage Ripple: Nominal Line, Nominal Trim, 50% load, C_{OUT} = 12 x 47µF Ceramic*

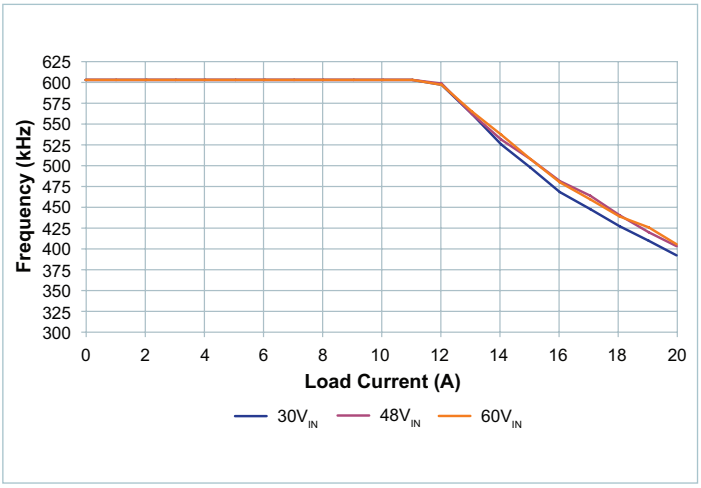


Figure 50 — *Switching Frequency vs. Load, Nominal Trim*

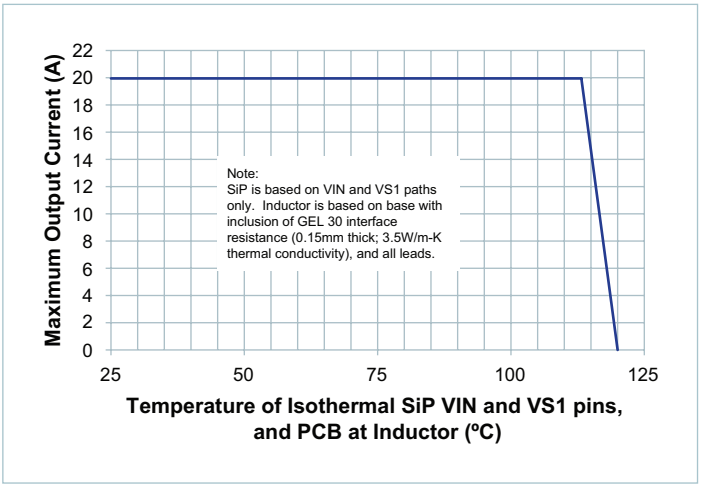


Figure 53 — *System Thermal Specified Operating Area: Max I_{OUT} at Nominal Trim vs. temperature at locations noted*

PI3525-00 ($5V_{OUT}$) Electrical Characteristics (Cont.)

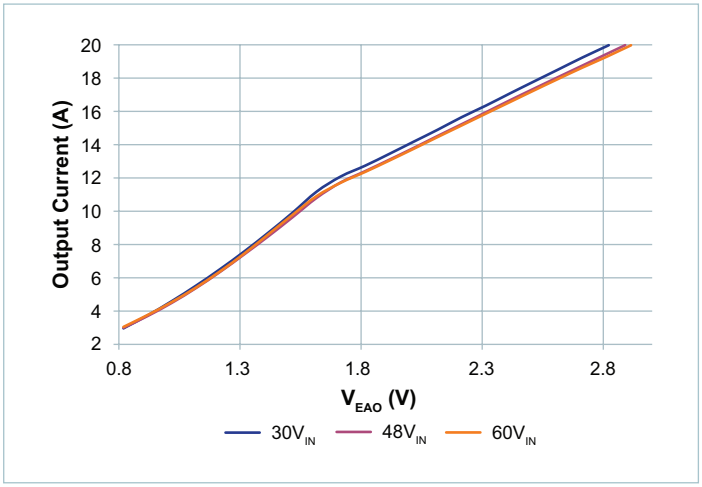


Figure 54 — *Output Current vs. V_{EAO}, Nominal Trim*

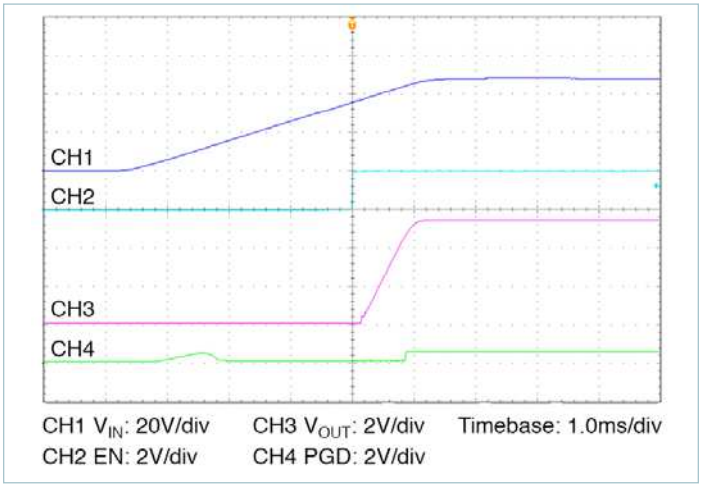


Figure 57 — *Start Up From V_{IN} Applied, Nominal Line, Nominal Trim, Typical Timing, PI3525*

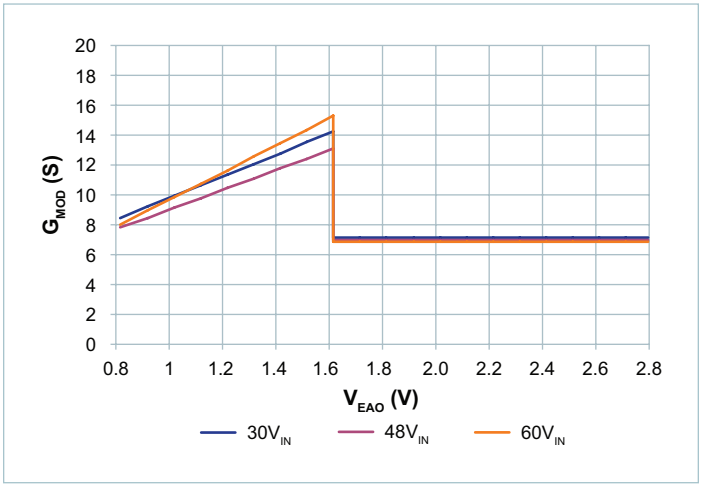


Figure 55 — *Small Signal Modulator Gain vs. V_{EAO}, Nominal Trim*

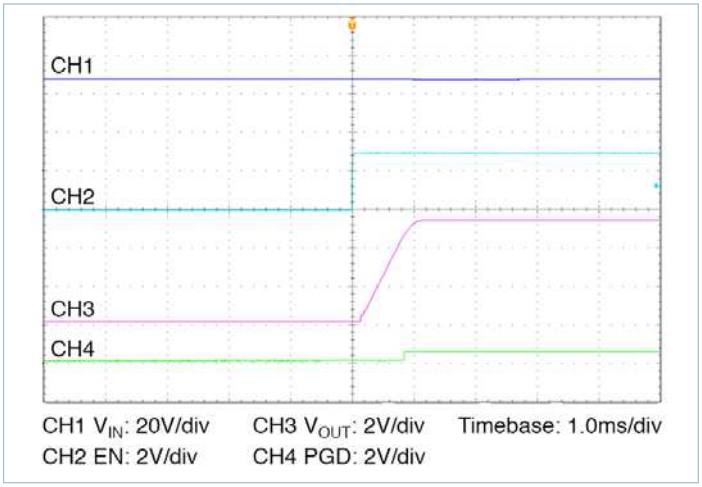


Figure 58 — *Start Up From EN, V_{IN} Pre-Applied, Nominal Line, Nominal Trim, Typical Timing, PI3525*

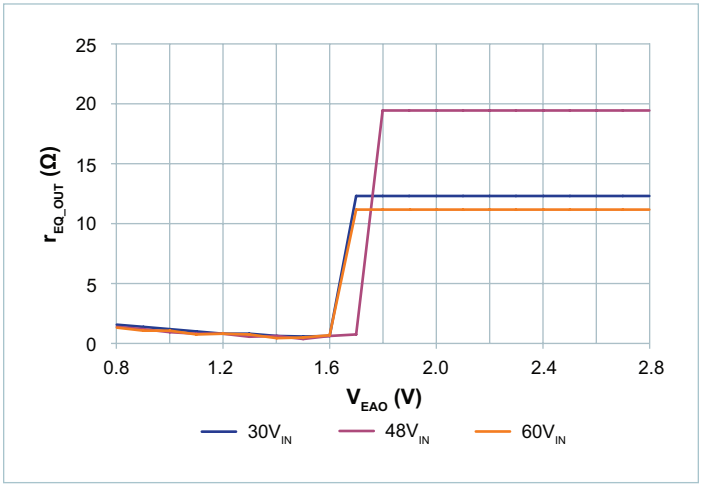


Figure 56 — *r_{EQ_OUT} vs V_{EAO}, Nominal Trim*

PI3526-00 ($12V_{OUT}$) Electrical Characteristics

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		30	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_{CASE} = 25°C, I_{OUT} = 18A		4.68		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		4.5		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75	1.2	mA
Input Quiescent Current	I_{Q_VIN}	Enabled, no load, T_{CASE} = 25°C		3.2		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Input capacitance, Internal	C_{IN_INT}	Effective value V_{IN} = 48V, 25°C		0.50		µF
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.975	0.990	1.005	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	6.5	12	14	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 30V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 2A < I_{OUT} < 20A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 18A, C_{OUT} = 8 x 10µF, 20MHz BW [d]		240		mVp-p
Output Current	I_{OUT_DC}	[e]	0		18	A
Current Limit	I_{OUT_CL}	Typical current limit based on nominal 480nH inductor.		20.7		A
Maximum Array Size	$N_{PARALLEL}$	[b]			3	Modules
Output Current, array of 2	$I_{OUT\_DC\_ARRAY2}$	Total array capability, [b] see applications section for details	0		[g]	A
Output Current, array of 3	$I_{OUT\_DC\_ARRAY3}$	Total array capability, [b] see applications section for details	0		[g]	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}			27	29.1	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		1.66	2.08	2.50	V
Input UVLO Response Time				1.25		µs
Input OVLO Stop Threshold	V_{OVLO}		62	64.3		V
Input OVLO Start Hysteresis	V_{OVLO_HYS}	Hysteresis active when OVLO present for at least t_{FR_DLY}	0.90	1.17	1.60	V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection, Relative	V_{OVP_REL}	Above set V_{OUT}		20		%
Output Overvoltage Protection, Absolute	V_{OVP_ABS}		14.6	15.7		V

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.
[g] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3526-00 ($12V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_{INT} < 120°C, V_{IN} = 48V, EN = High, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_s	[f] While in DCM operating mode only, SYNCI grounded	658	700	742	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Synchronization Input (SYNCI)						
Synchronization Frequency Range	f_{SYNCI}	–50% and +10% relative to set switching frequency (f_S), while in DCM operating mode only. [c] [f]	350		770	kHz
SYNCI Threshold	V_{SYNCI}			2.5		V
Synchronization Output (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EAIN_OV}		50	80	110	mV
Charge Current (Soft Start)	I_{TRK}		30	50	70	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		8.7		mA
TRK Capacitance, Internal	C_{TRK_INT}			47		nF
Soft-Start Time	t_{SS}	C_{TRK_EXT} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.8		V
EAIN Capacitance, Internal	$C_{EAIN-INT}$			56		pF
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		5		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI352x evaluation board with 3 x 3" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to Output Ripple plots.
[e] Refer to Load Current vs. Ambient Temperature curves.
[f] Refer to Switching Frequency vs. Load current curves.
[g] Contact factory applications for array derating and layout best practices to minimize sharing errors.

PI3526-00 ($12V_{OUT}$) Electrical Characteristics (Cont.)

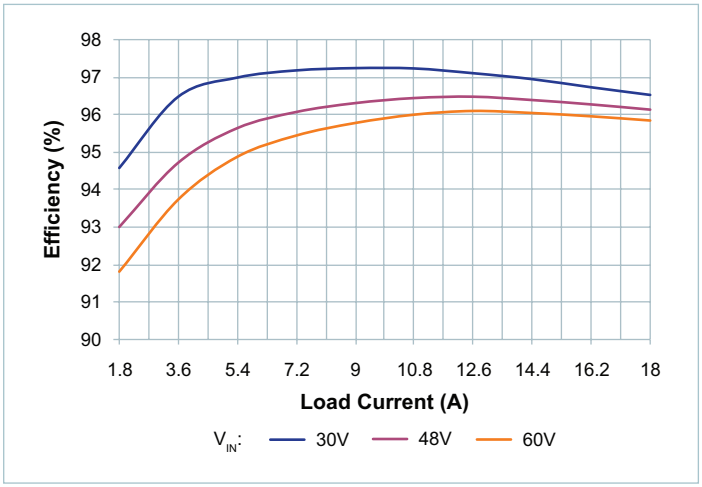


Figure 59 — *System Efficiency, Nominal Trim, Board Temperature = 25°C*

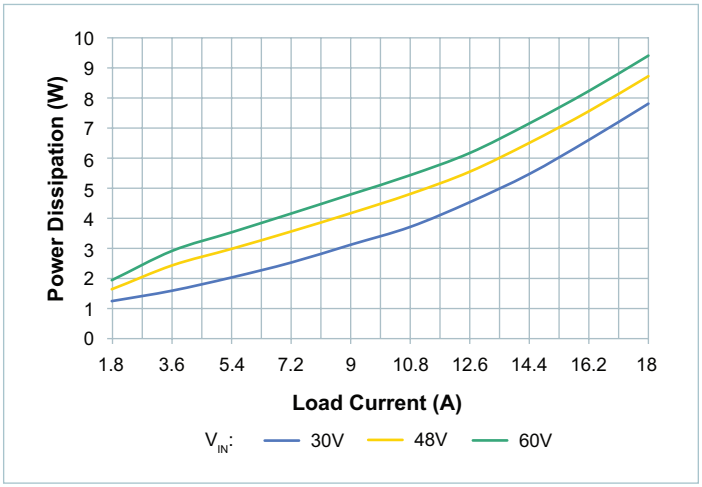


Figure 62 — *System Power Dissipation, Nominal Trim, Board Temperature = 25°C*

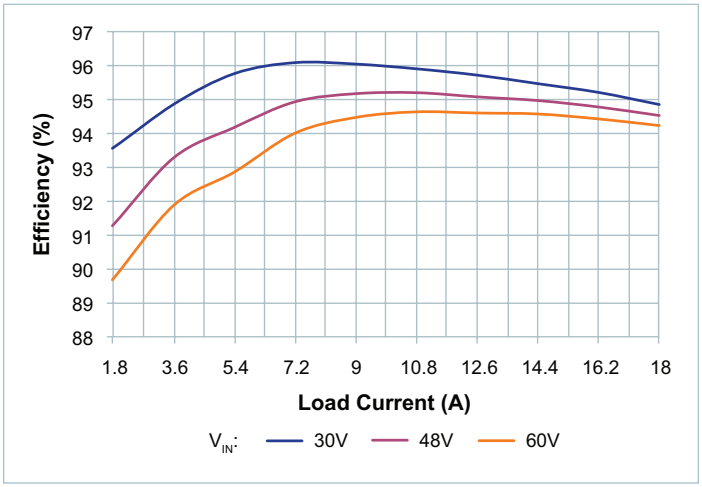


Figure 60 — *System Efficiency, Low Trim, Board Temperature = 25°C*

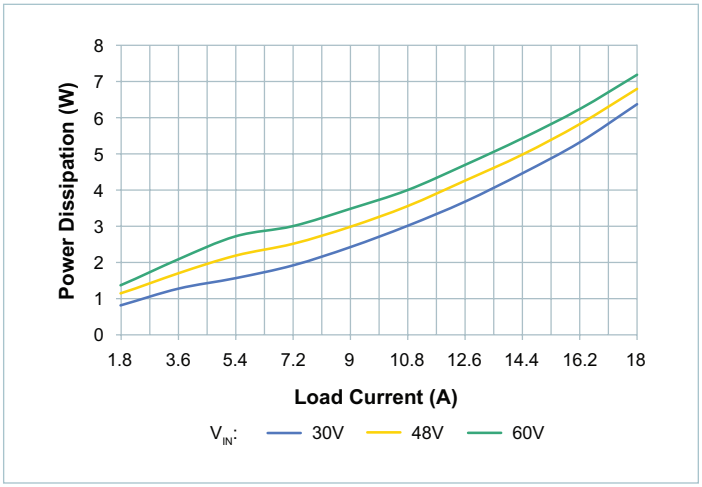


Figure 63 — *System Power Dissipation, Low Trim, Board Temperature = 25°C*

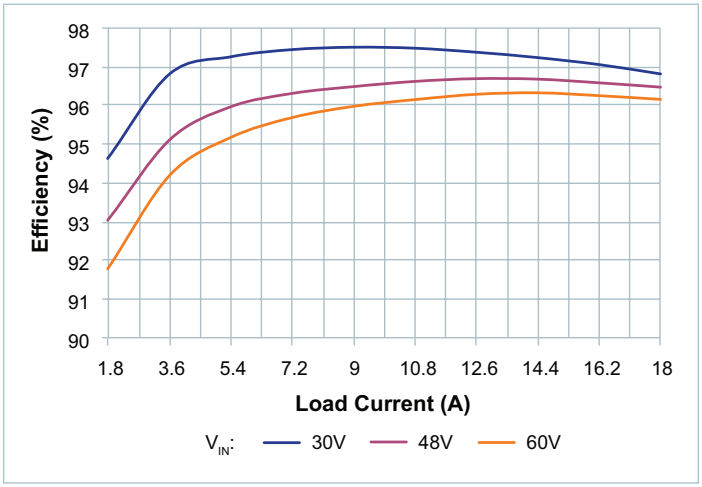


Figure 61 — *System Efficiency, High Trim, Board Temperature = 25°C*

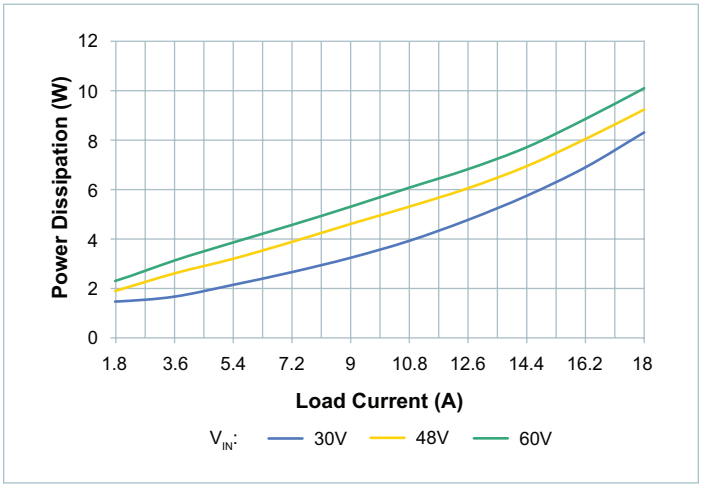


Figure 64 — *System Power Dissipation, High Trim, Board Temperature = 25°C*

PI3526-00 ($12V_{OUT}$) Electrical Characteristics (Cont.)

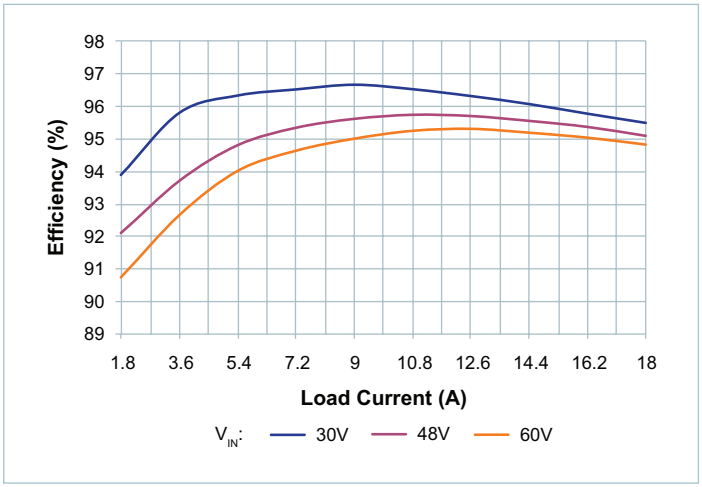


Figure 65 — *System Efficiency, Nominal Trim, Board Temperature = 100°C*

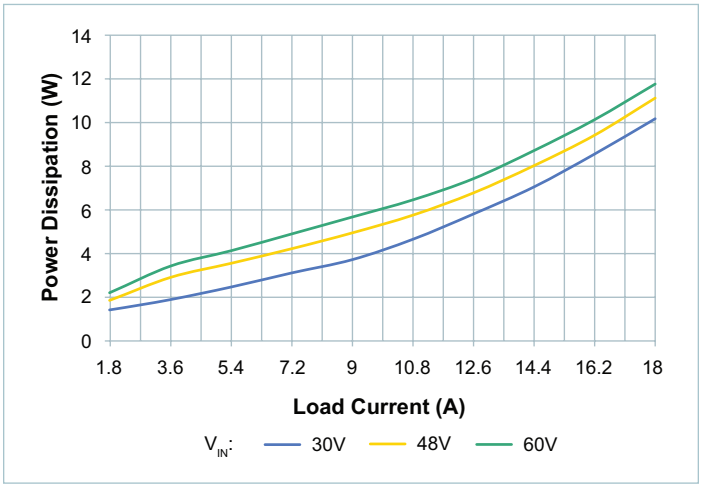


Figure 68 — *System Power Dissipation, Nominal Trim, Board Temperature = 100°C*

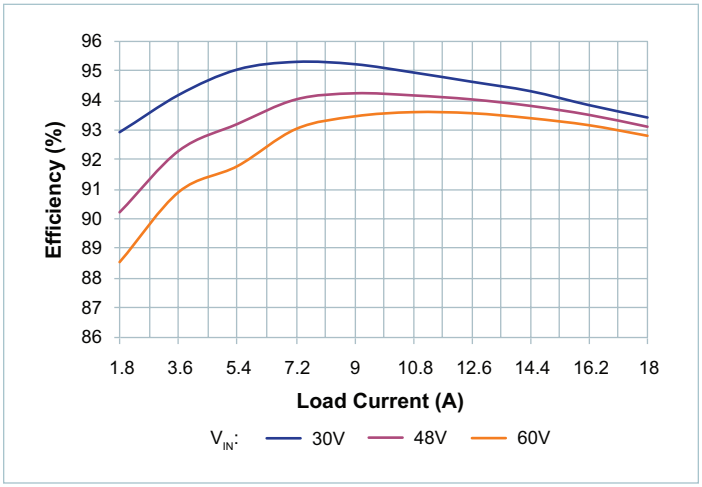


Figure 66 — *System Efficiency, Low Trim, Board Temperature = 100°C*

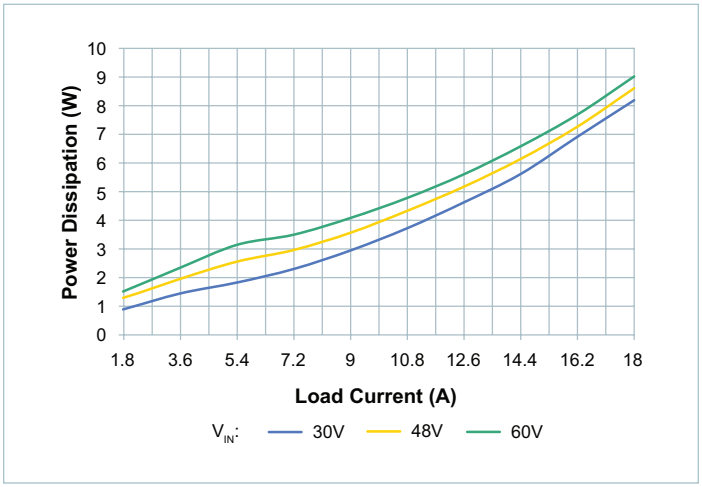


Figure 69 — *System Power Dissipation, Low Trim, Board Temperature = 100°C*

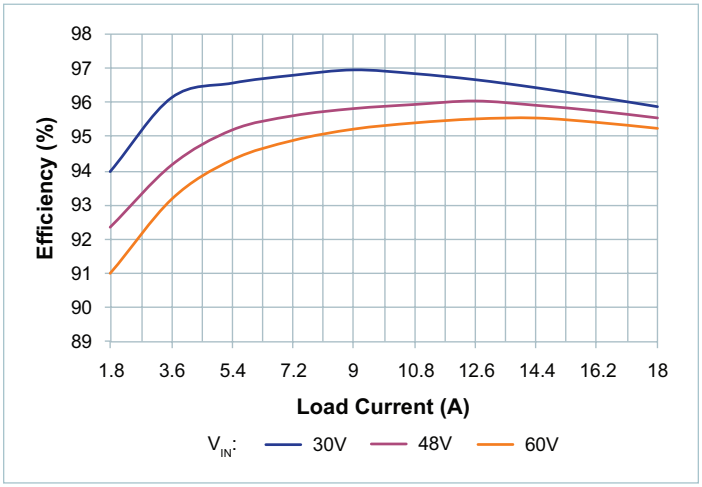


Figure 67 — *System Efficiency, High Trim, Board Temperature = 100°C*

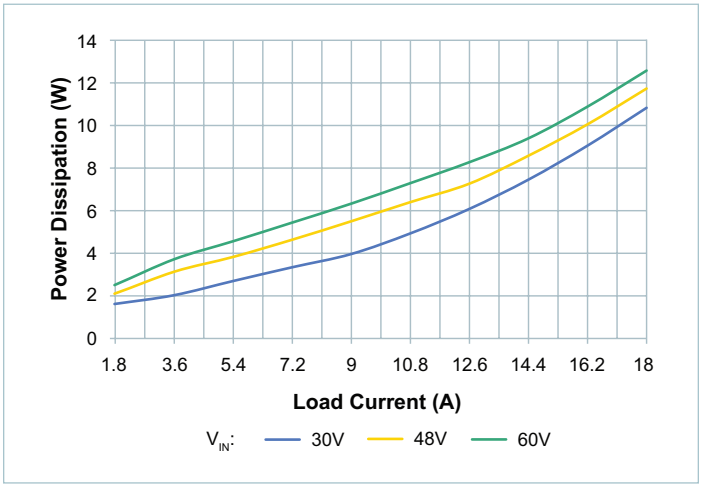


Figure 70 — *System Power Dissipation, High Trim, Board Temperature = 100°C*