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## Small Plastic Package, Quad SPDT Analog Switch

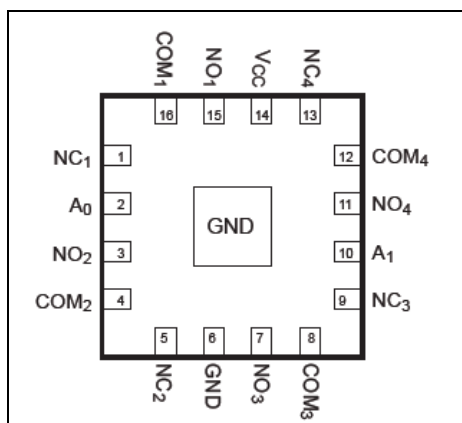
### Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.5Ω
- Wide V<sub>DD</sub> Range: 1.8V to 4.2V
- Rail-to-Rail Signal Range
- High Off Isolation: -83dB @ 100kHz
- Channel-to-Channel Crosstalk Rejection: -97dB @ 100kHz
- Break-Before-Make Switching
- Extended Industrial Temperature Range: -40°C to 85°C
- ESD protection: 4kV(HBM)
- Packaging (Pb-free & Green): 16-PinTQFN 3x3 (ZH16)

### Applications

- Cell Phones
- PDAs
- MP3 Players
- Portable Instrumentation
- Computer Peripherals
- Speaker Headset Switching
- Power Routing
- Relay Replacement
- Audio and Video Signal Routing
- PCMCIA Cards
- Modems

### Pin Configuration ( top view)



### Description

PI3A412 is a quad single-pole double throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage, 1.8V to 4.2V, the PI3A412 has an On-Resistance of 0.5Ω at +4.2V.

Control inputs(Ax) are independent of supply voltage.

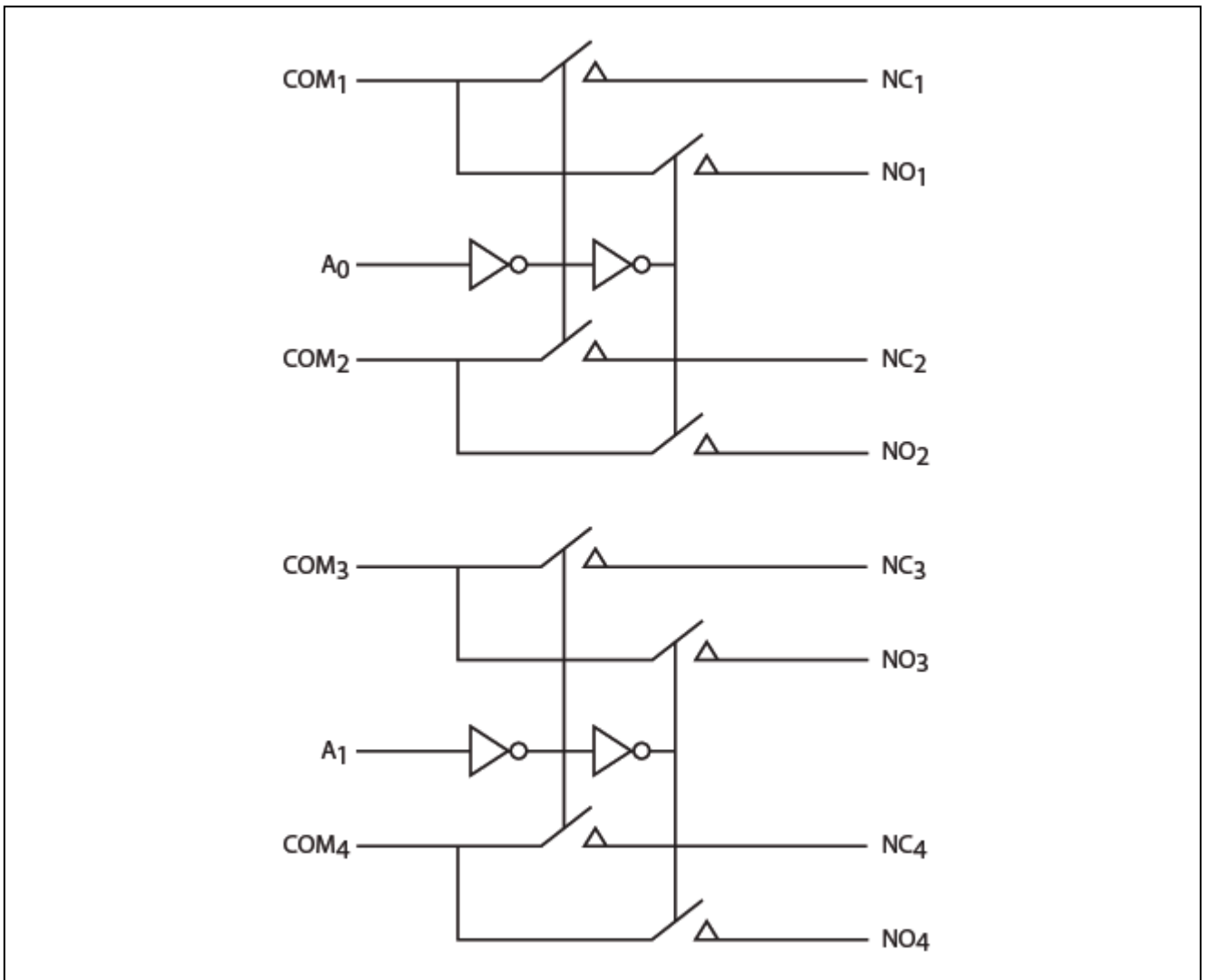
### Pin Description

Pin no	Name	Description
1	NC1	Data Port (Normally connect)
2	A0	Logic Input Control
3	NO2	Data Port (Normally open)
4	COM2	Common Output / Data Port
5	NC2	Data Port (Normally connect)
6	GND	Ground
7	NO3	Data Port (Normally open)
8	COM3	Common Output / Data Port
9	NC3	Data Port (Normally connect)
10	A1	Logic Input Control
11	NO4	Data Port (Normally open)
12	COM4	Common Output / Data Port
13	NC4	Data Port (Normally connect)
14	V <sub>CC</sub>	Positive Power Supply
15	NO1	Data Port (Normally open)
16	COM1	Common Output / Data Port

### Logic Function Table

Logic Input (IN <sub>x</sub> )	Function
0	NC <sub>x</sub> Connected to COM <sub>x</sub>
1	NO <sub>x</sub> Connected to COM <sub>x</sub>

Note: x = 1, 2, 3 or 4

**Functional Block Diagram**


A0	Function	A1	Function
0	NC <sub>x</sub> Connected to COM <sub>x</sub>	0	NC <sub>y</sub> Connected to COM <sub>y</sub>
1	NO <sub>x</sub> Connected to COM <sub>x</sub>	1	NO <sub>y</sub> Connected to COM <sub>y</sub>

**Notes:**

1. X = 1 or 2
2. Y = 3 or 4

## Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage $V_{DD}$ .....	-0.5V to +4.6V
Control Input Voltage $V_{INx}$ .....	0V to +4.6V
DC Input Voltage $V_{INPUT}$ .....	-0.5V to +4.6V
Continuous Current NO_NC_COM_.....	±400mA
Peak Current NO_NC_COM_.....	±500mA
(pulsed at 1ms 10% duty cycle) .....	±500mA
ESD (HBM) .....	4kV

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Control input must be held HIGH or LOW; it must not float.

## Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating Voltage	-	1.8	-	4.2	V
$V_{IN}$	Control Input Voltage	-	0	-	$V_{CC}$	V
$V_{INPUT}$	Switch Input Voltage	-	-0.3	-	$V_{CC}$	V
$T_A$	Operating Temperature	-	-40	25	85	°C
$t_r, t_f$	Input Rise and Fall Time	-	0	-	10	ns/V

### DC Electrical Characteristics

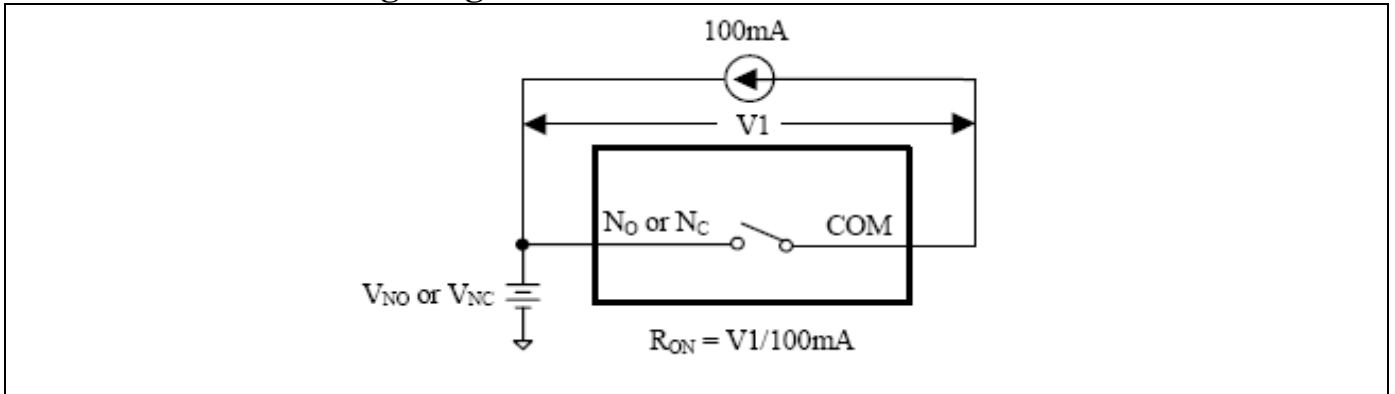
**+3.0V Supply** ( $V_{DD} = 2.7V$  to  $3.6V$ ,  $V_{IH} = +1.6V$ ,  $V_{IL} = +0.4V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ , unless otherwise noted. Typical values are at  $3.0V$  and  $+25^{\circ}C$ .)

Parameter	Symbol	Test Conditions	TEMP	Min.	Typ.	Max.	Units	
<b>ANALOG SWITCH</b>								
Analog Signal Range	$V_{NO}, V_{NC}, V_{COM}$		$-40^{\circ}C$ to $85^{\circ}C$	0	-	$V_{CC}$	V	
On-Resistance	$R_{ON}$	$V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO}$ or $V_{NC} = 1V, \text{Test Circuit 1}$	$+25^{\circ}C$	-	0.6	0.9	$\Omega$	
			$-40^{\circ}C$ to $85^{\circ}C$	-	-	1		
On-Resistance Match Between Channels	$\Delta R_{ON}$	$V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO}$ or $V_{NC} = 1V, \text{Test Circuit 1}$	$+25^{\circ}C$	-	0.05	0.2	$\Omega$	
			$-40^{\circ}C$ to $85^{\circ}C$	-	0.05	0.24		
On-Resistance Flatness	$R_{ONF}$	$V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO}$ or $V_{NC} = 1V, 2.5V, \text{Test Circuit 1}$	$+25^{\circ}C$	-	0.05	0.15	$\Omega$	
			$-40^{\circ}C$ to $85^{\circ}C$	-	0.1	0.2		
Source Off Leakage Current	$I_{OFF(NO)}$ or $I_{OFF(NC)}$	$V_{CC} = 3.6V, V_{NO}$ or $V_{NC} = 3.3V/0.3V, V_{COM} = 0.3V/3.3V$	$-40^{\circ}C$ to $85^{\circ}C$	-	-	1	$\mu A$	
Channel On Leakage Current	$I_{NC(ON)}, I_{NO(ON)}, I_{COM(ON)}$	$V_{CC} = 3.6V, V_{NO}$ or $V_{NC} = 3V/0.3V, V_{COM} = 3V/0.3V$ , or floating	$-40^{\circ}C$ to $85^{\circ}C$	-	-	1		
<b>DIGITAL INPUTS</b>								
Input Logic High	$V_{IH}$		$-40^{\circ}C$ to $85^{\circ}C$	1.2	-	-	V	
Input Logic Low	$V_{IL}$		$-40^{\circ}C$ to $85^{\circ}C$	-	-	0.5		
IN Input Leakage Current	$I_{IN}$	$V_{CC} = 2.7V, V_{IN} = 0$ or $2.7V$	$-40^{\circ}C$ to $85^{\circ}C$	-	-	1	$\mu A$	
<b>DYNAMIC CHARACTERISTICS</b>								
Turn-On Time	$t_{ON}$	$V_{CC} = 3.3V, V_{NO}$ or $V_{NC} = 2.0V, R_L = 50\Omega, C_L = 35pF, \text{See Test Circuit Figure 2.}$	$+25^{\circ}C$	-	16	-	ns	
Turn-Off Time	$t_{OFF}$		$+25^{\circ}C$	-	60	-	ns	
Break-Before-Make Delay	$t_D$	$V_{IH} = 1.5V, V_{IL} = 0V, \text{See Test Circuit Figure 3.}$	$+25^{\circ}C$	-	10	-	ns	
NC-NO and COM-NC/NO Off-Isolation	$O_{ISO}$	$V_{BIAS} = 1.5V, V_{IN} = 0dBm, V_{IH} = 1.5V, V_{IL} = 0V. \text{See Test Circuit Figure 4 \& Figure 5}$	100kHz	$+25^{\circ}C$	-	-81	-	dB
			1MHz	$+25^{\circ}C$	-	-61	-	
			10MHz	$+25^{\circ}C$	-	-39	-	
Channel-to-Channel Crosstalk	$X_{TALK}$	$V_{BIAS} = 1.5V, V_{IN} = 0dBm, V_{IH} = 1.5V, V_{IL} = 0V \text{See Test Circuit Figure 6.}$	100kHz	$+25^{\circ}C$	-	-97	-	dB
			1MHz	$+25^{\circ}C$	-	-98	-	
			10MHz	$+25^{\circ}C$	-	-77	-	
3dB Bandwidth	$f_{3dB}$	$V_{BIAS} = 1.5V, V_{IN} = 0dBm, V_{IH} = 1.5V, V_{IL} = 0V. \text{See Test Circuit Figure 7.}$	$+25^{\circ}C$	-	79	-	MHz	
Charge Injection Select Input to Common I/O	Q	$V_{IN} = GND, R_S = 0, C_L = 1nF, V_{IH} = 1.5V, V_{IL} = 0V \text{See Test Circuit Figure 8.}$	$+25^{\circ}C$	-	35	-	pC	
Off Capacitance	$C_{NC(OFF)}$	$f = 1MHz, \text{See Test Circuit Figure 9}$	$+25^{\circ}C$	-	20	-	pF	
Off capacitance	$C_{NO(OFF)}$			-	20	-		
On Capacitance	$C_{ON}$			$f = 1MHz, \text{See Test Circuit Figure 10}$	$+25^{\circ}C$	-		55

+4.2V Supply ( $V_{DD} = 4.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ , unless otherwise noted. Typical values are at  $4.2V$  and  $+25^\circ C$ .)

Parameter	Symbol	Test Conditions	TEMP	Min.	Typ.	Max.	Units	
<b>Analog Switch</b>								
Analog Signal Range	$V_{NO}, V_{NC}, V_{COM}$		$-40^\circ C$ to $85^\circ C$	0	-	$V_{CC}$	V	
On-Resistance	$R_{ON}$	$V_{CC} = 4.2V, I_{COM} = 100mA, V_{NO}$ or $V_{NC} = 1V, \text{Test Circuit 1}$	$+25^\circ C$	-	0.5	0.75	$\Omega$	
			$-40^\circ C$ to $85^\circ C$	-	-	0.85		
On-Resistance Match Between Channels	$\Delta R_{ON}$	$V_{CC} = 4.2V, I_{COM} = 100mA, V_{NO}$ or $V_{NC} = 1V, \text{Test Circuit 1}$	$+25^\circ C$	-	0.05	0.15	$\Omega$	
			$-40^\circ C$ to $85^\circ C$	-	0.1	0.2		
On-Resistance Flatness	$R_{ONF}$	$V_{CC} = 4.2V, I_{COM} = 100mA, V_{NO}$ or $V_{NC} = 1V, 2.5V, \text{Test Circuit 1}$	$+25^\circ C$	-	0.1	0.22	$\Omega$	
			$-40^\circ C$ to $85^\circ C$	-	-	0.26		
Source Off Leakage Current	$I_{OFF(NO)}$ or $I_{OFF(NC)}$	$V_{CC} = 4.2V, V_{NO}$ or $V_{NC} = 3.3V/0.3V, V_{COM} = 0.3V/3V$	$-40^\circ C$ to $85^\circ C$	-	-	1	$\mu A$	
Channel On Leakage Current	$I_{NC(ON)}, I_{NO(ON)}, I_{COM(ON)}$	$V_{CC} = 4.2V, V_{NO}$ or $V_{NC} = 3V/0.3V, V_{COM} = 3V/0.3V, \text{ or floating}$	$-40^\circ C$ to $85^\circ C$	-	-	1		
<b>DIGITAL INPUTS</b>								
Input Logic High	$V_{IH}$	-	$-40^\circ C$ to $85^\circ C$	1.2	-	-	V	
Input Logic Low	$V_{IL}$	-	$-40^\circ C$ to $85^\circ C$	-	-	0.5		
IN Input Leakage Current	$I_{IN}$	$V_{CC} = 4.2V, V_{IN} = 0$ or $4.2V$	$-40^\circ C$ to $85^\circ C$	-	-	1	$\mu A$	
<b>DYNAMIC CHARACTERISTICS</b>								
Turn-On Time	$t_{ON}$	$V_{IH} = 4.2V, V_{IL} = 2.0V, R_L = 50\Omega, C_L = 35pF, \text{ See Test Circuit Figure 2.}$	$+25^\circ C$	-	13	-	ns	
Turn-Off Time	$t_{OFF}$		$+25^\circ C$	-	38	-	ns	
Break-Before-Make Delay	$t_D$	$V_{NO}$ or $V_{NC} = 1.5V, R_L = 50\Omega, C_L = 35pF, \text{ See Test Circuit Figure 3.}$	$+25^\circ C$	-	8	-	ns	
NC-NO and COM-NC/NO Off-Isolation	$O_{ISO}$	Signal = 0dBm, $V_{NO}$ or $V_{NC}$ centered between $V_{CC}$ and GND, $R_L = 50\Omega, \text{ See Test Circuit Figure 4 \& Figure 5.}$	100kHz	$+25^\circ C$	-	-83	-	dB
			1MHz	$+25^\circ C$	-	-61	-	
			10MHz	$+25^\circ C$	-	-40	-	
Channel-to-channel Crosstalk	$X_{TALK}$	$V_{BIAS} = 2.1V, V_{IN} = 0dBm, V_{IH} = 3V, V_{IL} = 0V, \text{ See Test Circuit Figure 6.}$	100kHz	$+25^\circ C$	-	-97	-	dB
			1MHz	$+25^\circ C$	-	-97	-	
			10MHz	$+25^\circ C$	-	-77	-	
3dB Bandwidth	$f_{3dB}$	$V_{BIAS} = 2.1V, V_{IN} = 0dBm, V_{IH} = 3V, V_{IL} = 0V. \text{ See Test Circuit Figure 7.}$	$+25^\circ C$	-	78	-	MHz	
Charge Injection Select Input to Common I/O	Q	$V_{IN} = GND, R_S = 0, C_L = 1nF, \text{ See Test Circuit Figure 8.}$	$+25^\circ C$	-	50	-	pC	
Off Capacitance	$C_{NC(OFF)}$	$f = 1MHz, \text{ See Test Circuit Figure 9}$	$+25^\circ C$	-	20	-	pF	
Off capacitance	$C_{NO(OFF)}$			-	20	-		
On Capacitance	$C_{ON}$			$f = 1MHz, \text{ See Test Circuit Figure 10}$	$+25^\circ C$	-		55
<b>POWER REQUIREMENTS</b>								
Power Supply Range	$V_{CC}$	-	$-40^\circ C$ to $85^\circ C$	1.8	-	4.2	V	
Power Supply Current	$I_{CC}$	$V_{CC} = 4.2V, V_{IN} = 0V$ or $V_{CC}$	$-40^\circ C$ to $85^\circ C$	-	-	1	$\mu A$	

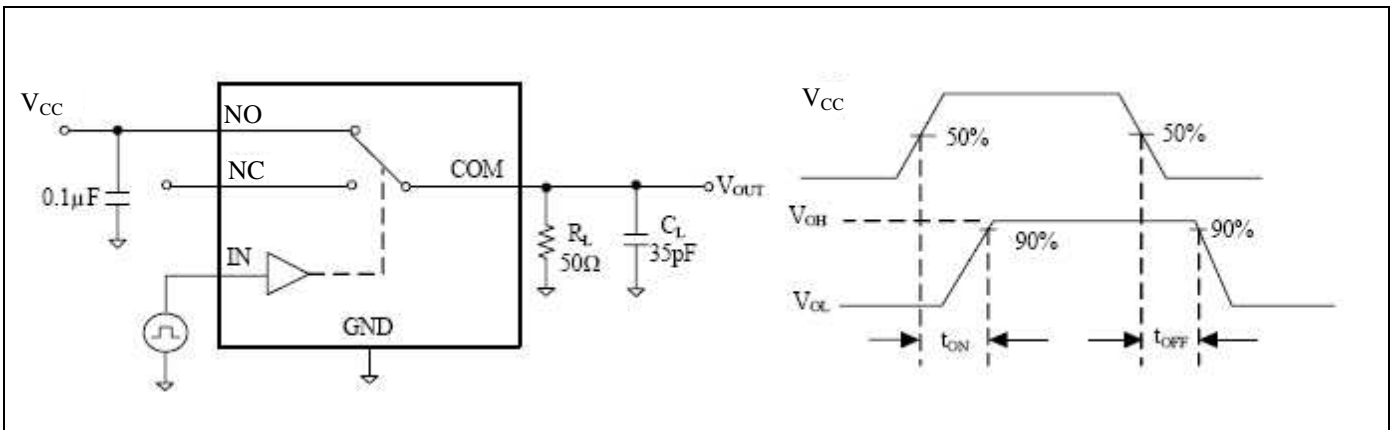
**Test Circuits and Timing Diagrams**



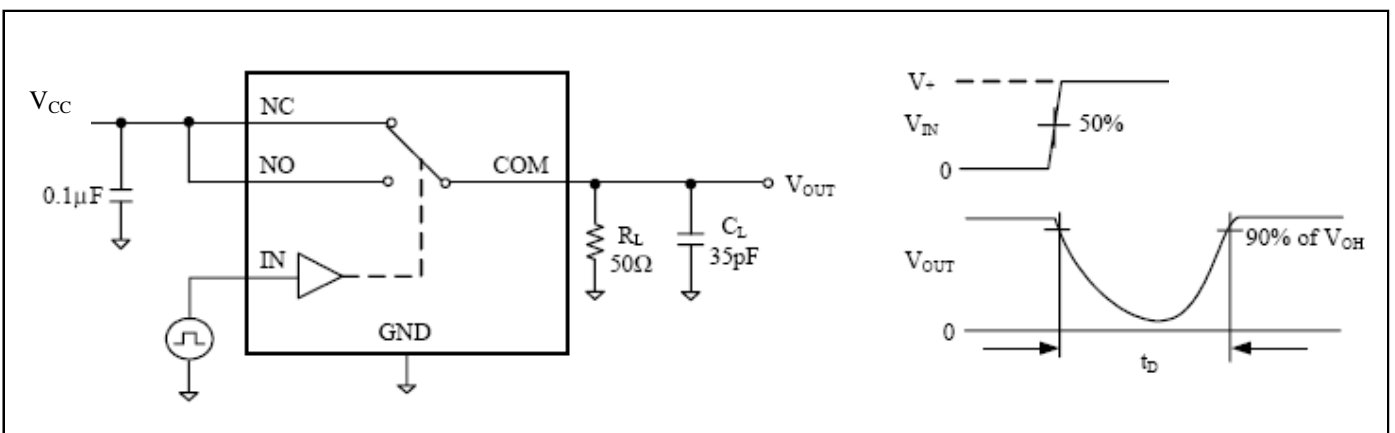
**Figure 1. On Resistance**

**Notes:**

1. Unused input (NC or NO) must be grounded.



**Figure 2. Switching Times**



**Figure 3. Break Before Make Interval Timing**

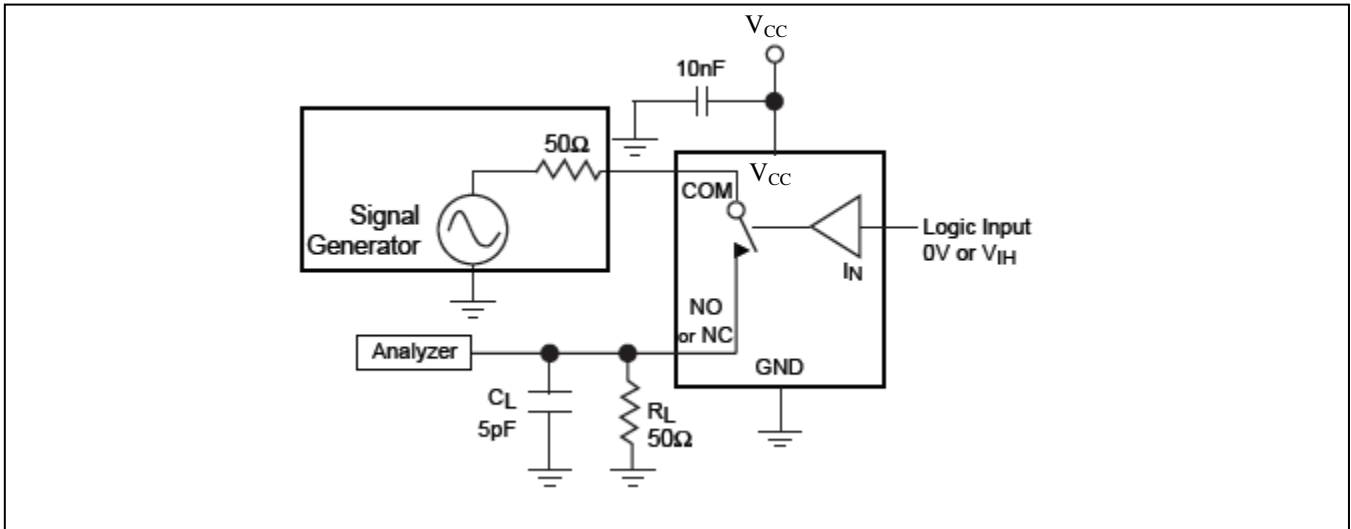


Figure 4. COM-NC/NO Isolation

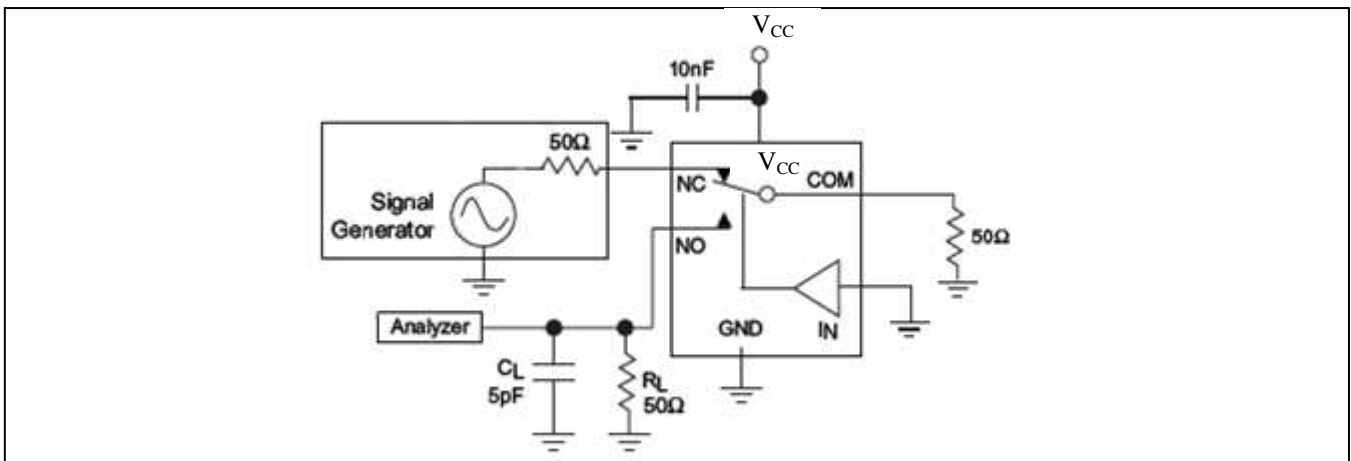
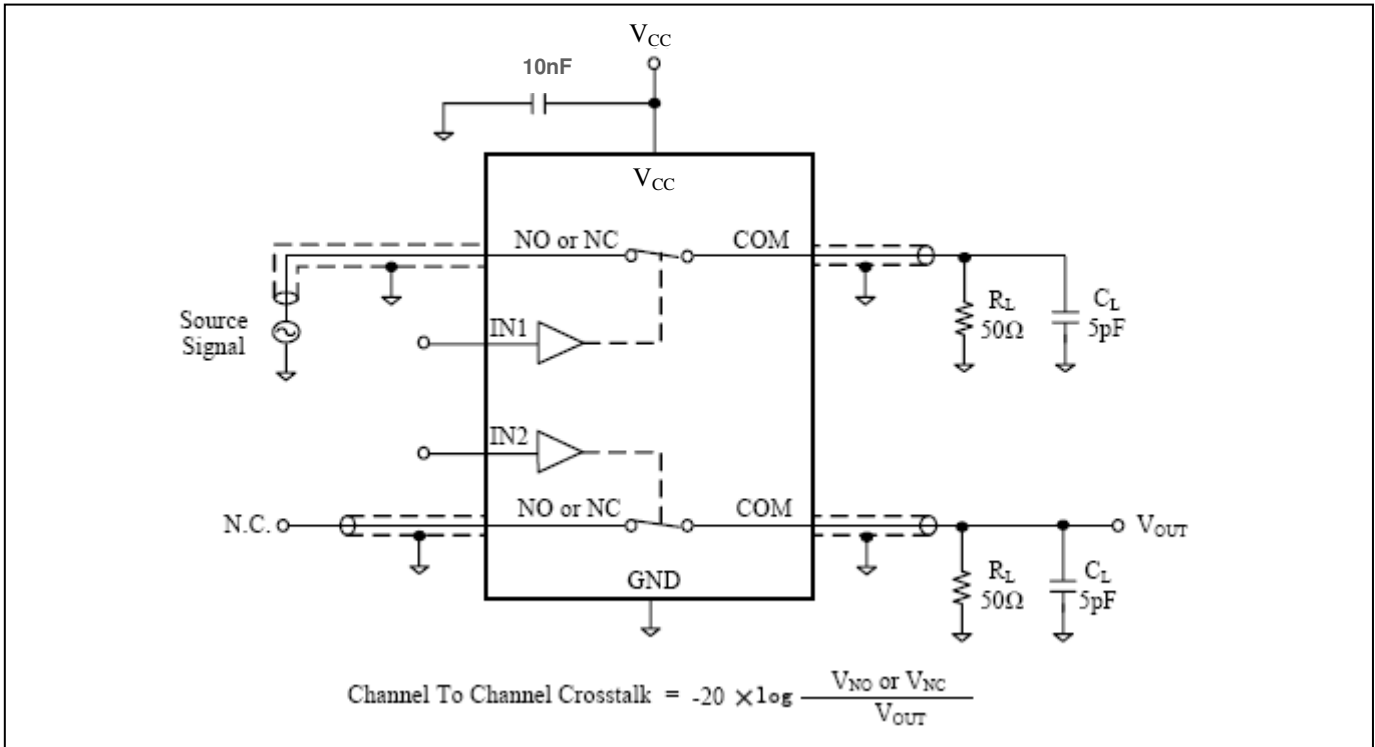
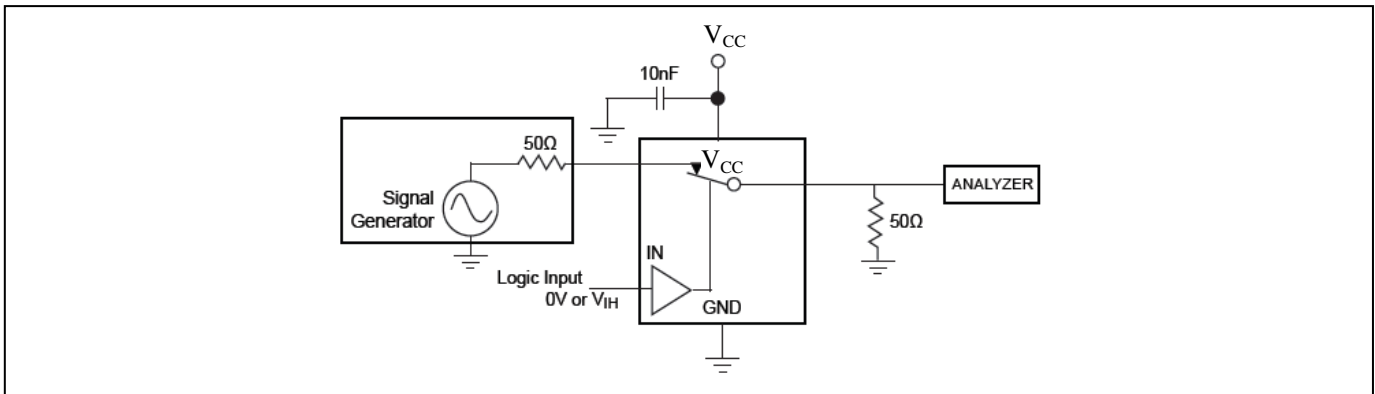


Figure 5. NC-NO Isolation





**Figure 6. Channel-to-Channel Crosstalk**



**Figure 7. Bandwidth**

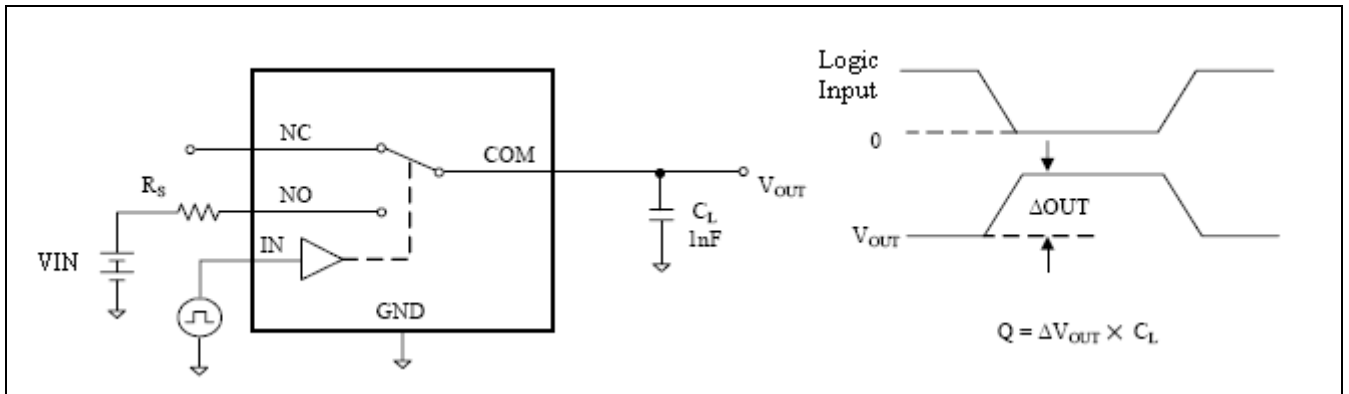


Figure 8. Charge Injection

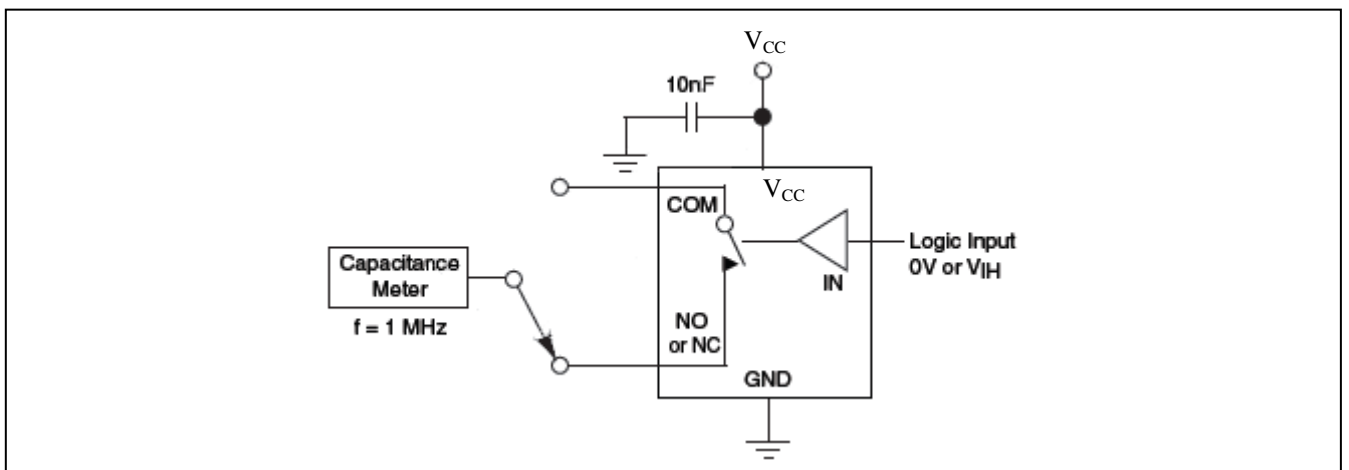


Figure 9. Channel Off Capacitance

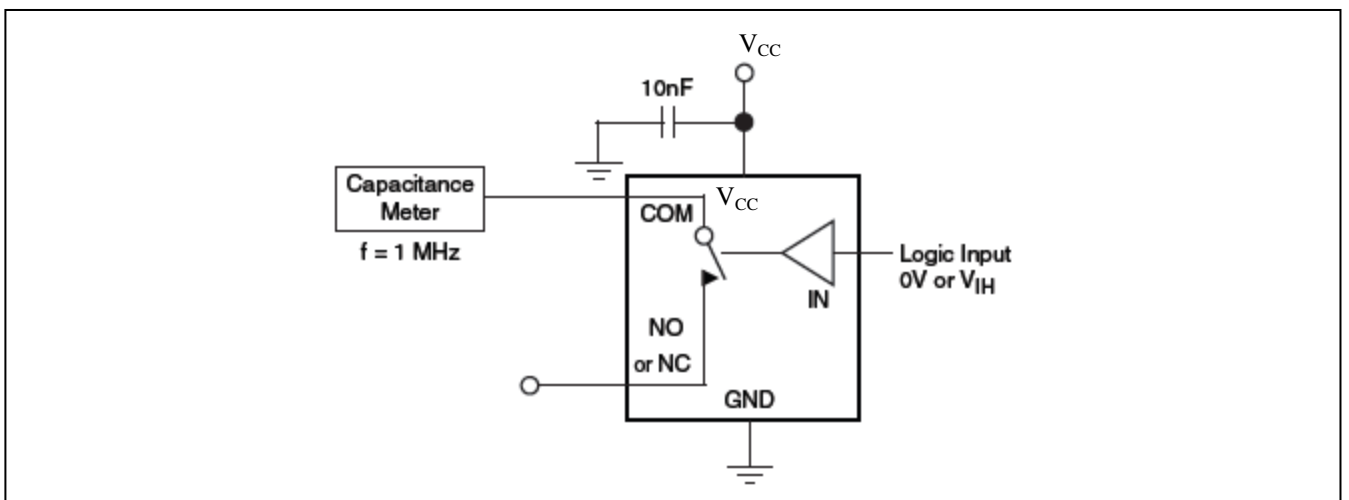
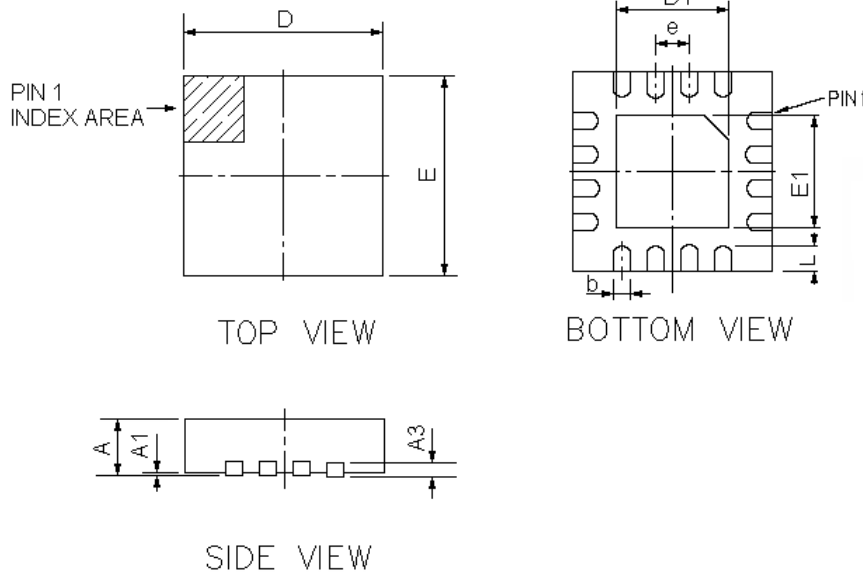


Figure 10. Channel On Capacitance

**Mechanical Information**
**16-pin TQFN (ZH16)**

DOCUMENT CONTROL NO. PD-0043
REVISION: A
DATE: 6/6/2012



PKG. DIMENSIONS(MM)		
SYMBOL	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	2.90	3.10
E	2.90	3.10
D1	1.60	1.80
E1	1.60	1.80
b	0.18	0.30
e	0.50 TYP	
L	0.30	0.50

**Note:**

1) Ref: JEDEC MO-220J

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 Shanghai,200233  
 Tel:(86-21)6485-0576. Fax: (86-21)6485-2181

**DESCRIPTION: 16 Pin, TQFN, 3X3**
**PACKAGE CODE: ZH16**
**Ordering Information**

Part Number	Packaging Code	Package
PI3A412ZHE	ZH	Lead Free and Green 16-pin TQFN

**Notes:**

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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