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A product Line of
Diodes Incorporated

PI3DPX1203B

DisplayPort 1.4 HBR3 Linear Redriver with Latency-Free, DP Transparent Link Training support

Description

PI3DPX1203B is the DisplayPort 1.4 compliant, up to 4 channel, 8.1 Gbps HBR3 Linear Redriver with Link Training transparency support. Displayport source-side and sink-side devices communicate through the AUX transaction between the source and the sink-side devices.

Input Equalization, Voltage Swing and Flat Gain control can be configured with pin-strapping or I2C programing to optimized Main Link high speed signals over a variety of physical medium by reducing inter-symbol interference. Pericom's Linear Redriver technology can deliver 2 times better additive jitters performance than traditional Redrivers.

Linear Equalizer always provide very flexible component placement, cascade connection and easy adjustment after the Redriver location changes during the product development events.

Features

- Compliant with VESA DisplayPort 1.4 specification up to 10 Gbps Link Rate
- Latency-free for the variable video frame rate support
- Dual mode DisplayPort support
- Linear Redriver allows flexible placement with DP Main Link boost setting
- Ideal for DP Alt Type-C Source and Sink-side application with PD Controllers with Aux Link Training Transparent Mode support
- Linear Equalizer increases Link Margin with Sink-side DFE (Decision Feedback Equalizer)
- Independent Main Link channel configuration for 4-bit Equalization, 2-bit Voltage Output swing and 2-bit Flat Gain control
- Pin strap or I2C programmable for device configuration setting
- Intra- and Inter-Channel Polarity Swap support
- I2C Address selectable for configuration register access
- Low Stand-by power consumption
- Power supply voltage: 3.3V

Applications

- Notebook, DeskTop, AIO PC
- Display, Monitors
- Active Adaptors, Dongles, Docking

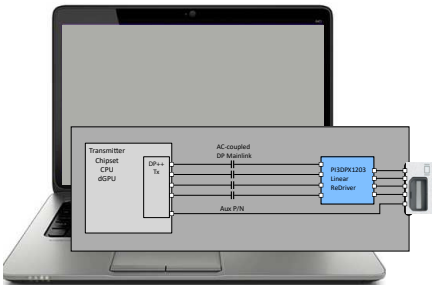


Figure 1-1 DP1.4 HBR3 Redriver in the NB PC

Ordering Information

Ordering Number	Package Code	Package Description
PI3DPX1203B ZLE(X)	ZL	Pb-free & Green 32-pin TQFN (3X6mm), Tray (Tape & Reel)
PI3DPX1203B ZHE(X)	ZH	Pb-free & Green 42-pin TQFN (3.5x9mm), Tray (Tape & Reel)
PI3DPX1203B ZHE -DRX	ZH	Pb-free & Green 42-pin TQFN (3.5x9mm), 16mm carrier Tape & Reel
PI3DPX1203B ZHIE(X)	ZH	Industrial Temperature, Pb-free & Green 42-pin TQFN, Tray (Tape & Reel)

Note: Suffix I = Industrial Temp, E = Pb-free and Green, X = Tape/Reel Type

2. General Information

2.1 Revision History

Revision	Description of Changes
Oct 2016	Ch2. 32-pin TQFN package added. Improve EQ , Stand-by power consumption from PI3DPX1203 DP1.4 Linear Redriver. Support I2C slave programming mode.
Feb 2017	Ch5. DP1.4 CTS compliance test report added
Mar 2017	Ch2. ZH42 pin-out typo fixed. Pin6, 12, 30 changed to NC. Ch4. No index Byte support Ch5. Gp, GF-gain, V1dB_4G typical value updated
May 2017	Ch5. power consumption; IDDQ = typ 0.2uA, max 1mA; IDD = typ 243mA, max =290mA. Ch5. Power-up timing diagram, PRSNT# application schematics added
Jun 2017	In 42-pin package, clarified NC and DNC pins
Jul 2017	Application reference schematic updated to support HPD IRQ
Dec 2017	Package marking added (p42).

2.2 Similar Products Comparison

	PI3DPX1203B	PI3DPX1203
Key Features	New silicon. Improved IDDQ = 0.2mA and IDD together. Optimized setting for the DP 1.4 application.	Old version. IDDQ = 2mA typ
Package Pin-out	Drop in compatible with PI3DPX1203 version	

2.3 Related Products

Part Numbers	Products Description
Retimers / Jitter Cleaner	
PI3HDX2711B	HDMI 2.0 and DP++ Retimer (Jitter Cleaner)
PI3HDX711B	HDMI 1.4 and DP++ ReTimer (Jitter Cleaner)
Redrivers	
PI3DPX1203B	DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type
PI3HDX1204B1	HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type
PI3HDX1204E	HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side
PI3DPX1207B	DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3DPX1202A	Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type
PI3HDX511F	High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type
Active Switches & Splitters	
PI3DPX1205A	DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3HDX231	HDMI 2.0 3:1 ports Mux Redriver, Linear-type
PI3HDX414	HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX412BD	HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX621	HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type

Contents

3. Pin Configuration

3.1 Package Pin-out

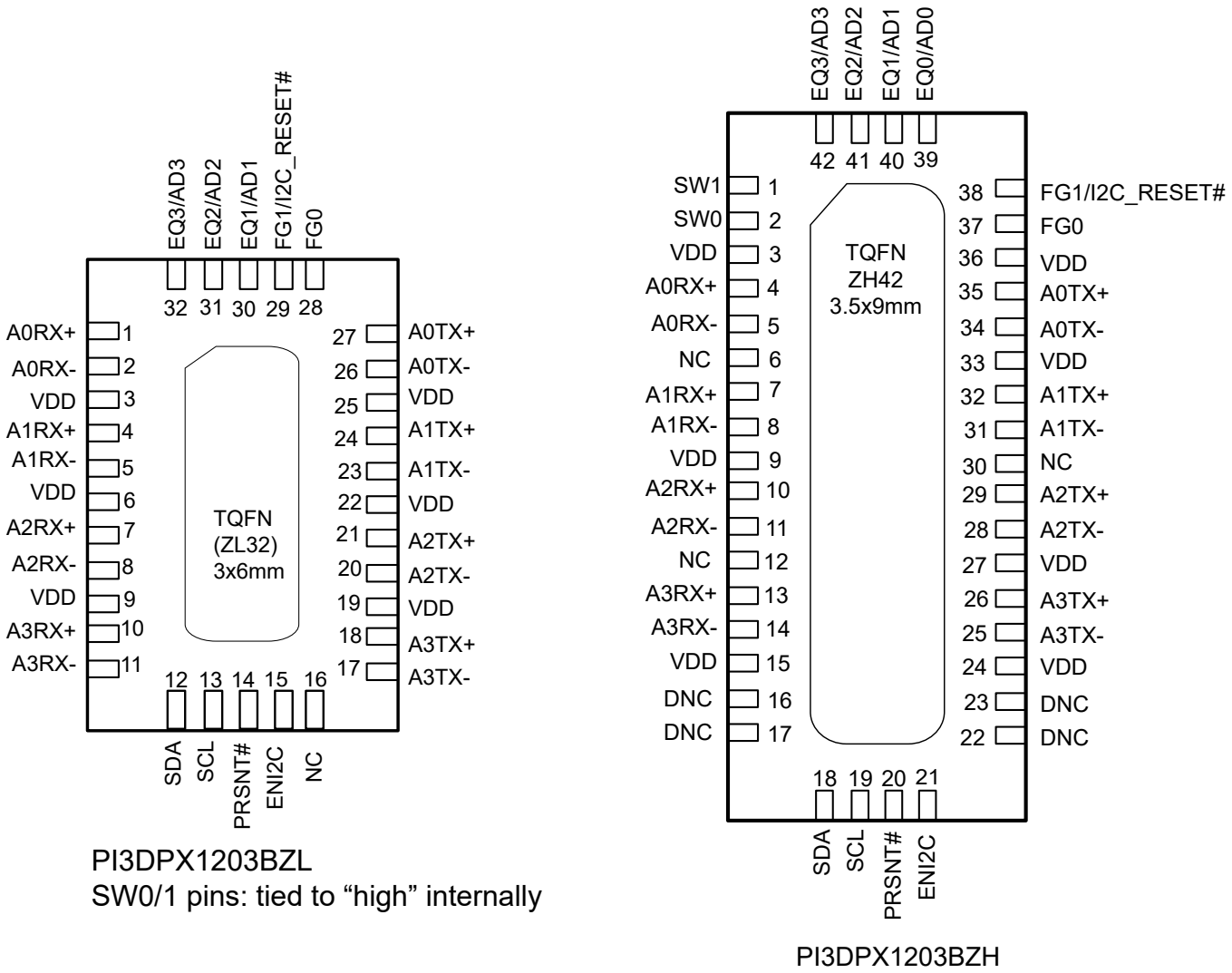


Figure 3-1 32/42-pin package pin-out

Note: The polarity (+/-) of each high speed pairs can use interchangeably. Output pins of polarity and data channel will always follow the input polarity and data channel assignment changes.

3.2 Pin Description

32-pin package

Pin #	Pin Name	Type	Description
Data Signals			
1 2	A0RX+ A0RX-	I	CML differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
27 26	A0TX+, A0TX-	O	CML differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
4 5	A1RX+, A1RX-	I	CML differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
24 23	A1TX+, A1TX-	O	CML differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7 8	A2RX+, A2RX-	I	CML differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
21 20	A2TX+, A2TX-	O	CML differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10 11	A3RX+, A3RX-	I	CML differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
18 17	A3TX+, A3TX-	O	CML differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
Control Signals			
12	SDA	I/O	I^2C Serial Data line
13	SCL	I/O	I^2C Serial Clock line
14	PRSNT#	I	Cable Present Detect input. This pin has internal 100KΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When Low, the device is enabled and in normal operation.
15	ENI2C	I	I2C Enable pin. Tied to VDD = Register access I2C Slave mode Tied to GND = Pin mode
32,31,30	EQ[3:1]	I	EQ Control pin. Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channels when ENI2C is low.
	AD[3:1]	I	Address bits control pins for I2C programming with internal 100kΩ pull-up.
29	FG1/I2C_RESET#	I	Shared pin for Gain Control bit-1 and I2C Reset pin. Inputs with internal 100kΩ pull up resistor. (1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low. (2) I2C Reset pin. Active Low to reset the registers to default state.
28	FG0	I	Flat Gain control bit-0 pin. Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
16	NC	NC	Not connect
Power Pins			
3,6,9,19,22,25	VDD	PWR	3.3V Power supply pins
Center Pad	GND	GND	Exposed Ground pad.

42-pin package

Pin #	Pin Name	Type	Description
Data Signals			
4 5	A0RX+ A0RX-	I	CML differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
35 34	A0TX+, A0TX-	O	CML differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7 8	A1RX+, A1RX-	I	CML differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
32 31	A1TX+, A1TX-	O	CML differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10 11	A2RX+, A2RX-	I	CML differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
29 28	A2TX+, A2TX-	O	CML differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
13 14	A3RX+, A3RX-	I	CML differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
26 25	A3TX+, A3TX-	O	CML differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
Control Signals			
19	SCL	I/O	I2C Serial Clock line
18	SDA	I/O	I2C Serial Data line
20	PRSNT#	I	Cable Present Detect input. This pin has internal 100KΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When Low, the device is enabled and in normal operation.
21	ENI2C	I	I2C Enable pin. Tie to VDD = Register access I2C Slave mode Tie to GND = Pin mode
39,40,41,42	EQ[3:0]	I	EQ Control pin. Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channel when ENI2C is LOW.
	AD[3:0]	I	I2C address bits control pins for programming with internal 100kΩ pull-up.
1,2	SW[1:0]	I	Output Swing control pins. Inputs with internal 100kΩ pull-up. This pin sets the output Voltage Level in all channel when ENI2C is LOW.
37	FG0	I	Gain Control pin bit 0 Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
38	FG1/I2C_RESET#	I	Shared pin for Flat Gain control bit-1 or I2C Reset pin. Inputs with internal 100kΩ pull up resistor. (1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low. (2) I2C Reset pin. Active Low to reset the registers to default state.

Pin #	Pin Name	Type	Description
6,12,30	NC		No Connect (Don't care) pin
16, 17, 22, 23	DNC		Do Not Connect pin
Power Pins			
3, 9, 15, 24, 27, 33, 36	VDD	PWR	3.3V Power Supply pins
Center Pad	GND	GND	Exposed Ground pad.

4. Functional Description

4.1 Functional Block Diagram

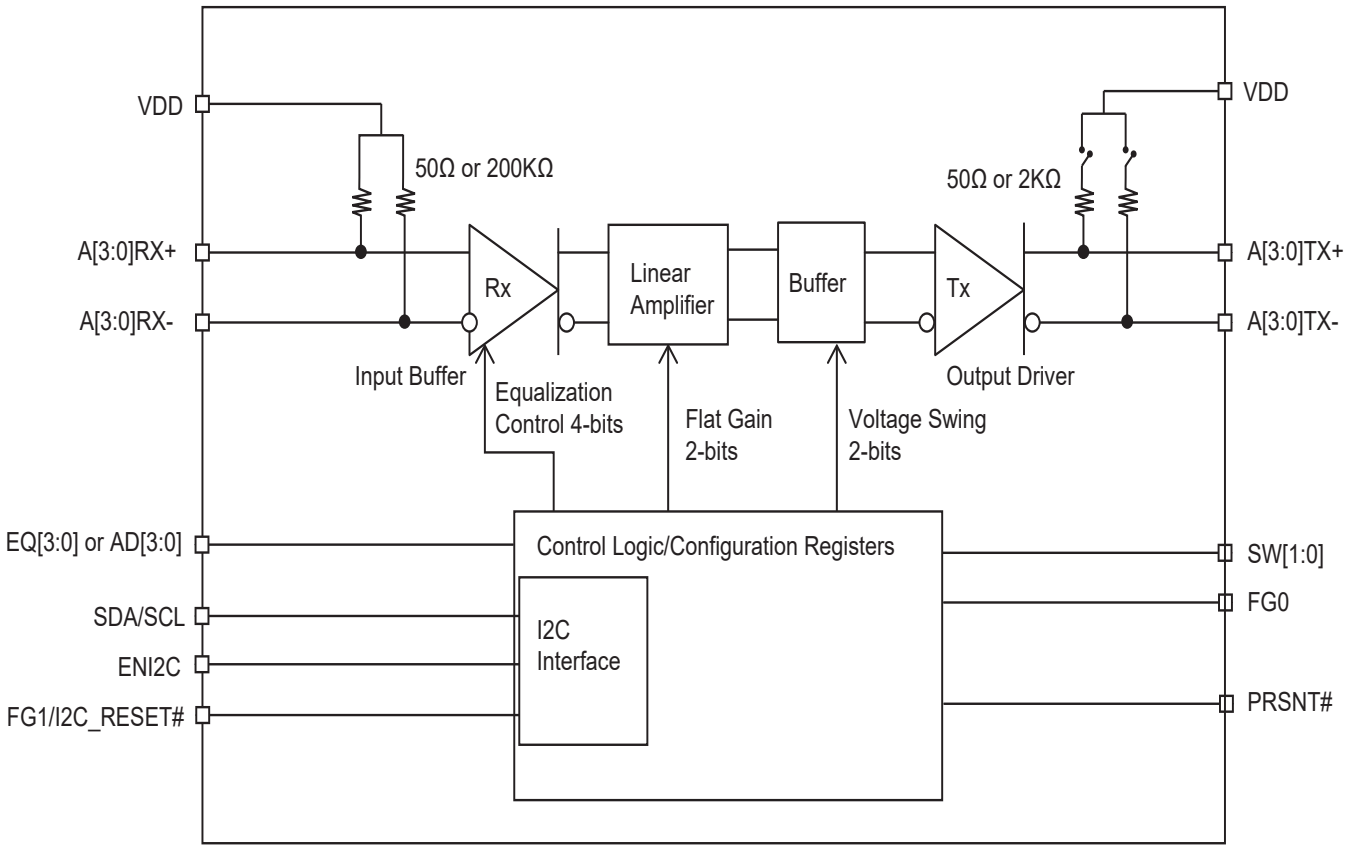


Figure 4-1 PI3DPX1203B Block Diagram

4.2 Power-Down Mode

Power Enable function: One pin control or I2C control, when PRSNT# is set to high, the IC goes into power down mode, both input and output termination set to 200K and high impedance respectively. Individual channel enabling is done through the I2C register programming.

PRSNT#	Description	Input Termination Resistor	Output Termination Resistor
H	Power-down mode. PRSNT# is internally pull-up 100 kΩ	200 kΩ pull-up	Hi-Z (2 kΩ pull-up)
L	Active Low for normal operation	50 Ω pull-up	50 Ω pull-up

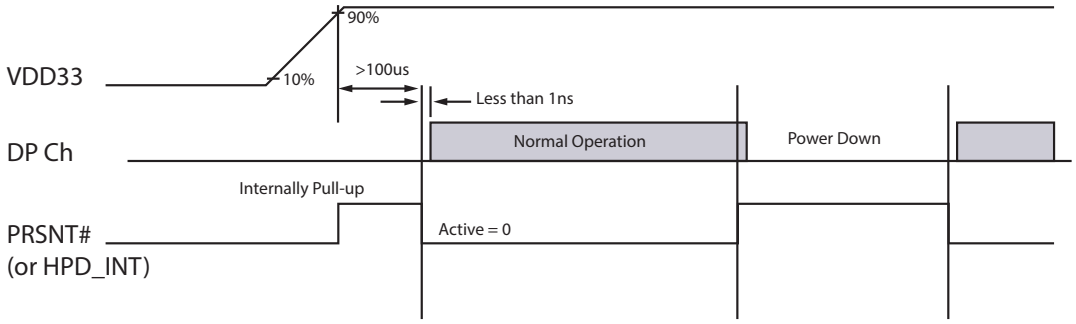


Figure 4-2 Power-up sequence recommendation

4.3 Flat Gain Setting

Flat Gain Control 2 bits FG[1:0] are the selection bits for the DC value.

Table 4-1. Flat Gain 2 bits Control Setting

FG1	FG0	Gain (dB)	Notes
0	0	-3.5	
0	1	-1.5	
1	0	0.5	Keep 0.5dB Gain setting for most application cases. Try other setting for the long cable/ transmission line when 0.5dB does not work.
1	1	2.5	

4.4 Output -1 dB Compression Setting

Swing Control 2 bits SW[1:0] control the linearity of the output voltage

Table 4-2. Output Swing -1dB Compression 2 bits Setting

SW1	SW0	mVppd @ 8 Gbps (Internally 100KΩ Pull-up)	Notes
0	0	920mV	Recommend setting for fixed DP swing like embedded DP
0	1	1040mV	
1	0	1280mV	DP spec max swing = 1.2Vdiff
1	1	1370mV	Reserved for the non-standard DP application

4.5 EQ Setting

Input EQ control 4 bits EQ[3:0] are the selection pins for the equalization selection for each Main Link channel.

Table 4-3. Input Equalizer 4 bits Setting

EQ3	EQ2	EQ1	EQ0	2.7 Gbps Input EQ(dB)	5.4 Gbps Input EQ(dB)	8 Gbps Input EQ(dB)
0	0	0	0	2.3	3.2	3.9
0	0	0	1	2.4	3.5	4.4
0	0	1	0	2.5	3.8	4.9
0	0	1	1	2.6	4.1	5.5
0	1	0	0	2.7	4.5	6.0
0	1	0	1	2.9	4.8	6.5
0	1	1	0	3.0	5.1	6.9
0	1	1	1	3.1	5.5	7.4
1	0	0	0	3.2	5.8	7.8
1	0	0	1	3.4	6.1	8.3
1	0	1	0	3.5	6.4	8.7
1	0	1	1	3.7	6.7	9.0
1	1	0	0	3.8	7.0	9.4
1	1	0	1	4.0	7.4	9.8
1	1	1	0	4.1	7.6	10.1
1	1	1	1	4.3	7.9	10.4

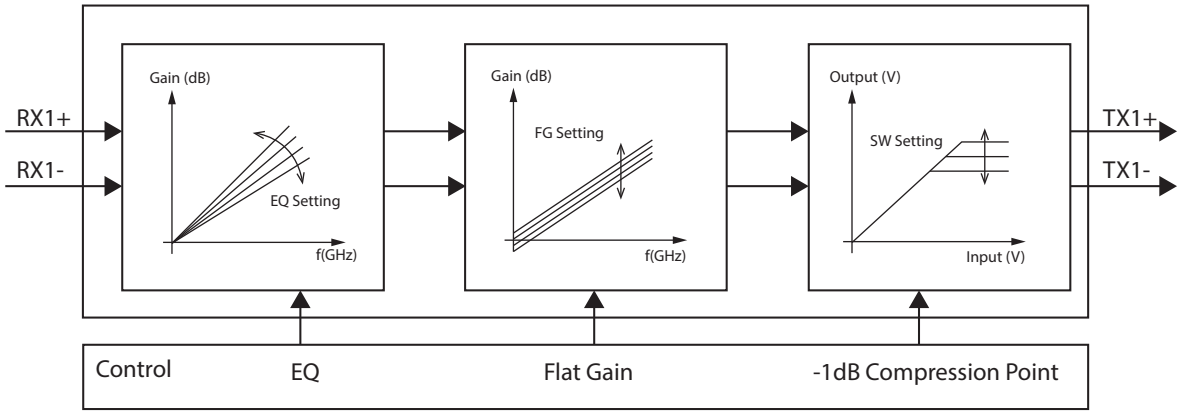


Figure 4-3 Illustration of EQ, Gain and -1dB Compression Point setting

5. I2C Programming

5.1 I2C Registers

Table 5-1. I2C Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	AD3	AD2	AD1	1 for ZL32 package AD0 for ZH42 package	1=R, 0=W

Table 5-2. I2C Programming Register definition

BYTE 0

Bit	Type	Power up condition	Description	Control affected	Comment
7:0	Reserved				

BYTE 1

Bit	Type	Power up condition	Description	Control affected	Comment
7:0	Reserved				

BYTE 2

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0		A3 Power down	1 = Power down
6	R/W	0		A2 Power down	
5	R/W	0		A1 Power down	
4	R/W	0		A0 Power down	
3	R/W	0	Reserved		
2	R/W	0			
1	R/W	0			
0	R/W	0			

BYTE 3

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 4

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 5

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 6

Bit	Type	Power up condition	Description	Control affected	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 7

Bit	Type	Power up condition	Description	Control affected	Comment
7:0	Reserved				

5.2 I2C Operation

The integrated I2C interface operates as a slave device mode. Standard I2C mode (100 Kbps) is supported with 7-bit addressing and data byte format 8-bit.
The device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A3 to A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.

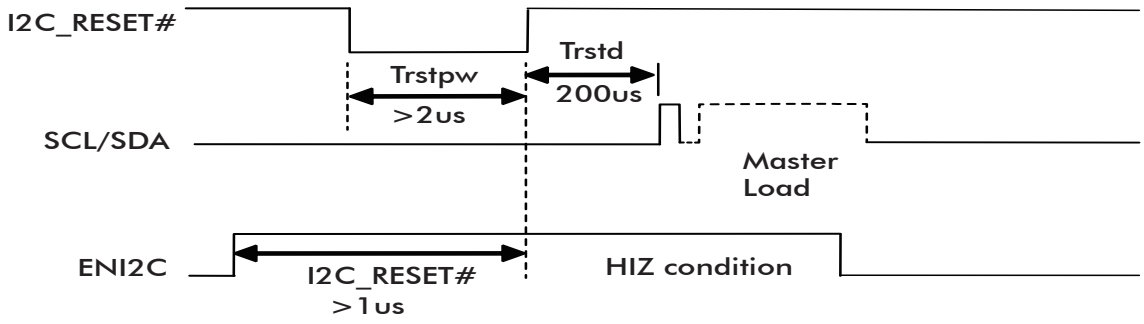


Figure 5-1 I2C Reset, Enable and SCL/SDA Timing Diagram

Transferring Data

Every byte put on the SDA line must be 8-bit long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). It will never hold the clock line SCL LOW to force the master into a wait state.

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first.

Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

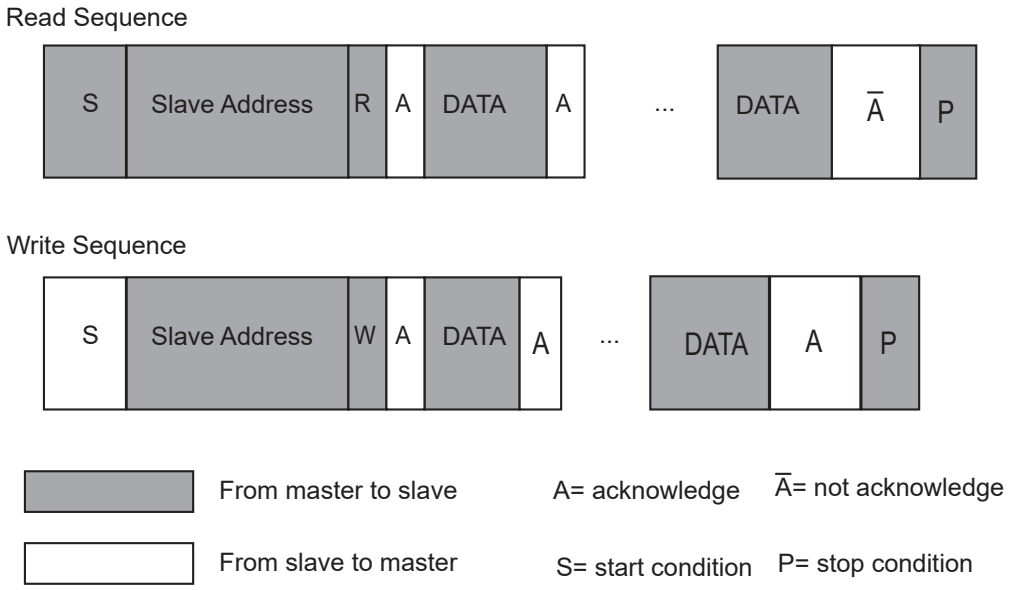


Figure 5-2 I2C Read / Write Timing Sequence

6. Electrical Specification

6.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5 V to +4.6 V
DC SIG Voltage ..... –0.5 V to +4.6 V
Output Current ..... –25 mA to +25 mA
Power Dissipation Continuous ..... 1.63 W
ESD, HBM ..... –2 kV to +2 kV
Storage Temperature ..... –65 °C to +150 °C
Maximum Junction temperature ..... 125 °C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Parameter		Min.	Typ.	Max	Units
Power supply voltage (VDD to GND)		3.0	3.3	3.6	V
Supply Noise Tolerance (from 100KHz to 10MHz)			100		mVp-p
Operating free-air temperature (TA)	Commercial Temperature	0		70	°C
	Industrial Temperature	-40(1)		85	°C

Note:
(1) I-temp is design guarantee, not production tested.

6.3 Power Consumption

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{DD}	Power supply voltage		3.0	3.3	3.6	V
I_{DD}	Operation power supply current	SW[1:0]=10 (1.2V_{DIFF} swing @8Gbps, 0dB pre-emphasis)		243	290	mA
I_{DDQ}	Standby power supply current	All other control pins are open. Disabled I2C master mode & I2C internal clock		0.2	1	mA

Note: Power consumption varies with the different Gain / Output Swing (-1dB Compression Point) setting.

Control Setting	Gain (dB)	Voltage Swing Limit (mV)	IDD(mA)
FG/SW=0000	-3.5	920	211
FG/SW=0001	-3.5	1040	228
FG/SW=0010	-3.5	1280	245
FG/SW=0100	-2.5	920	263
FG/SW=0101	-2.5	1040	228
FG/SW=0110	-2.5	1280	245
FG/SW=1000	+0.5	920	211

Control Setting	Gain (dB)	Voltage Swing limit (mV)	IDD(mA)
FG/SW=1000	+0.5	920	211
FG/SW=1001	+0.5	1040	223
FG/SW=1010	+0.5	1280	244
FG/SW=1100	+2.5	920	210
FG/SW=1101	+2.5	1040	226
FG/SW=1110	+2.5	1280	243

6.4 AC/DC Characteristics

6.4.1 LVCMOS I/O DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IH}	DC input logic HIGH		VDD/2 + 0.7		VDD + 0.3	V
V_{IL}	DC input logic LOW		-0.3		VDD/2 - 0.7	V
V_{OH}	At IOH = -200 µA		VDD + 0.2			V
V_{OL}	At IOL = -200 µA				0.2	V
V_{HYS}	Hysteresis of Schmitt trigger input		0.8			V

6.4.2 Main Link Differential

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC coupling capacitance			220		nF
S11	Input return loss(2)	10 MHz to 4.1 GHz differential		-13.0		dB
		1 GHz to 4.1 GHz common mode		-5.0		
S22	Output return loss(2)	10 MHz to 4.1 GHz differential		-15		dB
		1 GHz to 4.1 GHz common mode		-6.0		
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC single-ended output impedance			50		Ω
	DC Differential output Impedance			100		
Z_{RX-HIZ}	DC input impedance during reset or power down			200		kΩ
$V_{RX-DIFFp-p}$	Peak to peak differential input voltage	For HBR3		0.2(1)	1.2	Vppd
	Input Source common-mode noise	DC - 200MHz			150	mVpp
t_{PD}	Latency	From input to output		0.5		ns
G_P	Peaking gain: Compensation at 4 GHz, relative to 100 MHz, 100 mVp-p sine wave input	EQ[3:0] = 1111 EQ[3:0] = 1000 EQ[3:0] = 0000		10.4 7.8 3.9		dB
		Variation around typical	-3		+3	dB
G_{F-gain}	Flat gain: 100 MHz, EQ[3:0] = 1000, SW[1:0] = 10	FG[1:0] = 11 FG[1:0] = 10 FG[1:0] = 01 FG[1:0] = 00		+1.5 0.5 -1.5 -3.5		dB
		Variation around typical	-3		+3	dB
	Frequency Response Gain curve 1-5GHz with 18-inch FR4, FG=10		Pls refer the Freq/Gain curve below			dB

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{1dB_100M}	-1 dB compression point of output swing (at 100 MHz)	SW[1:0] = 11 SW[1:0] = 10 SW[1:0] = 01 SW[1:0] = 00			1370 1280 1040 920		mVppd
V_{Coup}	Channel isolation (Note 1)	100MHz to 4GHz			25		dB
V_{noise_input}	Input-referred noise	100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 0000			0.5		mV_{RMS}
		100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 1010			0.4		
V_{noise_output}	Output-referred noise (Note 2)	100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 0000			0.7		mV_{RMS}
		100MHz to 4GHz, FG<1:0> = 11, EQ<3:0> = 1010			0.8	1.6	
	Deterministic Jitter	Data Rate = 8Gbps FGx[1:0] = 10	EQ = 0000 EQ = 1010 EQ = 1111				UIp-p

Note:
(1) Channel Isolation measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
(2) Guaranteed by design and characterization.
(3) Please refer more data in the VIN / VOUT plot. VOUT changes withe EQ and FG setting. Both the ReDriver and the Sink device system should be carefully designed to ensure sink-device compliance.

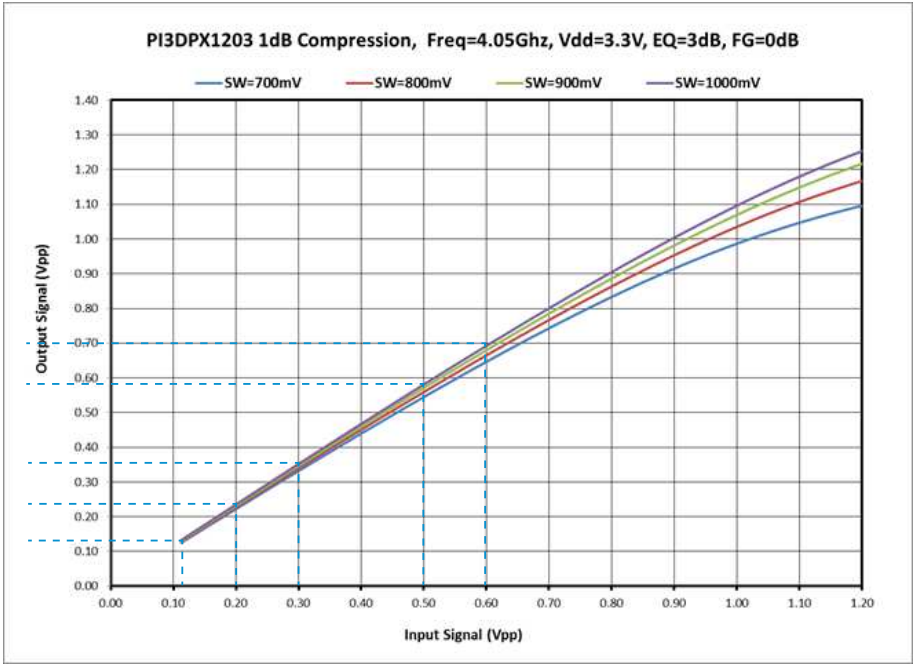


Figure 6-1 1dB Compression(Voltage Sweep) between 0 to 600mV Inputs @ 8Gbps

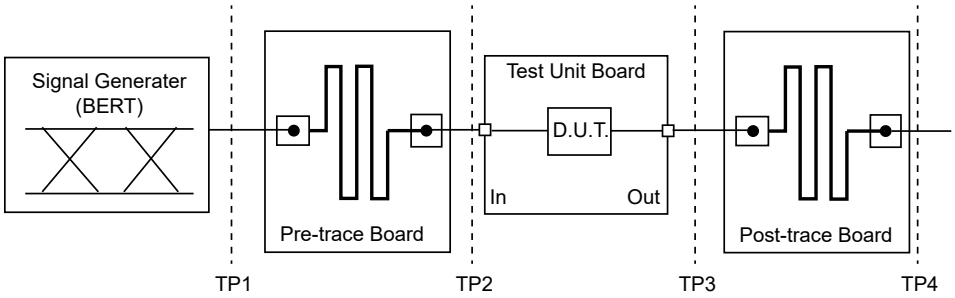


Figure 6-2 AC Electrical Measurement Test Setup

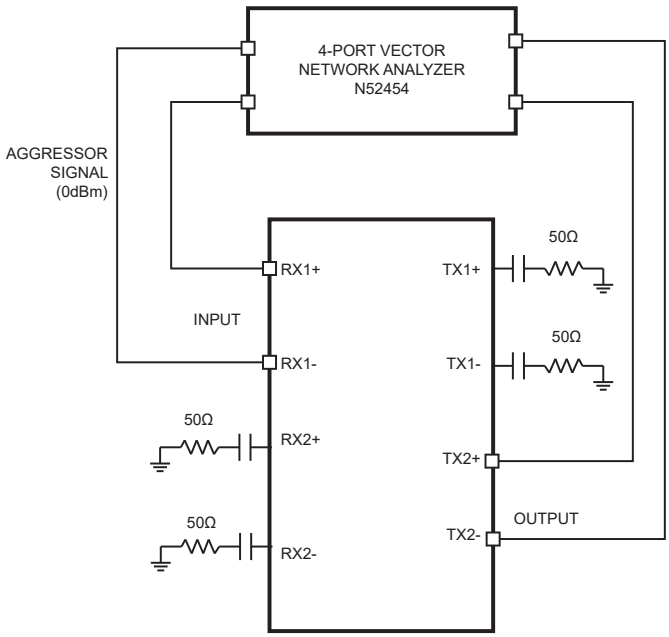


Figure 6-3 Channel-isolation test configuration

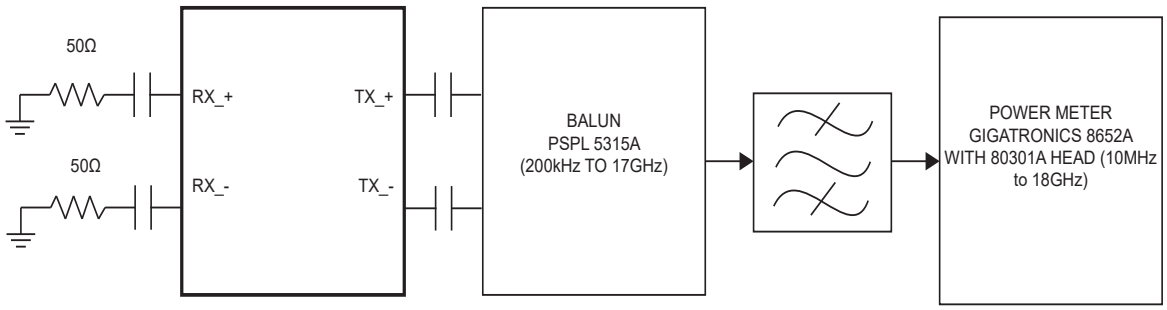
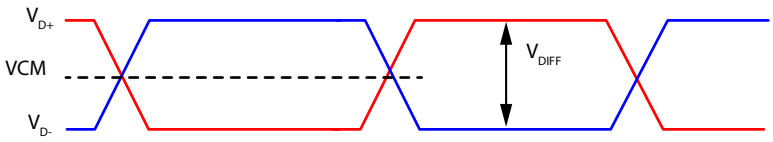


Figure 6-4 Noise test configuration

Common Mode Voltage
V_{CM} = (|VD+ + VD-| / 2)
V_{CMP} = (max |VD+ + VD-| / 2)



V_D + -V_D-

Symmetric Differential Swing
$V_{DIFFp-p}$ = (2 * max |V_{D+} - V_{D-}|)

Asymmetric Differential Swing
$V_{DIFFp-p}$ = (max |V_{D+} - V_{D-}| {V_{D+} > V_{D-}}
+ max |V_{D+} - V_{D-}| {V_{D+} < V_{D-}})

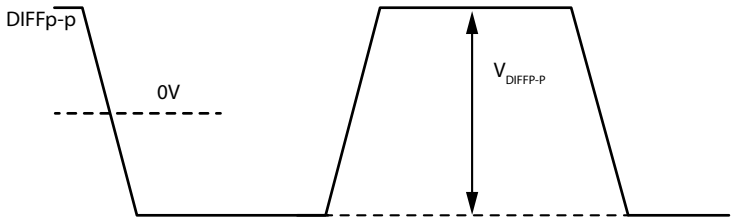


Figure 6-5 Definition of Differential Voltage and Differential Voltage Peak-to-Peak

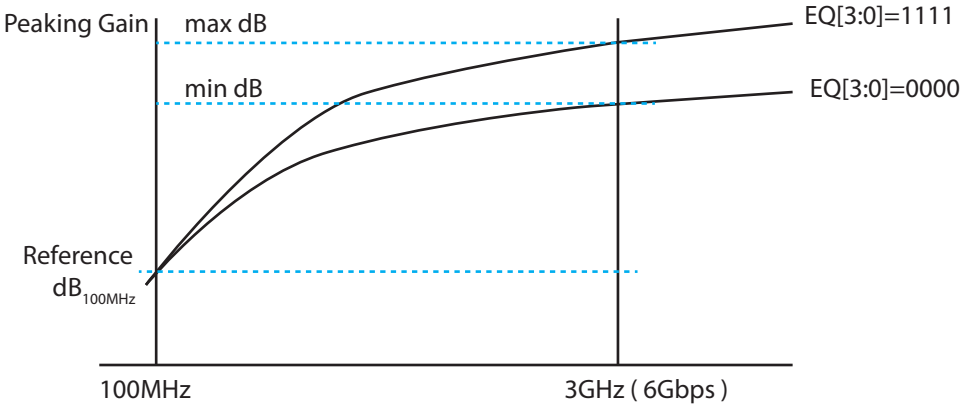


Figure 6-6 Definition of Peaking Gain relative to 100 MHz, 100 mVp-p sine wave input

6.4.3 SCL/SDA Specification for I2C BUS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
SDA and SCL I/O for I2C-bus						
V_{DD}	Nominal Bus Voltage		3.0		3.6	V
V_{IH}	DC input logic HIGH		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic LOW		-0.3		$V_{DD}/2 - 0.7$	V
V_{OL}	DC output logic LOW	I_{OL} = 3mA			0.4	V
t_{OF}	Output fall time from VIHmin to VIL-max with bus cap. 10-400pF				250	ns
AC/DC Specifications - SCL/SDA for I2C BUS						
I_{PU}	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
$I_{leak-bus}$	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
f_{SCLK}	Bus Operation Frequency			100		KHz
tBUF	"Bus Free Time Between Stop and Start condition"		1.3			us
tHD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
tSU:STA	Repeated start condition setup time		0.6			us
tSU:STO	Stop condition setup time		0.6			us
tHD:DAT	Data hold time		0			ns
tSU:DAT	Data setup time		100			ns
tLOW	Clock Low period		1.3			us
tHIGH	Clock High period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	"Time in which a device must be operation after power-on reset"				500	ms

Note:
(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) Ensured by Design. Parameter not tested in production.

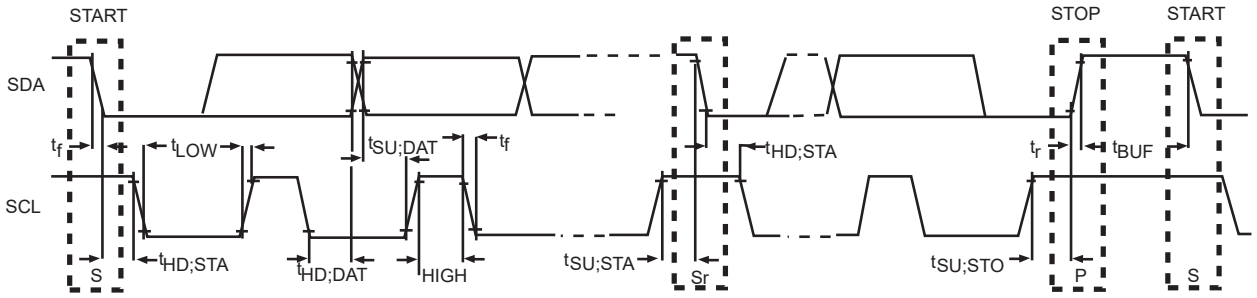
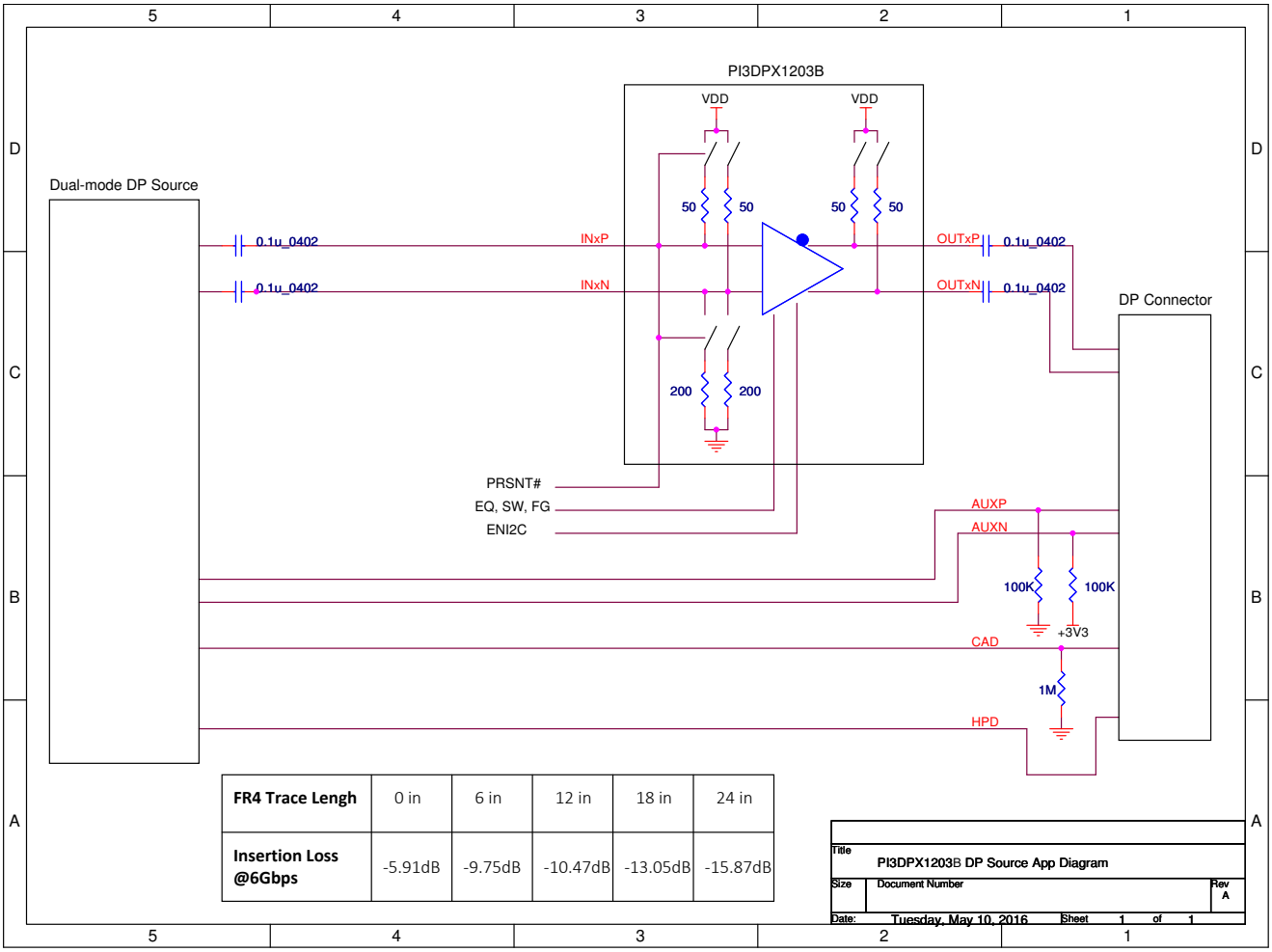


Figure 6-7 I²C Timing Diagram

7. Applications

7.1 Reference Schematic

- Determine the loss profile between transmitter and receiver.
- Based upon the loss profile and signal swing, determine the optimal equalization settings.
- Select appropriate voltage output swing.
- If required, select the correct differential pair polarity.
- To set voltage logic levels on configuration pins, use a 5-kΩ pull-up for high level, tie pin to GND for low level,and place a 5-kΩ pull-up and 5-kΩ pull-down for HiZ.



FR4 Trace Lengh	0 in	6 in	12 in	18 in	24 in
Insertion Loss @6Gbps	-5.91dB	-9.75dB	-10.47dB	-13.05dB	-15.87dB

Figure 7-1 Source side DP Redriver Connection Diagram