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A product Line of
Diodes Incorporated

PI3DPX1207B

DP-Alt DP1.4/USB3.1 10Gbps Linear Redriver with Non-Blocking, Latency-Free and built-in Aux Switch

Description

PI3DPX1207B is the DP-Alt 1.4 (Max 10Gbps) Linear Redriver. DP1.4 standard can support 4K2K@120Hz / 25.82 Gbps with 4-channels.

Each of the DP1.4 and USB3.1 Gen2 differential signals can be easily adjustable with equalization, output swing and gain adjustment by either pin or I2C control settings. It can optimize the DP/USB 10Gbps signal performance over a variety of physical mediums by reducing Inter-symbol interference jitters.

Non-blocking linear Redriver can provides 2x better additive jitter performance than the conventional CMOS-based Redriver. Since Linear Redriver does not block the Receiver DFE's adaptive channel controls, it can natively support DisplayPort Transparent LT(Link Training) without any dependency of the DP-Aux channels listener.

Named as "Trace Loss Canceling" technology, and supports the cascading high speed link connections between Host and Device. It means multiple linear Redriver can be placed in the link to work seamlessly to compensate high insertion loss.

The Cascading, Low Jitter and Simplicity of Gain adjustment capabilities to extend signal transmission features are ideal choice for the 8-10Gbps high speed DP Alt signal integrity solutions.

Features

- DP-Alt 4-channel Redriver and DeMux (DP 2-ch and USB 2-ch)
- Latency-free USB Read/Write Transfer rate and DisplayPort Redriver Link Training for variable video frame rate control
- DP1.4 (8.1 Gbps) and USB3.1 Gen 2 (10 Gbps) standard compliant
- Type-C DP/USB mode selection: DP only, USB only, DP/USB split modes
- Natively support Transparent DisplayPort Link training with Non-blocking No-latency Linear ReDriver
- Independently controlled EQ/Gain/Swing signal outputs for DisplayPort and USB modes
- Type-C Plug and Aux Flipping controls through I2C slave pins
- Slave I2C support only. I2C speed up to 1MHz
- Auto power saving circuit
- Single Power Supply: 3.3V

Applications

- Notebook, Desktop and AIO personal computers
- DP-Alt Monitors and Displays
- Active DP-Alt Cables/Adapters

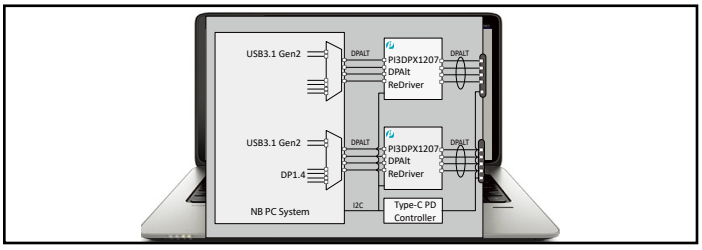


Figure 1-1 Type-C Connector inside PCs

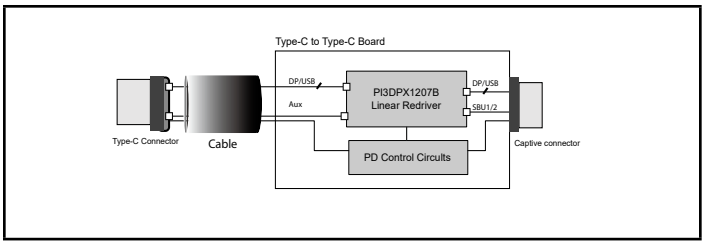


Figure 1-2 DP-Alt to DP Active Cables

Ordering Information

Ordering Number	Package Code	Package Description
PI3DPX1207BZHEX	ZH	42-pin, Very Thin Quad Flat No-Lead (TQFN) (3.5x9mm)

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.

2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/

3. E = Pb-free and Green

4. X suffix = Tape/Reel

2. General Information

2.1 Revision History

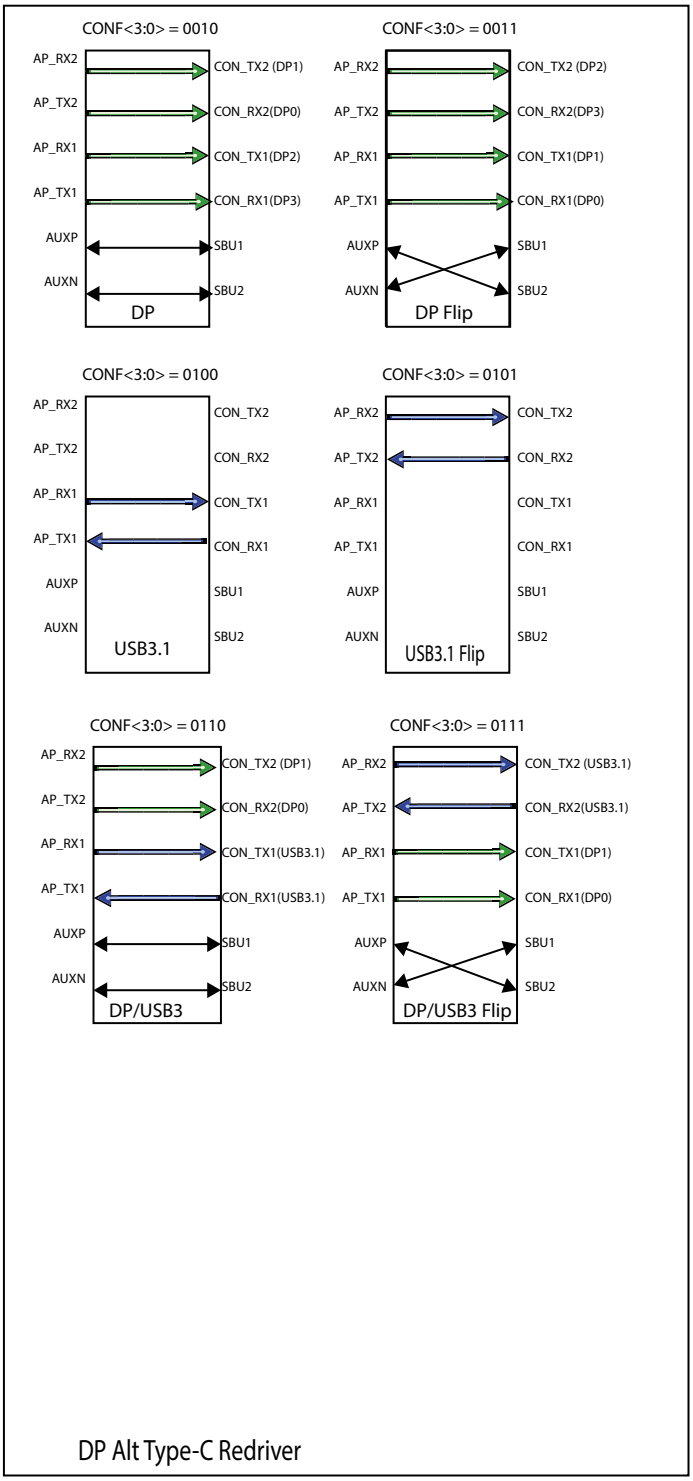
Revision	Description of Changes
Jul 2016	Preliminary Datasheet release.
Aug 2016	Low-power mode, ePad Via, Default register values added.
Oct 2016	Ch 4. $V_{in\text{-}Diff}$ 400mV to Typ changed. Add more clarification in Pin Description and Block Diagram.
Nov 2016	Ch 4. AC/DC electrical parameters and output eye added. Removed Generic mode. Pls contact Diodes for Generic mode application usage.
Dec 2016	Ch 4. Power consumption max added. Ch 5. PCB routing information, CTS report added. Add Sample Errata and disclaimer
Jan 2017	Ch5. DP1.4 CTS test report added.
May 2017	Ch3. 4-bit EQ and FG setting change for high speed Eye signal optimization. Related register spec updated Ch5. USB compliance report added.
Aug 2017	Application reference schematic changed for Aux & SBU1/2 connection. SiGe BiCmos Redriver Jitter performance Benchmark data added in Application session. Power down current max IPD increase 100uA from 66uA. Aux listener features and DP low power D3 mode removed.
Nov 2017	USB3.2, PCIeG3, TMDS modes added for special usage. EC / PD / TCPC programming guide(p51). Due to the Intel's new requirement on the TX impedance when Power-on and Receiver detect phase. All TX 4kOhm impedance changed from 4kOhm to 4.5kOhm (p9, p11,p17)
Mar 2018	AUXSBU2, 18 pin; AUXSBU1, 19 pin Page 46, EN and IN_HPD are reversed.
Apr 2018	Updated 2.3 Diagram
May 2018	Remove Industrial Temp Ordering Information, Remove PI3DPX1207D from Section 2.2; Remove PI3HDX711B and PI3HDX2711B from Section 2.4

2.2 Family Products Comparison

	PI3DPX1207B	PI3DPX1205A
General Features	Type-C DisplayPort Alt Redriver USB / DP Latency-Free	Type-C DisplayPort Alt Active Mux USB / DP Latency-Free
Max Data Rate	10Gbps	10Gbps
Package	42-pin TQFN (3.5x9mm)	40-pin TQFN(4x6mm)
NEXT Crosstalk	Very good, -45dB at 5GHz	Very good, -45dB at 5GHz
Package Pin-out	Place 2 pins space between 10Gbps Data channels TX0/1, RX0/1 to reduce Crosstalk	Place 2 pins space between 10Gbps Data channels TX0/1, RX0/1 to reduce Crosstalk
Control modes	I2C or Pin-mode	I2C mode control
Power supply	3.3V	3.3V

2.3 PI3DPX1207 Redriver Switching Preset modes

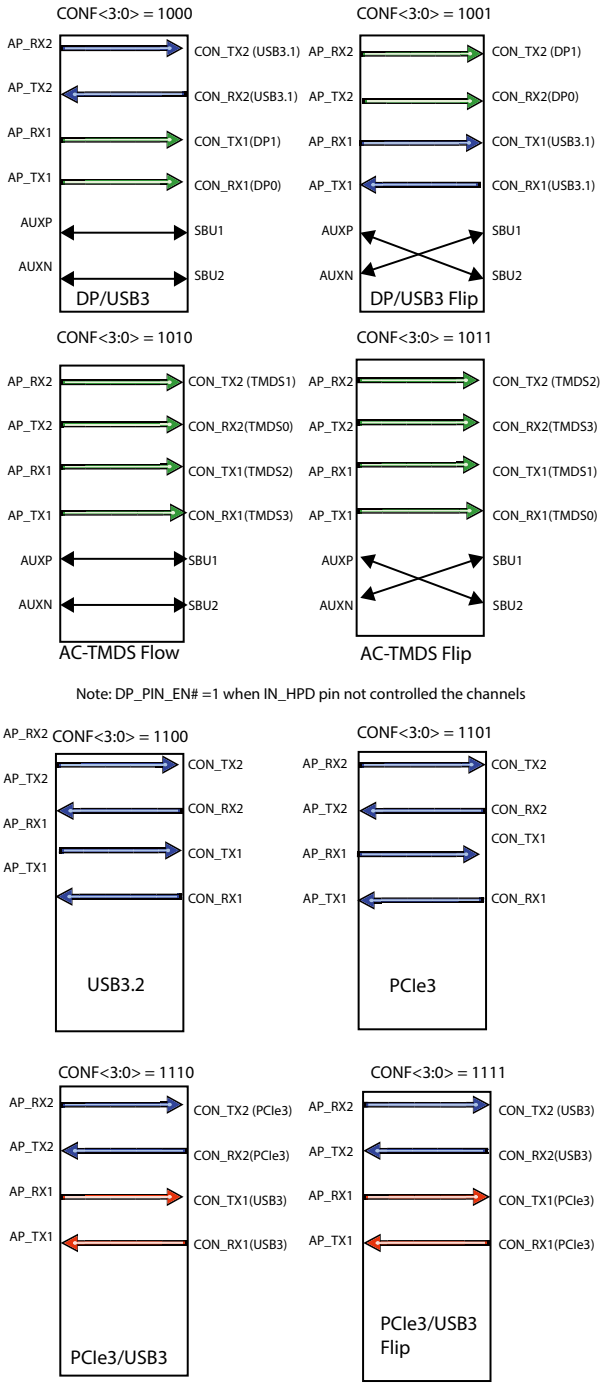
Preset mode with pin-strap (or I2C control)



DP Alt Type-C Redriver

Preset mode supporting with I2C control

CONF<3> bit controlled by I2C. Default CONF<3> = 0



USB3.2 and PCIe3 , AC-TMDS Redriver Modes

2.4 Other Related Products

Part Numbers	Products Description
Redrivers	
PI3DPX1203B	DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type
PI3HDX1204B1	HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type
PI3HDX1204E	HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side
PI3DPX1207B	DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3DPX1202A	Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type
PI3HDX511F	High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type
Active Switches & Splitters	
PI3DPX1205A	DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3HDX231	HDMI 2.0 3:1 ports Mux Redriver, Linear-type
PI3HDX414	HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX412BD	HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX621	HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type

Contents

3. Pin Configuration

3.1 Package Pin-out

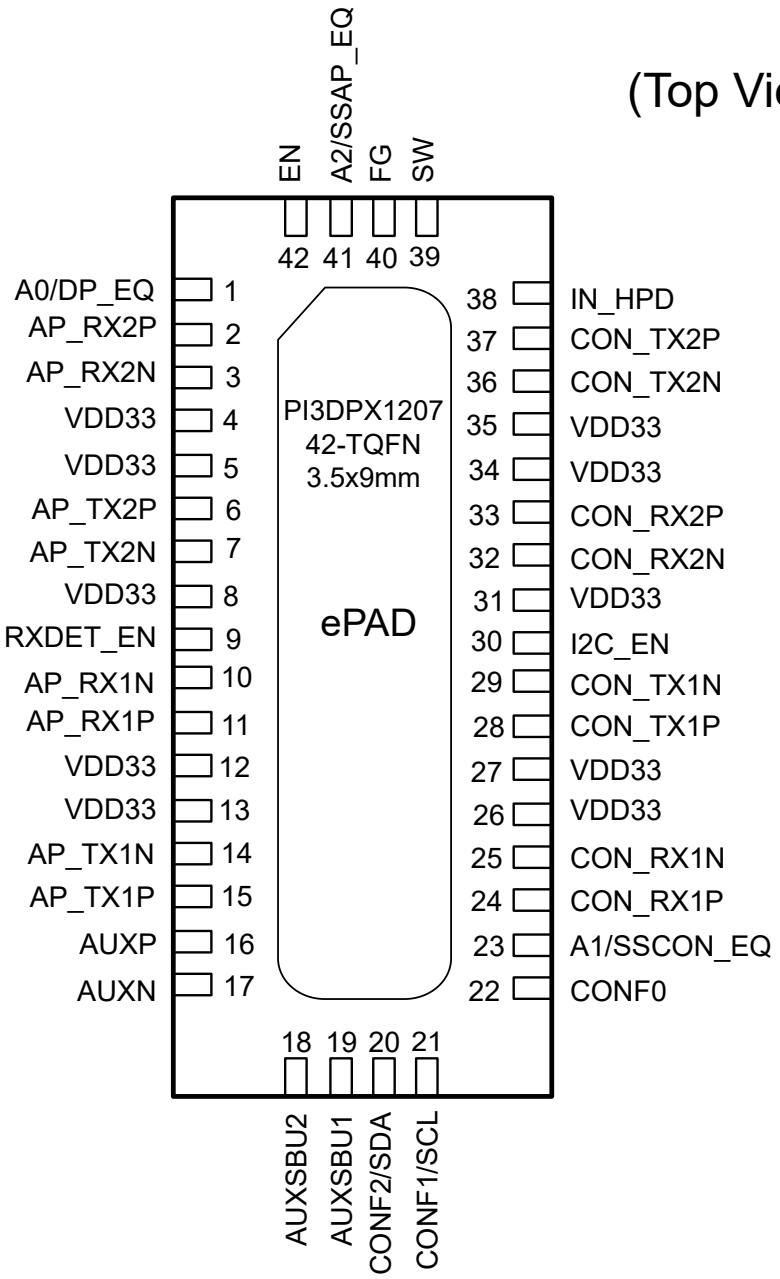


Figure 3-1 42-TQFN package pin-out (PI3DPX1207B)

3.2 Pin Description

Pin Name	Pin #	Type	Description
CON_RX1N/P	25,24	I/O	Type-C receptacle RX/TX Channel CML input/output With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
CON_RX2P/N	33,32	I/O	Type-C receptacle RX/TX Channel CML input/output With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
CON_TX2P/N	37,36	O	CML output terminals. With selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VbiasTx or Hi-Z
CON_TX1N/P	29,28	O	CML output terminals. With selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VbiasTx or Hi-Z
AP_RX2P/N	2,3	I	CML input terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
AP_RX1N/P	10,11	I	CML input terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
AP_TX2P/N	6,7	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
AP_TX1N/P	14,15	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
A0/DP_EQ	1	I	For pin control mode (I2C_EN=Low) DP Application processor side: The equalization selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
			For I2C control mode (I2C_EN=High). I2C address select. 2-level input pins. Internal 200kΩ pull-down resistor.
RXDET_EN	9	I	Receiver detect enable mode. With internal 300kΩ pull-up resistor. “Low”: Disabled “High”: Enabled (Default)
AUXP/N	16, 17	I/O	Host AP/UFP-side DisplayPort Aux Channel, connected to Source
AUXSBU2 AUXSBU1	18, 19	I/O	Connector/DFP Low Speed Signal Port. Side band use

Pin Name	Pin #	Type	Description
CONF2/SDA	20	I/O	For Pin control mode with internal 300kΩ pull-down resistor (I2C_EN=Low). CONF2 is the selection pin for the channel mode assignment and flip control
			For I2C control mode (I2C_EN=High). SDA is I2C control bus data. Open drain structure.
CONF1/SCL	21	I	For Pin control mode with internal 300kΩ pull-down resistor (I2C_EN=Low). CONF1 is the selection pin for the channel mode assignment and flip control
			For I2C control mode (I2C_EN=High) SCL is I2C control clock. Open drain structure.
CONF0	22	I	For Pin control mode (I2C_EN=Low) CONF0 is the selection pin for the channel mode assignment and flip control. 300kΩ pull-down resistor.
A1/SSCON_EQ	23	I	For pin control mode (I2C_EN=Low) USB Type-C connector side. The equalization selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
			For I2C control mode (I2C_EN=High) The I2C address select. 2-level input pins. With internal 200kΩ pull-down resistor.
I2C_EN	30	I	I2C enable control. With internal 300kΩ pull-up resistor. “Low”: Pin control is selected “High”: I2C control is selected (Default)
IN_HPD	38	I	Hot plug detection from Sink. With internal 300kΩ pull-down resistor.
SW	39	I	For pin control mode (I2C_EN=Low) DP Type-C Connector side: The -1dB linear swing selection. 2-level input pins. With internal 300kΩ pull-up resistor.
FG	40	I	For pin control mode (I2C_EN=Low) The flat selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
A2/SSAP_EQ	41	I	For pin control mode (I2C_EN=Low) USB Application Process side: The equalization selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
			For I2C control mode (I2C_EN=High) The I2C address select. 2-level input pins. With internal 200kΩ pull-down resistor.
EN	42	I	Chip Enable. With internal 300kΩ pull-up resistor. “Low”: Chip Power Down “High”: Normal Operation (Default)
VDD33	4,5 8, 12 13, 26 27,31 34,35	P	3.3V Power Supply
ePAD	ePAD	G	ePAD for the Ground

4. Functional Description

4.1 Product Feature Details

General Features

- ➔ DP-Alt HBR3 8.1Gbps mode and USB3.1 10Gbps Type-C application
- ➔ Flexible DP-Alt mode switching between USB3.1 Gen2 and DP 8.1Gbps
- ➔ Ultra Low standby power with auto power saving for the DisplayPort and USB mode
- ➔ Selectable adjustment of receiver Equalization, Flat gain, -1dB compression linear output swing
- ➔ Built-in control logic for Type-C plug/unplug normal and flipping orientations
- ➔ Active Linear ReDriving for signal integrity
- ➔ Except the EN pin, I2C_EN, I2C address pins, IN_HPD and I2C I/O pins, all other pin setting will be ignored in the I2C mode.
- ➔ Slave I2C only. I2C speed up to 1MHz
- ➔ The I2C I/O buffer supports the 1.8V/3.3V signal condition
- ➔ IN_HPD could be selected as active high or active low by I2C mode (byte4 [1])
- ➔ Single power supply 3.3±0.3V

DisplayPort 1.4

- ➔ DP LT-transparent through linear Redriver design
- ➔ Hot Plug Detect

USB 3.1 Gen 2

- ➔ Selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
- ➔ Selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VbiasTx or Hi-Z with receiver termination detection.
- ➔ Possible operation modes: PD, Unplug, deep slumber mode, slumber mode and active mode.
- ➔ Receives and transmits the signal in unplug, deep slumber mode and active mode.
- ➔ Active mode: The channel is always ready to transmit. No Ton/Toff due to the signal detector in this mode.
- ➔ Slumber mode, Deep slumber mode and Unplug mode: The channel is partially/fully off due to the power saving. Signal detector is monitoring the input signal actively. If the input signal is detected, the channel will switch to the active mode. ON-time is operation mode selection dependent.

4.2 Functional Block Diagram

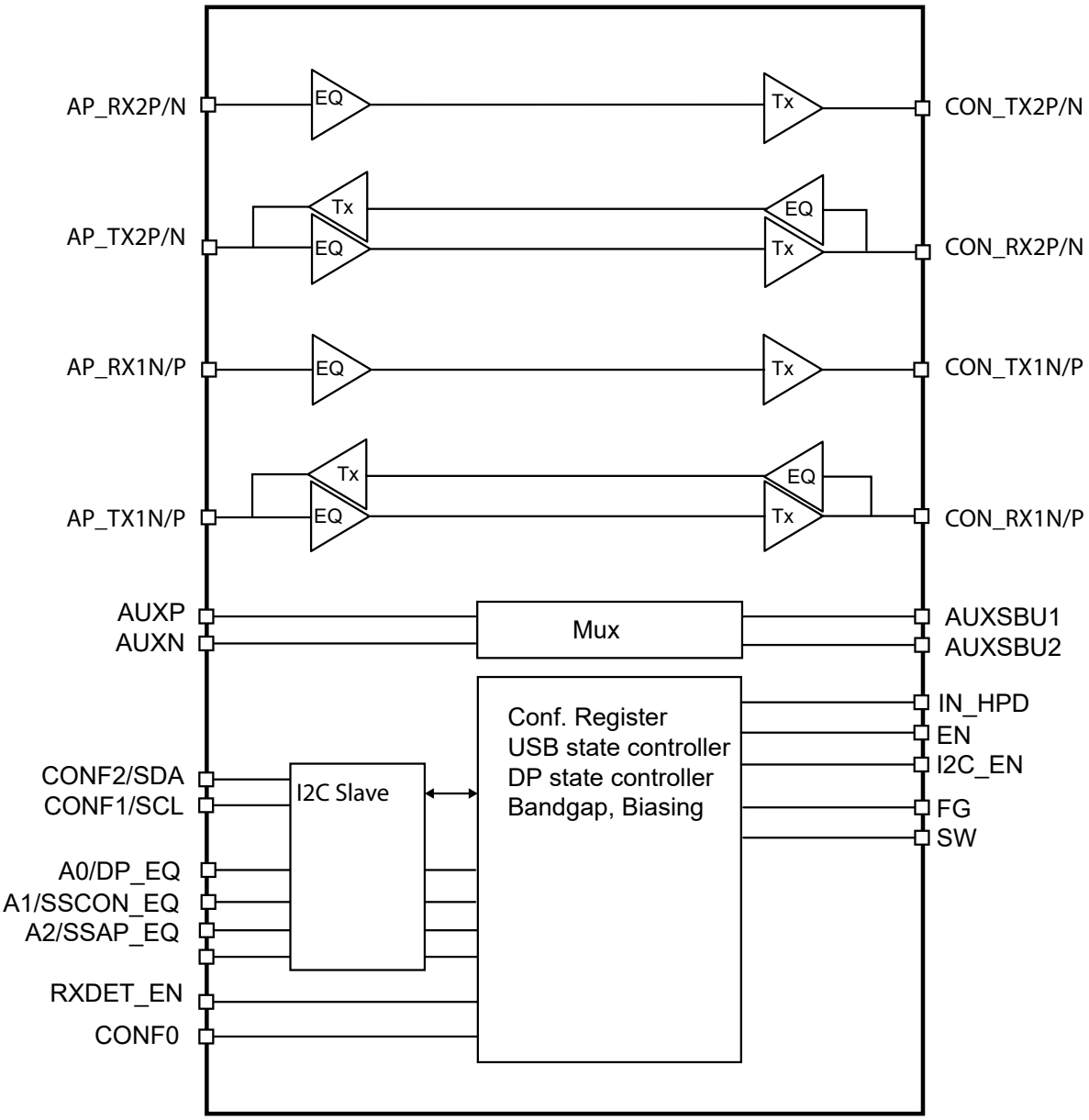


Figure 4-1 PI3DPX1207B DP-Alt ReDriver block diagram

4.3 The Operating mode control

4.3.1 Preset DP-Alt Channel mapping control

CONF	Modes	AP_RX2	AP_TX2	AP_RX1	AP_TX1	AUXP	AUXN	IN HPD/ AUX CMD
with CONF0/1/2 pins or CONF[3:0] I2C register bits control								
0000	Safe State	X	X	X	X	X	X	X
0001	Safe State	X	X	X	X	X	X	X
0010	4 lane DP1.4 + AUX	CON_ TX2 (DP1)	CON_ RX2 (DP0)	CON_ TX1 (DP2)	CON_ RX1 (DP3)	SBU1	SBU2	All CON response
0011	Flip mode: 4 lane DP1.4 + AUX	CON_ TX2 (DP2)	CON_ RX2 (DP3)	CON_ TX1 (DP1)	CON_ RX1 (DP0)	SBU2	SBU1	All CON response
0100	1 lane USB3.x (AP_CH1)	X	X	CON_ TX1	CON_ RX1	X	X	X
0101	Flip mode: 1 lane USB3.x (AP_CH2)	CON_ TX2	CON_ RX2	X	X	X	X	X
0110	USB3 (AP_CH1) + 2 lane DP1.4(AP_CH2) + AUX	CON_ TX2 (DP1)	CON_ RX2 (DP0)	CON_ TX1 (USB3)	CON_ RX1 (USB3)	SBU1	SBU2	CON2 response only
0111	Flip mode: USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) + AUX	CON_ TX2 (USB3)	CON_ RX2 (USB3)	CON_ TX1 (DP1)	CON_ RX1 (DP0)	SBU2	SBU1	CON1 response only
with CONF[3:0] i2C register bits control								
1000	USB3 (AP_CH2) + 2 lane DP1.4 (AP_CH1) + AUX	CON_TX-2(USB3)	CON_ RX-2(USB3)	CON_ TX1/DP1	CON_ RX1/ DP0	SBU1	SBU2	CON1 response only
1001	USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) +AUX (flipped)	CON_ TX2/ DP1	CON_ RX2/ DP0	CON_ TX-1(USB3)	CON_ RX-1(USB3)	SBU2	SBU1	CON2 response only
1010	4 lane TMDS mode with AUX channel for HDMI DDC	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	SBU1	SBU2	IN_HPD Only[3)]
1011	4 lane TMDS mode flipped with AUX channel for HDMI DDC	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	SBU2	SBU1	IN_HPD Only[3)]
1100	2 lane USB3.x	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	X	X	
1101	2 lane PCIe3	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	X	X	
1110	USB3 (AP_CH1) + PCIe3 (AP_CH2)	CON_TX-2(PCIe3)	CON_ RX2(P-CIe3)	CON_ TX-1(USB3)	CON_ RX-1(USB3)	X	X	X

CONF	Modes	AP_RX2	AP_TX2	AP_RX1	AP_TX1	AUXP	AUXN	IN HPD/ AUX CMD
1111	USB3 (AP_CH2) + PCIe3 (AP_CH1)	CON_ TX2(USB3)	CON_ RX2(USB3)	CON_ TX1(P-CIe3)	CON_ RX1(P-CIe3)	X	X	X

Note:
1) CONF[2:0] pins and CONF[3:0] (I2C 0x3[7:4]) with mode description. Both Pin and I2C mode can access below setting
2) The high speed channels don't do any flip action. Only the AUX channel is flipped.
3) Set the I2C reg byte12 bit2 DP_HPD_PIN_EN#=1 if the target channel is not controlled by the IN_HPD pin.

4.3.2 IN_HPD control

Table 4-1. DP_HPD_PIN_EN# register can enable the IN_HPD control

I2C Byte 0x12[2]: DP_HPD_PIN_EN#	Pin IN_HPD Status (Hot plug detection input from Sink)	DP output status
1	x	Enabled
0	0	Disabled
0	1	Enabled

4.3.3 IN_HPD assert and De-assert De-bounce timer

IN_HPD transition	De-bounce timer timeout	Notes
Assert: Low -> High	~0s	
De-assert: High -> Low	~ 325ms typ	Any Low-> High transition within timeout will reset the timer.

4.4 EQ/FG/SW controls

Table 4-2. Equalization Setting

EQ pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
L	0	0	0	0	3.2	3.8	4.9	5.7	6.1	I2C Default
	0	0	0	1	3.5	4.2	5.5	6.4	6.9	
	0	0	1	0	3.8	4.7	6.1	7.1	7.7	
	0	0	1	1	4.2	5.1	6.6	7.7	8.4	
	0	1	0	0	4.7	5.6	7.2	8.3	9	
R	0	1	0	1	5	6	7.7	8.9	9.6	
	0	1	1	0	5.4	6.4	8.2	9.4	10.1	
	0	1	1	1	5.7	6.8	8.6	9.9	10.6	
	1	0	0	0	6.2	7.3	9	10.2	11	
	1	0	0	1	6.5	7.6	9.4	10.7	11.4	
F	1	0	1	0	6.8	7.9	9.8	11.1	11.8	Pin Default
	1	0	1	1	7	8.2	10.1	11.4	12.1	
	1	1	0	0	7.4	8.5	10.4	11.7	12.4	
	1	1	0	1	7.6	8.8	10.7	12	12.7	
	1	1	1	0	7.8	9.1	11	12.3	13	
H	1	1	1	1	8.1	9.3	11.3	12.6	13.3	

4.4.1 Flat Gain Setting

Table 4-3. FG 4-level input selection pins for the DC gain

FG pin	FG[1:0]	Flat Gain Settings V/V
R (Tie Rext to GND)	00	-1.5 dB
F (Leave Open)	01	0 dB (Default)
L (Tie 0Ω to GND)	10	+1 dB
H (Tie 0Ω to VDD)	11	+2.5 dB

4.4.2 Output -1 dB Compression point output swing setting

Table 4-4. SW selection pins for the -1dB compression point output swing setting

SW pin	USB	DP
0	900mVppd	1100mVppd
1	1000mVppd	1200mVppd (Default)

4.4.3 I2C mode: 0x5[1:0] to 0x8[1:0]

CONx_SW[1:0]	Output Linear Swing Settings
00	900mVppd
01	1000mVppd
10	1100mVppd
11	1200mVppd (Default)

4.4.4 Chip Enable Setting:

Table 4-5. Channel EN enable pin

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

4.5 USB mode

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Low Power Mode and receiver detection will be active again per 6ms.

Table 4-6. The I/O termination resistance under different conditions

Symbol	Parameter	Resistance	Units
RX terminal			
Rin-pd	Input resistance at power down mode	67k to GND	Ω
Rin-U0	Input resistance at U0 condition	50 to VDD	Ω
Rin-U1	Input resistance inU1 (1)	50 to VDD	Ω
Rin-U2/U3	Input resistance in U2/U3 (1)	50 to VDD	Ω
Rin-RXDet	Input resistance in RXDET (1)	67k to VbiasRx	Ω
TX terminal			
Rout-pd	Output resistance at power down mode	HIZ	Ω
Rout-U0	Output resistance at U0 condition	50 to VbiasTx1	Ω
Rout-U1	Output resistance in U1 mode (1)	4.5k to VbiadTx1	Ω
Rout-U2/U3	Output resistance in U2/U3 mode (1)	4.5k to VbiasTx2	Ω
Rout-RXDet	Output resistance in RXDET mode (1)	4.5k to VbiasTx2	Ω

Notes: (1) The value of Rin-RxDet will be updated only after the receiver evaluation has been done. Thus, the value can be 50Ω or 67kΩ pull-low.

4.6 DisplayPort mode

By default, all channels will go to active modes if IN_HPD = 1. The ON/OFF of each DP channel is controlled by the Aux lane count.

4.6.1 DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DP TX drives doubly terminated, AC-coupled differential pairs, as shown in Figure 3-34 in a manner compliant with the Main-Link Transmitter electrical specification.

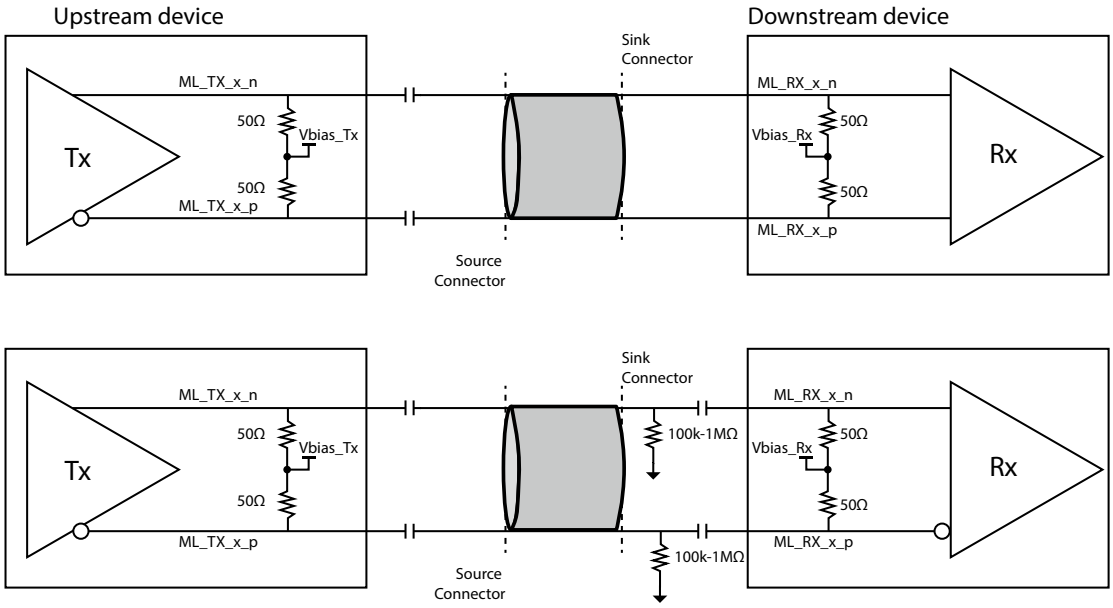


Figure 4-2 DisplayPort Main Link Connection Diagram

Table 4-7. DP Low Power Mode Description

PM_State	Mode	Description
1	Active mode	Data transfer (normal operation); The AUX monitor is actively monitoring for Link Training unless it is disabled through I2C interface. At power-up all Main Link outputs are Enabled by default. AUX Link Training is necessary to overwrite the DPCD registers to Enable/Disable Main Link outputs.
2	Standby mode	Low power consumption (I2C interface is active; AUX monitor is inactive); Main Link outputs are disabled; the Sink device has de-asserted HPD
3	Power down mode(OFF)	Lowest power consumption (EN = 0); all outputs are high-impedance; I2C interface is turned off, all inputs are ignored, I2C register is reset and AUX DPCD is reset:

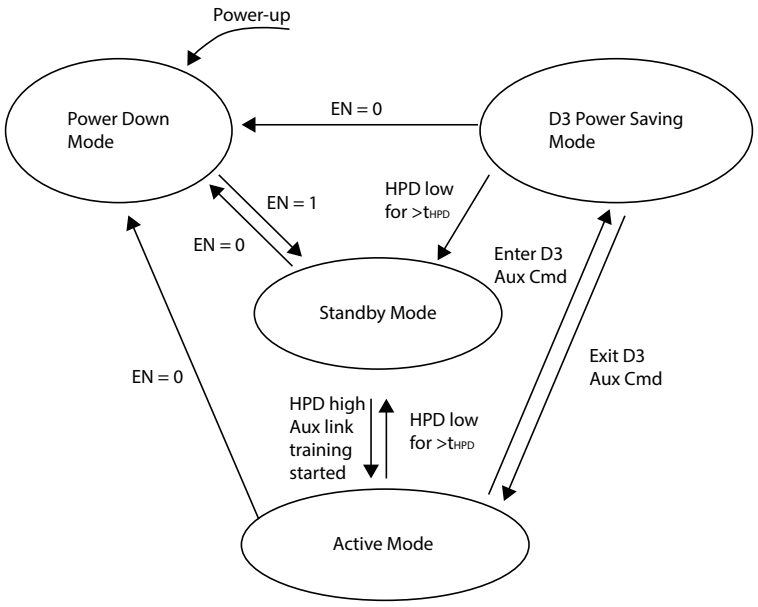


Figure 4-3 DisplayPort Operation mode

4.6.2 DisplayPort Aux Channel

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction.

The system design of a DFP_D on a USB Type-C connector connected to a UFP_D on a USB Type-C connector using a USB Type-C to USB Type-C Cable. The 2MΩ pull-down resistors on SBU1 and SBU2 are representative of the leakage of ESD and EMI/RFI components including termination to ensure no floating nodes, and are intended to show compliance with SBU Termination in USB Type-C r1.1. The plug orientation switch may be replaced by AUX polarity inversion logic in the DisplayPort transmitter or receiver, controlled by the plug orientation detection mechanism associated with the USB Type-C Receptacle. Note: The 3.3V levels in the Adaptors are derived from VCONN because not all DisplayPort UFP_D devices provide DP_PWR.

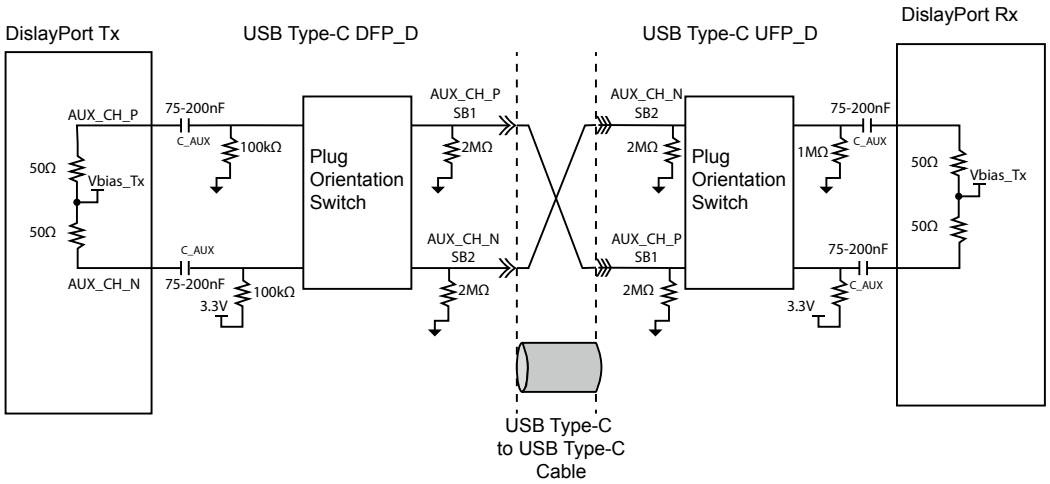


Figure 4-4 AUX Signaling Using USB Type-C to USB Type-C Cables

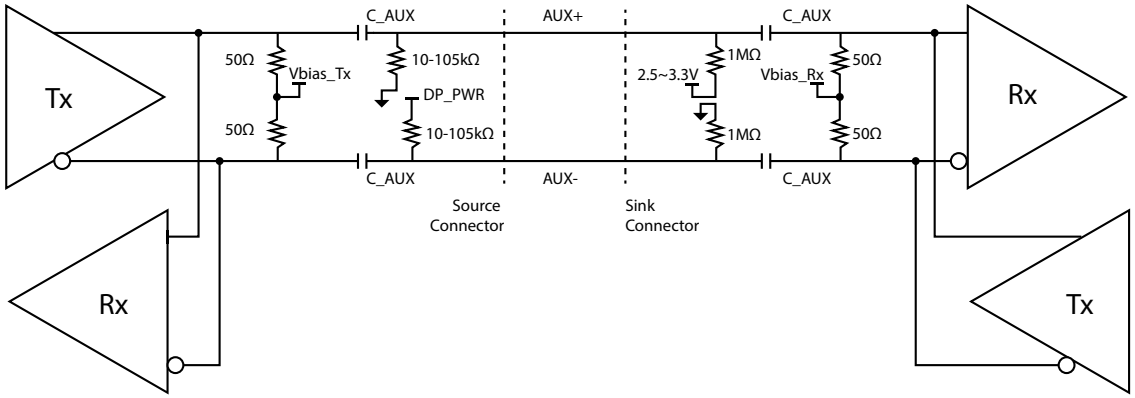


Figure 4-5 DisplayPort Aux Channel Connection

4.7 I2C Programming

4.7.1 I2C Address

Table 4-8. I2C Address bits

	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address (First byte is slave address)	1	0	1	0	A2	A1	A0	0/1 (W/R)

Note: A0, A1, A2 are pin-strapping selectable

4.7.2 I2C Feature Summary

- I2C interface operates as a slave device.
- The device supports Bulk read/write
- Support operating speed up to 1MHz
- Supported 7-bit addressing
- The data byte format is 8-bit bytes with the most significant bit (MSB) first.
- Will never hold the clock line SCL LOW to force the master into a wait state.
- No response when the data on common bus is matched to the device address.
- When I2C_EN=0, all registers become RO byte.
- If I2C master want read/write invalid register, i.e. the I2C slave just write/read from a dummy RO register with FF by default.

4.7.3 Acknowledge

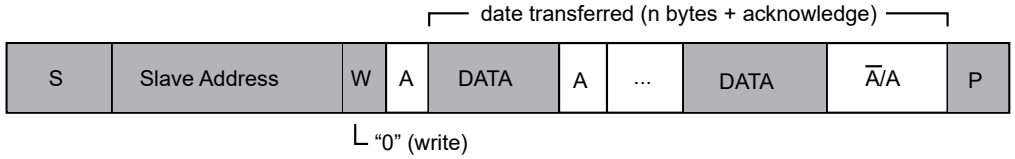
Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

4.7.4 Data Transfer

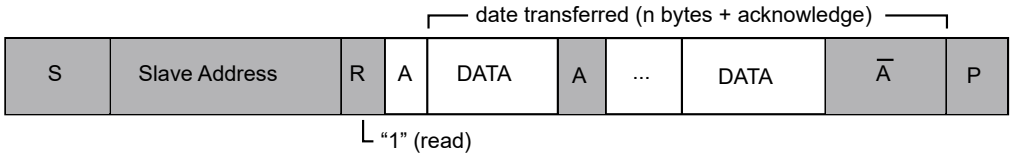
A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first. It will never hold the clock line SCL LOW to force the master into a wait state.

4.7.5 Start & Stop Condition

A HIGH to LOW transition on the SDA line, while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below



A master-transmitter addressing a slave receiver with a 7-bit address. The transfer direction is not changed



A master reads a slave immediately after the first byte.

Combined format

Figure 4-6 Block read/write protocol

4.8 Detail Programming Registers

4.8.1 Register Default Summary

Table 4-9. Programming Register Map

Byte	Read after power up	CONF[3:0]															
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h
1	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h
2	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h
3	00h	00h	10h	20h	30h	40h	50h	60h	70h	80h	90h	A0h	B0h	C0h	D0h	E0h	F0h
4	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh
5	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
6	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
7	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
8	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
9	60h	60h	62h	68h	67h	00h	0Eh	48h	27h	21h	4Eh	60h	63h	00h	00h	00h	00h
10	FCh	FCh	FCh	FCh	FCh	42h	42h	FCh	42h	42h	FCh	FEh	Feh	42h	7Fh	7Eh	42h
11	FCh	FCh	FCh	FCh	FCh	42h	42h	42h	FCh	FCh	42H	FEh	Feh	42h	7Fh	42h	7Eh
12	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h
13	00h	00h	00h	FFh	FFh	00h	00h	F0h	0Fh	0Fh	F0h	FFh	FFh	00h	00h	00h	00h
14	FFh	FFh	FFh	00h	00h	33h	CCh	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
15	C8h	C8h	C8h	C8h	C8h	C8h	C8h	59h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h
16	DCh	DCh	DCh	5Ch	5Ch	D3h	D3h	DCh	56h	56h	59h	5Ch	5Ch	D3h	D3h	D3h	D3h
17	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h
18	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h
19 ~30	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
31	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h

4.8.2 BYTE 0 (Revision and Vendor ID Register)

Bit	Type	Power up condition	Control affected	Comment
7	RO	0	Revision ID	Rev# = 0000
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0	Vendor ID	Pericom
2	RO	0		
1	RO	1		
0	RO	1		

4.8.3 BYTE 1 (Device Type/Device ID register)

Bit	Type	Power up condition	Control affected	Comment
7	RO	0	Device Type	Device Type Active Mux = 0001
6	RO	0		
5	RO	0		
4	RO	1		
3	RO	0	Device ID	Device ID PI3DPX1207 = 0001
2	RO	0		
1	RO	0		
0	RO	1		

4.8.4 BYTE 2 (Byte count register)

Bit	Type	Power up condition	Control affected	Comment
7	RO	0	Register Byte count	I2C byte count = 32 bytes
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		

4.8.5 BYTE 3 (Mode control)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, This byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	0	0	CONF<3>	Channel Preset assignment for the Preset Application Mode,
6	R/W	Latch	0	CONF<2>	
5	R/W	Latch	0	CONF<1>	
4	R/W	Latch	0	CONF<0>	
3	R/W	0	0	Reserved	
2	R/W	Latch	0	PIN_RXDET_EN# Inverted version of Pin9 RXDET_EN	Far end Receiver termination detection Enable (Active Low) 0 - Detection is enabled. 1 - Detection is disabled.
1:0	R/W	0	0		Reserved

4.8.6 BYTE 4 (Override the power down control)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EN pin	0	PD_CON_RX1	CONx power down override 0 – Normal operation 1 – Force the CONx to power down state
6	R/W	Latch EN pin	0	PD_CON_TX1	
5	R/W	Latch EN pin	0	PD_CON_TX2	
4	R/W	Latch EN pin	0	PD_CON_RX2	
3	R/W	1	1	Reserved	
2	R/W	1	1	Reserved	
1	R/W	0	0	IN_HPD_ActiveHigh_EN#	0 - IN_HPD Active High 1 - IN_HPD Active Low
0	R/W	1	1	Reserved	

4.8.7 BYTE 5 (Equalization, Flat gain and -1dB linear Swing setting of CON_RX2)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_RX2_EQ<3>	CON_RX2 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_RX2_EQ<2>	
5	R/W	Latch EQ	0	CON_RX2_EQ<1>	
4	R/W	Latch EQ	0	CON_RX2_EQ<0>	
3	R/W	Latch_FG	0	CON_RX2_FG<1>	
2	R/W	Latch_FG	1	CON_RX2_FG<0>	
1	R/W	Latch_SW	1	CON_RX2_SW<1>	
0	R/W	Latch_SW	1	CON_RX2_SW<0>	

4.8.8 BYTE 6 (Equalization, Flat gain and -1dB linear Swing setting of CON_TX2)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_TX2_EQ<3>	CON_TX2 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_TX2_EQ<2>	
5	R/W	Latch EQ	0	CON_TX2_EQ<1>	
4	R/W	Latch EQ	0	CON_TX2_EQ<0>	
3	R/W	Latch_FG	0	CON_TX2_FG<1>	
2	R/W	Latch_FG	1	CON_TX2_FG<0>	
1	R/W	Latch_SW	1	CON_TX2_SW<1>	
0	R/W	Latch_SW	1	CON_TX2_SW<0>	

4.8.9 BYTE 7 (Equalization, Flat gain and -1dB linear Swing setting of CON_TX1)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_TX1_EQ<3>	CON_TX1 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_TX1_EQ<2>	
5	R/W	Latch EQ	0	CON_TX1_EQ<1>	
4	R/W	Latch EQ	0	CON_TX1_EQ<0>	
3	R/W	Latch_FG	0	CON_TX1_FG<1>	
2	R/W	Latch_FG	1	CON_TX1_FG<0>	
1	R/W	Latch_SW	1	CON_TX1_SW<1>	
0	R/W	Latch_SW	1	CON_TX1_SW<0>	

4.8.10 BYTE 8 (Equalization, Flat gain and -1dB linear Swing setting of CON_RX1)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_RX1_EQ<3>	CON_RX1 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_RX1_EQ<2>	
5	R/W	Latch EQ	0	CON_RX1_EQ<1>	
4	R/W	Latch EQ	0	CON_RX1_EQ<0>	
3	R/W	Latch_FG	0	CON_RX1_FG<1>	
2	R/W	Latch_FG	1	CON_RX1_FG<0>	
1	R/W	Latch_SW	1	CON_RX1_SW<1>	
0	R/W	Latch_SW	1	CON_RX1_SW<0>	

4.8.11 BYTE 9 (RESERVED)

4.8.12 BYTE 10 (Feature control of the CON_RX2 and CON_TX2)

- CON2 represents CON_RX2 and CON_TX2

Bit	Type	Power up condition	Control affected	Comment
7	R/W	1	CON2 Feature 0	
6	R/W	1	CON2 Feature 1	
5	R/W	1	CON2 Feature 2	
4	R/W	1	CON2 Feature 3	
3	R/W	1	CON2 Feature 4	
2	R/W	1	CON2 Feature 5	
1	R/W	0	CON2 Feature 6	
0	R/W	0	CON2 Feature 7	