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PERICOM®

# PI3HDMI341ART

## 3:1 Active HDMI 1.3 Compatible Switch with Optimized Equalization for Enhanced Signal Integrity

### Features

- Supply voltage, $V_{CC}$ = 3.3V ±5%
- Each Port is compatible w/ DVI, HDMI 1.1, HDMI 1.2 or HDMI 1.3 signals
- Supports both AC-coupled and DC-coupled inputs
- Support for 8-bit, 10-bit, and 12-bit deep color per channel
- High Performance, up to 2.5 Gbps per channel
- Switching support for 3 side band signals (SCL, SDA and HPD)
- 5V Tolerance on all side band signals
- SCL, SDA, and HPD pins are the only pins that can support HOT INSERTION
- Integrated 50-ohm (±10%) termination resistors at each high speed signal input
- Configurable output swing control (500mV, 750mV, 1000mV)
- Configurable Pre-Emphasis levels (0dB, 1.5dB, 3.5dB, & 6.0dB)
- Configurable De-Emphasis (0dB, -3.5dB, -6.0dB, -9.5dB)
- Optimized Equalization
  Single default setting will support all cable lengths
- ESD protection = 8kV (typical) on high-speed data channels only
- Propagation delay ≤ 2ns
- High Impedance Outputs when disabled
- Packaging (Pb-free & Green): 80-contact LQFP (FF80)

### Description

Pericom Semiconductor's PI3HDMI341ART 3:1 active switch circuit is targeted for high-resolution video networks that are based on DVI/HDMI standards and TMDS signal processing. The PI3HDMI341ART is an active 3 TMDS to 1 TMDS receiver switch with Hi-Z outputs. The device receives differential signals from selected video components and drives the video display unit. It provides three controllable output swings that can be controlled through a single bit. The allowable output swings are 500mV, 750mV and 1000mV. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times which are reduced during transmission across long distances.

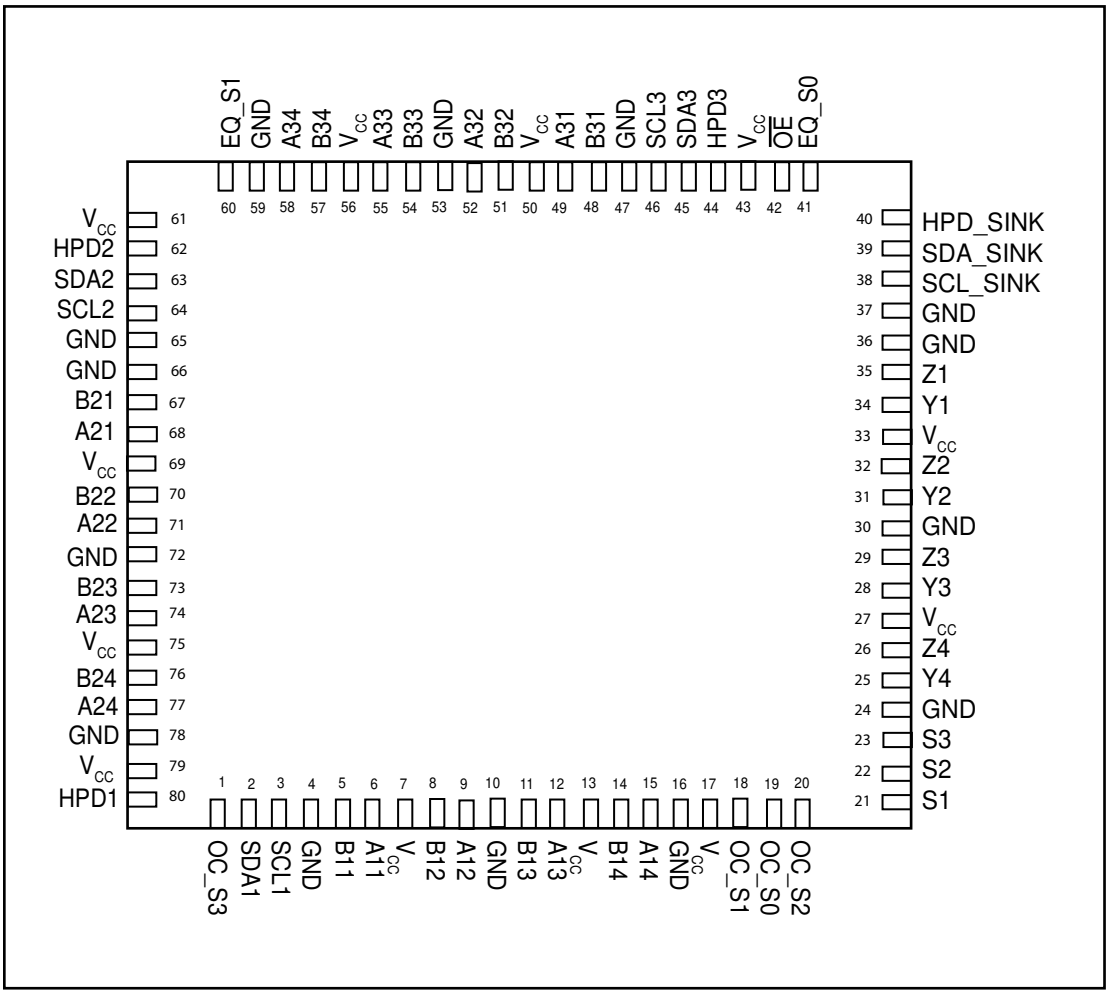
Each complete HDMI/DVI channel also has slower speed, side band signals, that are required to be switched. Pericom's solution provides a complete solution by integrating the side band switch together with the high speed switch in a single solution. Using Equalization at the input of each of the high speed channels, Pericom can successfully eliminate deterministic jitter caused by long cables from the source to the sink. The elimination of the deterministic jitter allows the user to use much longer cables (up to 25 meters).

The maximum DVI/HDMI Bandwidth of 2.5 Gbps provides 12-bit deep color support, which is offered by HDMI revision 1.3. Due to its active uni-directional feature, this switch is designed for usage only for the video receiver's side. For consumer video networks, the device sits at the receiver's side to switch between multiple video components, such as PC, DVD, STB, D-VHS, etc. The PI3HDMI341ART is the industry's first active DVI/HDMI switch compatible with HDMI 1.1, 1.2, and 1.3 which ensures transmitting high-bandwidth video streams from video components to the display unit. The PI3HDMI341ART also provides enhanced robust ESD/EOS protection of 8kV, which is required by many consumer video networks today.

The Optimized Equalization provides the user a single optimal setting that can provide HDMI compliance for all cable lengths: 1meter to 20meters and color depths of 8bit/ch, or 12bit/ch.

Pericom also offers the abiility to fine tune the equalization settings in situations where cable length is known. For example, if 25meter cable length is required, Pericom's solution can be adjusted to 16dB EQ to accept 25metere cable length.

## Pin Configuration

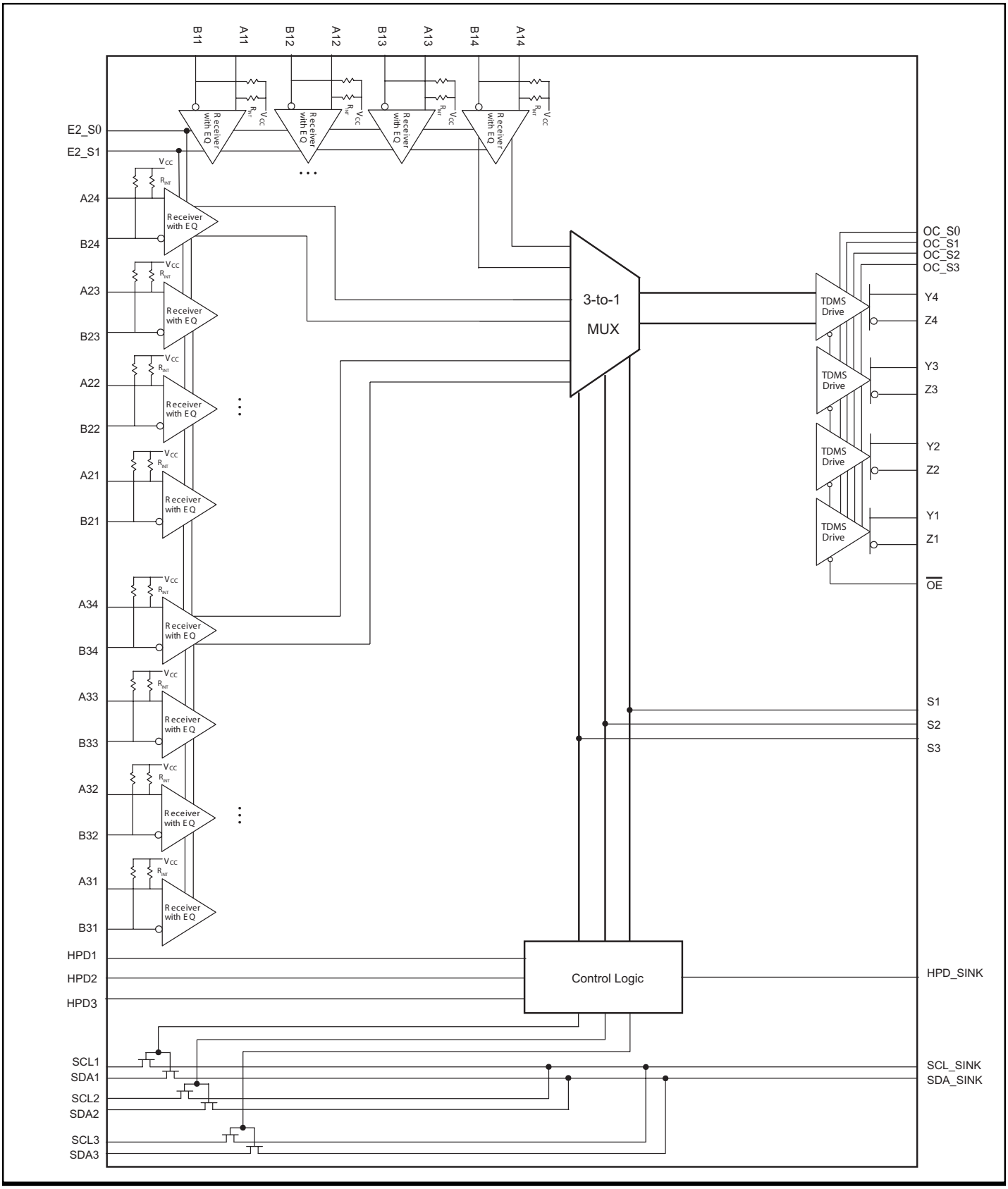


## Pin Description

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 6,9,12,15 | A11, A12, A13, A14 | I | Port 1 TMDS Positive inputs |
| 68, 71, 74, 77 | A21, A22, A23, A24 | I | Port 2 TMDS Positive inputs |
| 49, 52, 55, 58 | A31, A32, A33, A34 | I | Port 3 TMDS Positive inputs |
| 5, 8, 11, 14 | B11, B12, B13, B14 | I | Port 1 TMDS Negative inputs |
| 67, 70, 73, 76 | B21, B22, B23, B24 | I | Port 2 TMDS Negative inputs |
| 48, 51, 54, 57 | B31, B32, B33, B34 | I | Port 3 TMDS Negative inputs |
| 4, 10, 16 24, 30, 36, 37, 47, 53, 59, 65, 66, 72, 78 | GND | | Ground |
| 80 | HPD1 | O | Port 1 HPD output |
| 62 | HPD2 | O | Port 2 HPD output |
| 44 | HPD3 | O | Port 3 HPD output |
| 40 | HPD_Sink | I | Sink side hot plug detector input. High: 5-V power signal asserted from source to sink and EDID is ready.<br>Low: No 5-V power signal asserted from source to sink, or EDID is not ready. |
| 42 | $\overline{OE}$ | I | Output Enable, Active LOW |
| 3 | SCL1 | I/O | Port 1 DDC Clock |
| 64 | SCL2 | I/O | Port 2 DDC Clock |
| 46 | SCL3 | I/O | Port 3 DDC Clock |
| 38 | SCL_Sink | I/O | Sink Side DDC Data |
| 2 | SDA1 | I/O | Port 1 DDC Data |
| 63 | SDA2 | I/O | Port 2 DDC Data |
| 45 | SDA3 | I/O | Port 3 DDC Data |
| 39 | SDA_Sink | I/O | Sink Side DDC Data |
| 21,22,23 | S1, S2, S3 | I | Source Input Selector |
| 7, 13, 17 27, 33, 43, 50, 56 61, 69, 75, 79 | $V_{CC}$ | | 3.3V Power Supply |
| 34, 31, 28, 25 | Y1, Y2, Y3, Y4 | O | TMDS positive outputs |
| 35, 32, 29, 26 | Z1, Z2, Z3, Z4 | O | TMDS negative outputs |
| 41, 60 | EQ_S0, EQ_S1 | I | Equalizer controls(1) |
| 19, 18, 20, 1 | OC_S0, OC_S1, OC_S2, OC_S3 | I | Output buffer controls<br>Note: OC_S3 has an internal pull-up resistor. OC_S2 has an internal pull-down resistor. |

Note:
1. EQ_S0 has an internal pull-down and EQ_S1 has an internal pull-up

## Switch Block Diagram



## Truth Table

| Control Pins | | | I/O Selected | | Hot Plug Detect Status | | |
|---|---|---|---|---|---|---|---|
| S1 | S2 | S3 | Y/Z | SCL_Sink<br>SDA_Sink | HPD1 | HPD2 | HPD3 |
| H | x | x | A1/B1 | SCL1<br>SDA1 | HPD_Sink | L | L |
| L | H | x | A2/B2 | SCL2<br>SDA2 | L | HPD_Sink | L |
| L | L | H | A3/B3 | SCL3<br>SDA3 | L | L | HPD_Sink |
| L | L | L | None (Hi-Z) | None (Hi-Z) | L | L | L |

## OC Setting Value Logic Table

| Input Control Pins | | | | Setting Value | | |
|---|---|---|---|---|---|---|
| OC_S3 | OC_S2 | OC_S1 | OC_S0 | $V_{swing}$ (mV) | $V_{os}$ (V) | Pre-emphasis/De-emphasis (dB) |
| 0 | 0 | 0 | 0 | 500 | 3.06 | none |
| 0 | 0 | 0 | 1 | 750 | 2.95 | none |
| 0 | 0 | 1 | 0 | 1000 | 2.84 | none |
| 0 | 0 | 1 | 1 | 500 | 3.02 | none |
| 0 | 1 | 0 | 0 | 500 | 3.06 | 0 |
| 0 | 1 | 0 | 1 | 500 | 3.05 | 1.5 |
| 0 | 1 | 1 | 0 | 500 | 2.97 | 3.5 |
| 0 | 1 | 1 | 1 | 500 | 2.9 | 6 |
| 1 | 0 | 0 | 0 | 500 | 3.08 | 0 |
| 1 | 0 | 0 | 1 | 340 | 3.08 | -3.5 |
| 1 | 0 | 1 | 0 | 270 | 3.08 | -6 |
| 1 | 0 | 1 | 1 | 160 | 3.08 | -9.5 |
| 1 | 1 | 0 | 0 | 1000 | 2.85 | 0 |
| 1 | 1 | 0 | 1 | 830 | 2.85 | -3.5 |
| 1 | 1 | 1 | 0 | 500 | 2.85 | -6 |
| 1 | 1 | 1 | 1 | 330 | 2.85 | -9.5 |

## EQ Setting Value Logic Table

| EQ_S1 | EQ_S0 | Setting Value |
|---|---|---|
| 0 | 0 | 3dB on all high speed inputs |
| 0 | 1 | 8dB on all high speed inputs |
| 1 | 0 | Optimized Equalization enabled on all high speed inputs (default value if both EQ_S0 and EQ_S1 are left floating) |
| 1 | 1 | 16dB on all high speed inputs |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential..... –0.5V to +4.0V
DC Input Voltage ..... –0.5V to $V_{CC}$
DC Output Current..... 120mA
Power Dissipation ..... 1.0W

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |
| **TMDS Differential Pins (A/B)** | | | | | |
| $V_{ID}$ | Receiver peak-to-peak differential input voltage | 150 | | 1560 | mVp-p |
| $V_{IC}$ | Input common mode voltage | 2 | | $V_{CC}$ + 0.01 | V |
| $V_{CC}$ | TMDS output termination voltage | 3.135 | 3.3 | 3.465 | V |
| $R_T$ | Termination resistance | 45 | 50 | 55 | ohm |
| | Signaling rate | 0 | | 2.5 | Gbps |
| **Control Pins (OC_Sx, EQ_Sx, S, $\overline{OE}$)** | | | | | |
| $V_{IH}$ | LVTTL High-level input voltage | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | LVTTL Low-level input voltage | GND | | 0.8 | |
| **DDC Pins (SCL, SCL_SINK, SDA, SDA_SINK)** | | | | | |
| $V_{I(DDC)}$ | Input voltage | GND | | 5.5 | V |
| **Status Pins (HPD_SINK)** | | | | | |
| $V_{IH}$ | LVTTL High-level input voltage | 2 | | 5.3 | V |
| $V_{IL}$ | LVTTL Low-level input voltage | GND | | 0.8 | |

## TMDS Compliance Test Results

| Item | HDMI 1.3 Spec | Pericom Product Spec |
|---|---|---|
| **Operating Conditions** | | |
| Termination Supply Voltage, $V_{CC}$ | 3.3V ≤ 5% | 3.30 ± 5% |
| Terminal Resistance | 50-ohm ± 10% | 45 to 55-ohm |
| **Source DC Characteristics at TP1** | | |
| Single-ended high level output voltage, VH | $V_{CC}$ ± 10mV | $V_{CC}$ ±10mV |
| Single-ended low level output voltage, VL | ( $V_{CC}$ - 600mV) ≤ VL ≤ ( $V_{CC}$- 400mV) | ( $V_{CC}$ - 600mV) ≤ VL ≤ ( $V_{CC}$ - 400mV) |
| Single-ended output swing voltage, Vswing | 400mV ≤ Vswing ≤ 600mV | 400mV ≤ Vswing ≤ 600mV |
| Single-ended standby (off) output voltage, Voff | $V_{CC}$ ± 10mV | $V_{CC}$ ± 10mV |
| **Transmitter AC Characteristics at TP1** | | |
| Risetime/Falltime (20%-80%) | 75ps ≤ Risetime/Falltime ≤ 0.4 Tbit<br>(75ps ≤ tr/tf ≤ 242ps) @ 1.65 Gbps | 240ps |
| Intra-Pair Skew at Transmitter Connector, max | 0.15 Tbit<br>(90.9ps @ 1.65 Gbps) | 60ps max |
| Inter-Pair Skew at Transmitter Connector, max | 0.2 Tpixel<br>(1.2ns @ 1.65 Gbps) | 100ps max |
| Clock Jitter, max | 0.25 Tbit<br>(151.5ps @ 1.65 Gbps) | 82ps max |
| **Sink Operating DC Characteristics at TP2** | | |
| Input Differential Voltage Level, Vdiff | 150 ≤ Vdiff ≤ 1200mV | 150mV ≤ $V_{DIFF}$ ≤ 1200mV |
| Input Common Mode Voltage Level, $V_{ICM}$ | ( $V_{CC}$ - 300mV) ≤ Vicm ≤ ( $V_{CC}$- 37.5mV)<br>Or<br>$V_{CC}$ ±10% | ( $V_{CC}$ - 300mV) ≤ Vicm ≤ ( $V_{CC}$- 37.5mV)<br>Or<br>$V_{CC}$ ±10% |
| **Sink DC Characteristics When Source Disabled or Disconnected at TP2** | | |
| Differential Voltage Level | $V_{CC}$ ± 10mV | $V_{CC}$ ±10mV |

**Electrical Characteristics** (over recommended operating conditions unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ.(1) | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current | $V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 0.4V, $R_T$ = 50-ohm, $V_{CC}$ = 3.3V Am/Bm = 1.65 Gbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 165 MHz clock | | 190 | 230 | mA |
| $P_D$ | Power Dissipation | | | 394 | 657 | mW |
| **TMDS Differential Pins (A/B; Y/Z)** | | | | | | |
| $V_{OH}$ | Single-ended high-level output voltage | $V_{CC}$ = 3.3V, $R_T$ = 50-ohm Pre-emphasis/De-emphasis = 0dB | $V_{CC}$- 10 | | $V_{CC}$ + 10 | mV |
| $V_{OL}$ | Single-ended low-level output voltage | | $V_{CC}$ - 600 | | $V_{CC}$ - 400 | |
| $V_{swing}$ | Single-ended output swing voltage | | 400 | | 600 | |
| $V_{OD(O)}$ | Overshoot of output differential voltage | | | 6% | 15% | 2x $V_{swing}$ |
| $V_{OD(U)}$ | Undershoot of output differential voltage | | | 12% | 25% | |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | | | 0.5 | 5 | mV |
| $\|I_{(OS)}\|$ | Short circuit output current | | | | 12 | mA |
| $V_{ODE(SS)}$ | Steady state output differential voltage | OC_S0 = $V_{CC}$, Am/Bm = 250 Mbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 25 MHz clock | 560 | | 840 | mVp-p |
| $V_{ODE(PP)}$ | Peak-to-peak output differential voltage | | 800 | | 1200 | |
| $V_{I(open)}$ | Single-ended input voltage under high impedance input or open input | $I_I$ = 10µA | $V_{CC}$ - 10 | | $V_{CC}$ + 10 | mV |
| $R_{INT}$ | Input termination resistance | $V_{IN}$ = 2.9V | 45 | 50 | 55 | ohm |
| **DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)** | | | | | | |
| $\|I_{lkg}\|$ | Input leakage current | $V_I$ = 0.1$V_{CC}$ to 0.9$V_{CC}$ to isolated DDC ports | | 0.1 | 2 | µA |
| $C_{IO}$ | Input/output capacitance | $V_I$ = 0V | | 7.5 | | pF |
| $R_{ON}$ | Switch resistance | $I_O$ = 3mA, $V_O$ = 0.4V | | 25 | 50 | ohm |
| $V_{PASS}$ | Switch output voltage | $V_I$ = 3.3V, $I_I$ = 100µA | 1.5(2) | 2.0 | 2.5(3) | V |
| **Status Pins (HPD)** | | | | | | |
| $V_{OH(TTL)}$ | TTL High-level output voltage | $I_{OH}$ = -8mA | 2.4 | | | V |
| $V_{OL(TTL)}$ | TTL Low-level output voltage | $I_{OH}$ = 8mA | | | 0.4 | V |

**(Table Continued)**

## Electrical Characteristics (Continued)

| Symbol | Parameter | Test Conditions | Min. | Typ.(1) | Max. | Units |
|---|---|---|---|---|---|---|
| **Control Pins (OC_Sx, EQ_Sx, S, $\overline{OE}$)** | | | | | | |
| $\|I_{IH}\|$ | High-level digital input current | $V_{IH}$= 2.0V or $V_{CC}$ | | 0.1 | 2 | µA |
| $\|I_{IL}\|$ | Low-level digital input current | $V_{IL}$ = GND or 0.8V | | 0.1 | 2 | |
| **Status Pins (HPD_SINK)** | | | | | | |
| $\|I_{IH}\|$ | High-level digital input current | $V_{IH}$ = 5.3V | | 23 | 100 | µA |
| | | $V_{IH}$ = 2.0V or $V_{CC}$ | | 0.1 | 2 | |
| $\|I_{IL}\|$ | Low-level digital input current | $V_{IL}$ = GND or 0.8V | | 0.1 | 2 | |

**Notes:**

1. All typical values are at 25°C and with a 3.3V supply.
2. The value is tested in full temperature range at 3.0V.
3. The value is tested in full temperature range at 3.6V.

**Switching Characteristics** (over recommended operating conditions unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ.(1) | Max. | Units |
|---|---|---|---|---|---|---|
| **TMDS Differential Pins (Y/Z)** | | | | | | |
| tpd | Propagation delay | $V_{CC}$ = 3.3V, $R_T$ = 50-ohm, pre-emphasis/de-emphasis = 0dB | | 2000 | | ps |
| $t_r$ | Differential output signal rise time (20% - 80%) | | 75 | | 240 | |
| $t_f$ | Differential output signal fall time (20% - 80%) | | 75 | | 240 | |
| $t_{sk(p)}$ | Pulse skew | | | 7 | 50 | |
| $t_{sk(D)}$ | Intra-pair differential skew | | | 23 | 50 | |
| $t_{sk(o)}$ | Inter-pair differential skew(2) | | | | 100 | |
| $t_{jit(pp)}$ | Peak-to-peak output jitter from Y/Z(1) residual jitter | pre-emphasis/de-emphasis = 0dB, Am/Bm = 1.65 Gbps HDMI data pattern, m = 2 ,3, 4 A1/B1 = 165 MHz clock | | 15 | 30 | |
| $t_{jit(pp)}$ | Peak-to-peak output jitter from Y/Z(2:4) residual jitter | | | 18 | 50 | |
| $t_{DE}$ | De-emphasis duration | de-emphasis = -3.5dB, Am/Bm = 250 Mbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 25 MHz clock | | 240 | | |
| $t_{SX}$ | Select to switch output | | | 6 | 10 | ns |
| $t_{en}$ | Enable time | | | 6 | 10 | |
| $t_{dis}$ | Disable time | | | 6 | 10 | |
| **DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)** | | | | | | |
| $t_{pd(DDC)}$ | Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAn | $C_L$ = 10pF | | 0.4 | 2.5 | ns |
| **Control and Status Pins (OC_SX, EQ_SX, S, HPD_SINK, HPD)** | | | | | | |
| $t_{pd(HPD)}$ | Propagation delay (from HPD_SINK to the active port of HPD) | $C_L$ = 10pF | | 2 | 6.0 | ns |
| $t_{sx(HPD)}$ | Switch time (from port select to the latest valid status of HPD) | | | 3 | 6.5 | |

**Notes:**

1. All typical values are at 25°C and with a 3.3V supply.
2. $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.

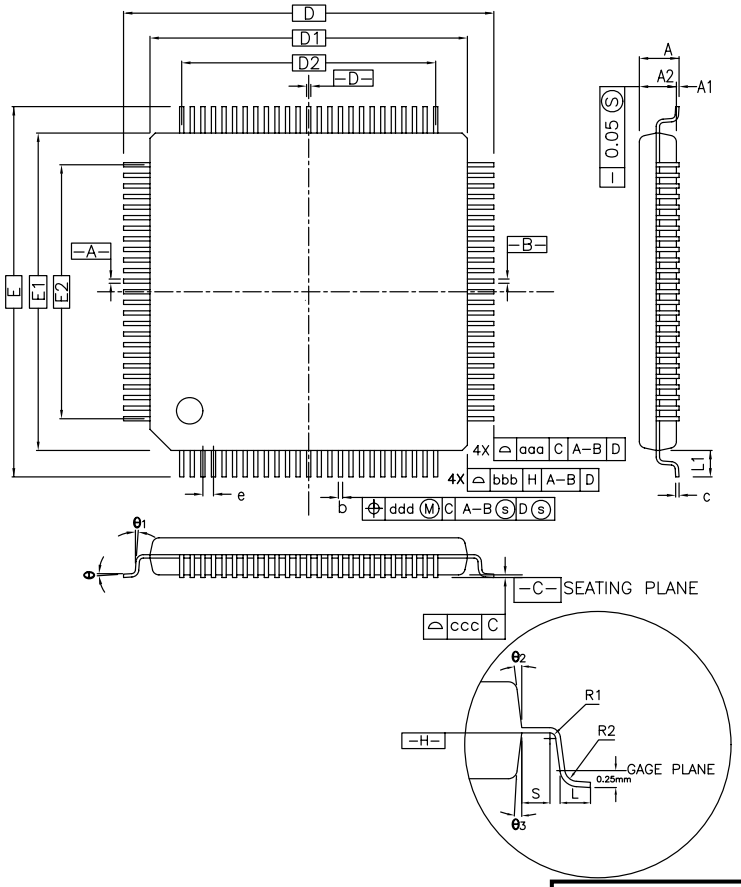
## Application Information

***Supply Voltage***

All $V_{CC}$ pins are recommended to have a 0.01uF capacitor tied from $V_{CC}$ to GND to filter supply noise

***TMDS inputs***

Standard TMDS terminations have already been integrated into Pericom's PI3HDMI341ART device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.




| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 14.00 BSC. | | | 0.551 BSC. | | |
| D1 | 12.00 BSC. | | | 0.472 BSC. | | |
| E | 14.00 BSC. | | | 0.551 BSC. | | |
| E1 | 12.00 BSC. | | | 0.472 BSC. | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 9.50 | | | 0.374 | | |
| E2 | 9.50 | | | 0.374 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

**Notes:**
1) All dimensions are in millimeters, angles in degrees
2) Ref JEDEC: MS-026/BDD
3) Package outline exclusive of mold flash and metal burr

PERICOM Semiconductor Corporation

**DATE: 07/27/06**

**DESCRIPTION: 80-pin, Low Profile Quad Flat Package (LQFP)**

**PACKAGE CODE: FF80**

**DOCUMENT CONTROL #: PD-2064** **REVISION: -**

## Ordering Information

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI3HDMI341ARTFFE | FF | 80-pin, Pb-free & Green LQFP |

**Notes:**

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel