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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Dual Mode DisplayPort™ to DVI/HDMI™ Electrical bridge (Level Shifter)

## Features

- Converts low-swing AC coupled differential input to HDMI™ rev 1.3 compliant open-drain current steering Rx terminated differential output
- HDMI Level shifting operation up to 2.5Gbps per lane (250MHz pixel clock)
- Integrated 50-ohm termination resistors for AC-coupled differential inputs.
- Provide Output Squelch function to turn off TMDS common mode output buffer when TMDS clock is not present
- Enable/Disable feature to turn off TMDS outputs to enter low-power state.
- Output slew rate control on TMDS outputs to minimize EMI
- Integrated Active / Passive DDC level shifters (3.3V source to 5V sink)
- Transparent operation: no re-timing or configuration required
- Level shifter for HPD signal from HDMI/DVI connector
- Integrated pull-down on HPD_SINK input guarantees "input low" when no display is plugged in
- 3.3V Power supply required
- TMDS output enable control
- ESD protection on all I/O pins
  - 4kV HBM
  - ±8kV contact ESD protection on the following pins
    - → OUT_Dx±
    - → SDA_SINK, SCL_SINK
    - → HPD_SINK
- Packaging (Pb-free & Green available):
  - 48 TQFN, 7mm × 7mm (ZBE)

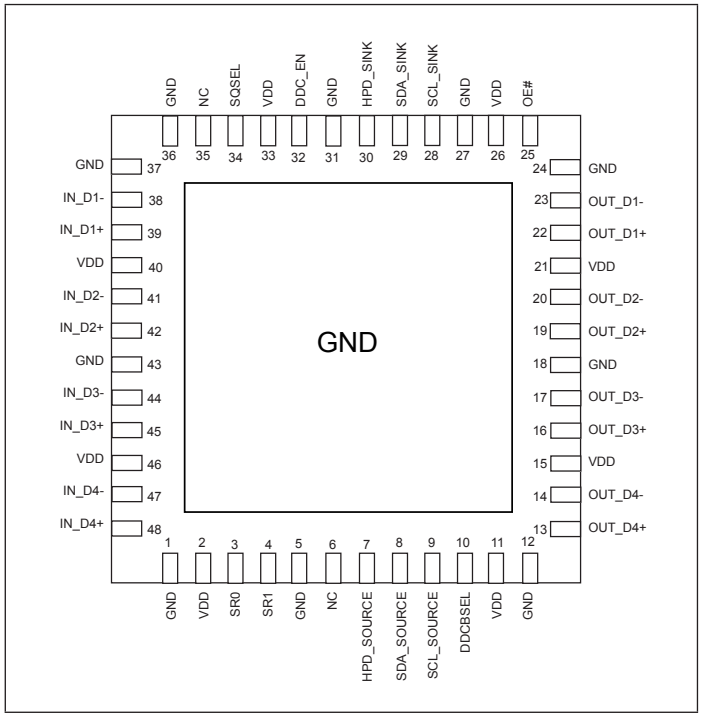
## Description

Pericom Semiconductor's PI3VDP411LSA provides the ability to use a Dual-mode DisplayPort™ transmitter in HDMI™ mode. This flexibility provides the user a choice of how to connect to their favorite display. All signal paths accept AC coupled video signals. The PI3VDP411LSA converts this AC coupled signal into an HDMI rev 1.3 compliant signal with proper signal swing. This conversion is automatic and transparent to the user.

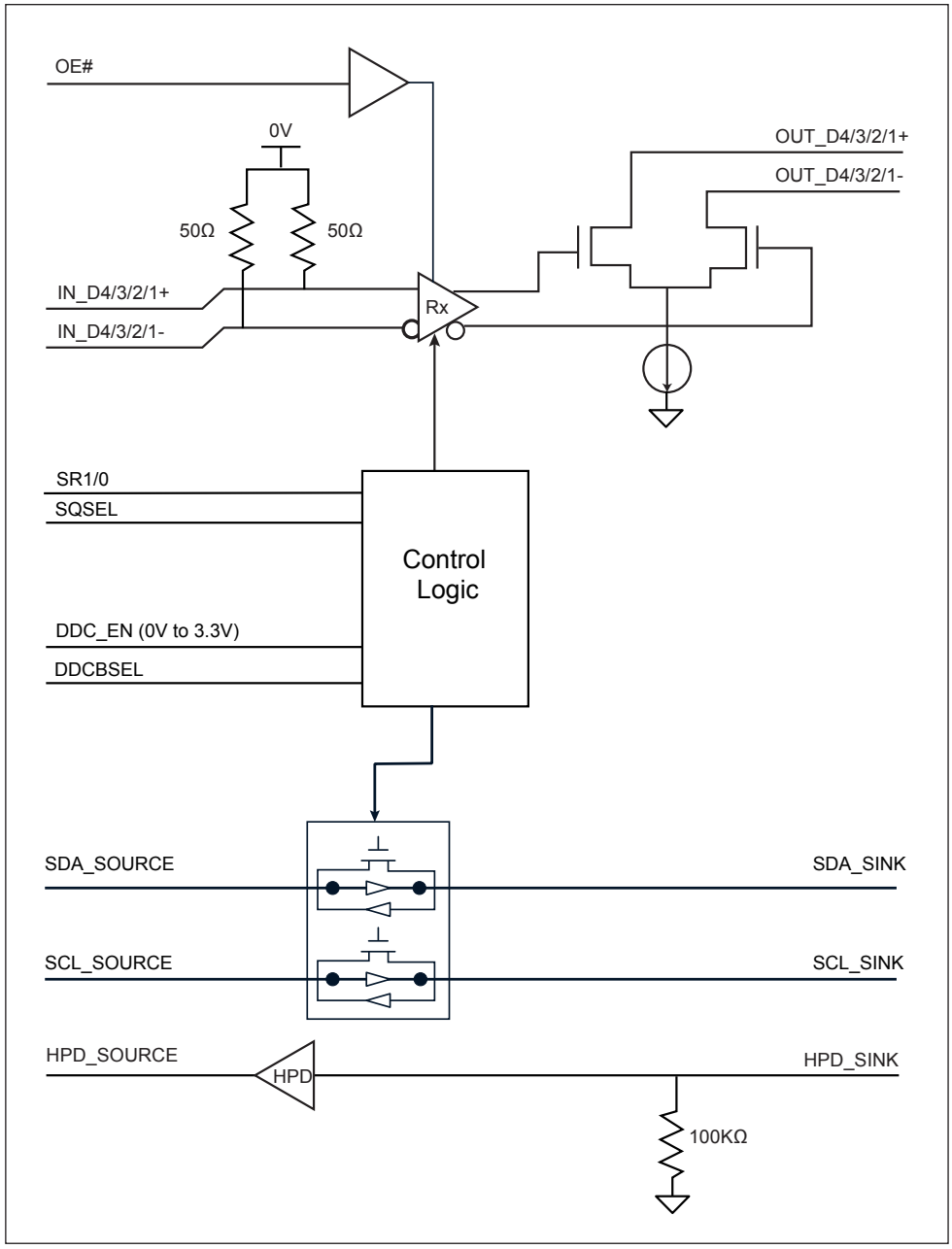
Output squelch function is provided for each channel. When output channel is enable (OE#=0) and operating, that TMDS pixel clock input signal determines whether the output is enabled. When no TMDS pixel clock is present, TMDS output channel will be disabled.

The PI3VDP411LSA supports up to 2.5Gbps, which provides 12-bits of color depth per channel, as indicated in HDMI rev 1.3.

## Pin Configuration (48-Pin TQFN)



## Block Diagram



## Pin Description

<table>
<tr><th>Pin</th><th>Name</th><th>I/O Type</th><th>Descriptions</th></tr>
<tr><td>1, 5, 12, 18, 24, 27, 31, 36, 37, 43</td><td>GND</td><td>POWER</td><td>GROUND</td></tr>
<tr><td>2, 11, 15, 21, 26, 33, 40, 46</td><td>$V_{DD}$</td><td>POWER</td><td>POWER, 3.3V ±10%</td></tr>
<tr><td>3, 4</td><td>SR0, SR1</td><td>I</td><td>Slew Rate Control. Acceptable connections to SRx pin are: resistor to 3.3V or short to GND. (internal 200KΩ pull-LOW)</td></tr>
<tr><td>6, 35</td><td>NC</td><td>O</td><td>No Connect</td></tr>
<tr><td>7</td><td>HPD_SOURCE</td><td>O</td><td>HPD_SOURCE: 0V to 3.3V (nominal) output signal. HPD_Sink input can be as high as 5V and then HPD_Source will output no higher than 3.3V.</td></tr>
<tr><td>8</td><td>SDA_SOURCE</td><td>I/O</td><td>3.3V DDC Data I/O. Pulled up by external termination to 3.3V.
<table>
<tr><th>DDC_EN</th><th>DDCBSEL</th><th>DDC level shifter type</th></tr>
<tr><td>Low</td><td>X</td><td>DISABLE DDC level shifter</td></tr>
<tr><td>High</td><td>Low</td><td>Passive level shifter ENABLE<br>Connected to SDA_SINK through voltage-limiting integrated NMOS passgate</td></tr>
<tr><td>High</td><td>High</td><td>Active level shifter ENABLE<br>Connected to SDA_SINK through bi-direction buffer</td></tr>
</table></td></tr>
<tr><td>9</td><td>SCL_SOURCE</td><td>I/O</td><td>3.3V DDC Data I/O. Pulled up by external termination to 3.3V.
<table>
<tr><th>DDC_EN</th><th>DDCBSEL</th><th>DDC level shifter type</th></tr>
<tr><td>Low</td><td>X</td><td>DISABLE DDC level shifter</td></tr>
<tr><td>High</td><td>Low</td><td>Passive level shifter ENABLE<br>Connected to SCL_SINK through voltage-limiting integrated NMOS passgate</td></tr>
<tr><td>High</td><td>High</td><td>Active level shifter ENABLE<br>Connected to SCL_SINK through bi-direction buffer</td></tr>
</table></td></tr>
<tr><td>10</td><td>DDCBSEL</td><td>I</td><td>Active DDC level shifter enable pin. (internal 200KΩ pull-LOW)
<table>
<tr><th>DDCBSEL</th><th>DDC path</th></tr>
<tr><td>Low (0V)</td><td>Passive DDC level shifter</td></tr>
<tr><td>High (3.3V)</td><td>Active DDC level shifter</td></tr>
</table></td></tr>
<tr><td>13</td><td>OUT_D4+</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4-.</td></tr>
<tr><td>14</td><td>OUT_D4-</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4+</td></tr>
<tr><td>16</td><td>OUT_D3+</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3-.</td></tr>
<tr><td>17</td><td>OUT_D3-</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3+</td></tr>
</table>

<table>
<tr><th>Pin</th><th>Name</th><th>I/O Type</th><th>Descriptions</th></tr>
<tr><td>19</td><td>OUT_D2+</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2-.</td></tr>
<tr><td>20</td><td>OUT_D2-</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D2- makes a differential output signal with OUT_D2+</td></tr>
<tr><td>22</td><td>OUT_D1+</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-.</td></tr>
<tr><td>23</td><td>OUT_D1-</td><td>O</td><td>HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+</td></tr>
<tr><td>25</td><td>OE#</td><td>I</td><td>Enable for level shifter path.
<table>
<tr><td>OE#</td><td>IN_D Termination</td><td>OUT_D Outputs</td></tr>
<tr><td>1</td><td>> 100KΩ</td><td>High-Z</td></tr>
<tr><td>0</td><td>50Ω</td><td>Active</td></tr>
</table></td></tr>
<tr><td>28</td><td>SCL_SINK</td><td>I/O</td><td>5V DDC Clock I/O. Pulled up by external termination to 5V.
<table>
<tr><td>DDC_EN</td><td>DDCBSEL</td><td>DDC level shifter type</td></tr>
<tr><td>Low</td><td>X</td><td>DISABLE DDC level shifter</td></tr>
<tr><td>High</td><td>Low</td><td>Passive level shifter ENABLE<br>Connected to SCL_SOURCE through voltage-limiting integrated NMOS passgate</td></tr>
<tr><td>High</td><td>High</td><td>Active level shifter ENABLE<br>Connected to SCL_SOURCE through bi-direction buffer</td></tr>
</table></td></tr>
<tr><td>29</td><td>SDA_SINK</td><td>I/O</td><td>5V DDC Data I/O. Pulled up by external termination to 5V.
<table>
<tr><td>DDC_EN</td><td>DDCBSEL</td><td>DDC level shifter type</td></tr>
<tr><td>Low</td><td>X</td><td>DISABLE DDC level shifter</td></tr>
<tr><td>High</td><td>Low</td><td>Passive level shifter ENABLE<br>Connected to SDA_SOURCE through voltage-limiting integrated NMOS passgate</td></tr>
<tr><td>High</td><td>High</td><td>Active level shifter ENABLE<br>Connected to SDA_SOURCE through bi-direction buffer</td></tr>
</table></td></tr>
<tr><td>30</td><td>HPD_SINK</td><td>I</td><td>Low Frequency, 0V to 5V (nominal) input signal. This signal comes from the TMDS connector. Voltage High indicates “plugged” state; voltage low indicated “unplugged”. HPD_SINK is pulled down by an integrated 100K ohm pull-down resistor.</td></tr>
<tr><td>32</td><td>DDC_EN</td><td>I</td><td>Enables DDC level shifter path
<table>
<tr><td>DDC_EN</td><td>Passgate</td></tr>
<tr><td>Low (0V)</td><td>Disable</td></tr>
<tr><td>High (3.3V)</td><td>Enable</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin</th><th>Name</th><th>I/O Type</th><th>Descriptions</th></tr>
<tr><td>34</td><td>SQSEL</td><td>I</td><td>TMDS clock detection setting<br>Pulled up by external termination to 3.3V or short to GND.
<table>
<tr><td>SQSEL</td><td>Clock Monitor Pin</td></tr>
<tr><td>0</td><td>Device monitor HDMI pixel clock on Pin38/39<br>(Channel IN_D1±)</td></tr>
<tr><td>1</td><td>Device monitor DVI pixel clock on Pin 47/48<br>(Channel IN_D4±)</td></tr>
</table></td></tr>
<tr><td>38</td><td>IN_D1-</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D1- makes a differential pair with IN_D1+.</td></tr>
<tr><td>39</td><td>IN_D1+</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D1+ makes a differential pair with IN_D1-.</td></tr>
<tr><td>41</td><td>IN_D2-</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D2- makes a differential pair with IN_D2+.</td></tr>
<tr><td>42</td><td>IN_D2+</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D2+ makes a differential pair with IN_D2-.</td></tr>
<tr><td>44</td><td>IN_D3-</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D3- makes a differential pair with IN_D3+.</td></tr>
<tr><td>45</td><td>IN_D3+</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D3+ makes a differential pair with IN_D3-.</td></tr>
<tr><td>47</td><td>IN_D4-</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D4- makes a differential pair with IN_D4+.</td></tr>
<tr><td>48</td><td>IN_D4+</td><td>I</td><td>Low-swing diff input from DP Tx outputs. IN_D4+ makes a differential pair with IN_D4-.</td></tr>
</table>

## Truth Table (Slew Rate control function)

| SR1 | SR0 | Rise/Fall Time (Typ) |
|---|---|---|
| 1 | 1 | 140ps |
| 1 | 0 | 130ps |
| 0 | 1 | 120ps |
| 0 | 0 | 110ps |

## Test Setup Condition

$V_{DD}$ = 3.3V, Ambient temperature 25°C

Rise/Fall time is from 20% to 80% on Rising/Falling edge

Date rate: 620 Mbps

Input: 1V differential peak-to-peak clock pattern

Equalization : 3dB

## Table 1: OE Pin Description

| OE# | Device State | Comments |
|---|---|---|
| Asserted (low voltage) | Differential input buffers and output buffers enabled. Input impedance = 50Ω | Normal functioning state for IN_D to OUT_D level shifting function. |
| Unasserted (high voltage) | Low-power state.<br>▫ Differential input buffers and termination are disabled.<br>▫ Differential inputs are in a high impedance state.<br>▫ OUT_D level-shifting outputs are disabled.<br>▫ OUT_D level-shifting outputs are in high impedance state.<br>▫ Internal bias currents are turned off. | Intended for lowest power condition when:<br>▫ No display is plugged in or<br>▫ The level shifted data path is disabled HPD_SINK input and HPD_SOURCE output are not affected by OE# SCL_ SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE# |

## Absolute Maximum Ratings (Over operating free-air temperature range)

| Item | Rating |
|---|---|
| Supply Voltage to Ground Potential | 5.5V |
| All Inputs and Outputs | -0.5V to $V_{DD}$+0.5V |
| Ambient Operating Temperature | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 150°C |
| Soldering Temperature | 260°C |

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

## Electrical Characteristics

**Table: Power Supplies and Temperature Range**

| Symbol | Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{DD}$ | 3.3V Power supply | 3.0 | 3.3 | 3.6 | V | |
| $I_{CC}$ | Max Current | | | 100 | mA | |
| $I_{CC_squelch}$ | Supply Current when no TMDS clock present | | 8 | | mA | |
| $I_{CCQ}$ | Standby Current | | | 2 | mA | OE# = HIGH |
| $T_{CASE}$ | Case temperature range for operation with spec. | -40 | | 85 | Celsius (°) | |

**Table: Differential Input Characteristics forIN_Dx signals**

| Symbol | Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{bit}$ | UI, Unit Interval | 360 | | | ps | $T_{bit}$ is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal Tbit at 2.5 Gbps = 400 ps. 360ps = 400ps-10% |
| $V_{RX_DIFF}$ | Input Differential Voltage Level | 0.175 | | 1.200 | V | See note 1 below |
| $T_{RX_EYE}$ | Minimum Eye Width at IN_D input pair | 0.8 | | | Tbit | |
| $V_{CM\text{-}ACp\text{-}p}$ | AC Peak Common Mode Input Voltage | | | 100 | mV | See note 2 below |
| $Z_{RX_DC}$ | | 40 | 50 | 60 | Ω | Required IN_D+ as well as IN_D- DC impedance (50 ±20% tolerance). |
| $Z_{RX\text{-}Bias}$ | | 0 | | 2.0 | V | Intended to limit power-up stress on chipset's PCIE output buffers. |
| $Z_{RX_HIGH\text{-}Z}$ | | 100 | | | k Ω | Differential inputs must be in a high impedance state when OE# is HIGH. |

**1. $V_{RX\text{-}DIFF} = 2x|V_{RX\text{-}D\text{-}} - V_{RX\text{-}D\text{-}}|$ Applies to IN_Dx signals**

**2. $V_{CM\text{-}AC\text{-}p\text{-}p} = |V_{RX\text{-}D\text{-}} - V_{RX\text{-}D\text{-}}|/2 - V_{RX\text{-}CM\text{-}DC}$**

**$V_{RX\text{-}CM\text{-}DC}$ = DC(avg) of $|V_{RX\text{-}D+} + V_{RX\text{-}D\text{-}}|/2$**

**$V_{CM\text{-}AC\text{-}p\text{-}p}$ includes all frequencies above 30 kHz.**

### TMDS Outputs

The level shifter's TMDS outputs are required to meet HDMI 1.3 specifications.

The HDMI 1.3 Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

**Table 2: Differential Output Characteristics for TMDS_OUT signals**

| Symbol | Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_H$ | Single-ended high level output voltage | $V_{DD}$-10mV | $V_{DD}$ | $V_{DD}$+10mV | V | $V_{DD}$ is the DC termination voltage in the HDMI or DVI Sink. $V_{DD}$ is nominally 3.3V |
| $V_L$ | Single-ended low level output voltage | $V_{DD}$-600mV | $V_{DD}$-500mV | $V_{DD}$-400mV | V | The open-drain output pulls down from $V_{DD}$. |
| $V_{SWING}$ | Single ended output swing voltage | 425 | 500 | 600 | mV | Swing down from TMDS termination voltage (3.3V ±10%) |
| $I_{OFF}$ | Single-ended current in high-Z state | | | 50 | µA | Measured with TMDS outputs pulled up to $V_{DD}$ Max _(3.6V) through 50Ω resistors. |
| $T_{SKEW-INTRA}$ | Intra-pair differential skew | | | 30 | ps | This differential skew budget is in addition to the skew presented between D+ and D- paired input pins. HDMI revision 1.3 source allowable intrapair skew is 0.15 $T_{bit}$. |
| $T_{SKEW-INTER}$ | Inter-pair lane-to-lane output skew | | | 100 | ps | This lane-to-lane skew budget is in addition to skew between differential input pairs |
| $T_{JIT}$ | Jitter added to TMDS signals | | | 25 | ps | Jitter budget for TMDS signals as they pass through the level shifter. 25ps = 0.056 at 2.25 Gbps |

**TMDS output oscillation elimination**

The inputs already incorporate a squelch circuit. Therefore, nothing is needed from application standpoint to eliminate TMDS output oscillation when there is no TMDS input present. The IC will do this automatically.

**Table 3: HPD Characteristics**

| Symbol | Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{IH-HPD}$ | Input High Level | 2.0 | 5.0 | 5.3 | V | Low-speed input changes state on cable plug/unplug |
| $V_{IL-HPD}$ | HPD_SINK Input Low Level | 0 | | 0.8 | V | |
| $I_{IN-HPD}$ | HPD_SINK Input Leakage Current | | | 70 | µA | Measured with HPD_SINK at $V_{IH-HPD}$ max and $V_{IL-HPD}$ min |
| $V_{OH-HPD}$ | HPD_source Output High-Level | 2.5 | | $V_{DD}$ | V | $V_{DD}$ = 3.3V ±10%<br>$I_{OH}$ = -4mA(MIN) / -8mA(MAX) |
| $V_{OL-HPD}$ | HPD_source Output Low-Level | 0 | | 0.4 | V | $I_{OL}$ = 4mA(MIN) / 8mA(MAX) |
| $T_{HPD}$ | HPD_SINK to HPD_source propagation delay | | | 200 | ns | Time from HPD_SINK changing state to HPD_source changing state. Includes HPD_source rise/fall time |
| $T_{RF-HPDB}$ | HPD_source rise/ fall time | 1 | | 20 | ns | Time required to transition from $V_{OH-HPDB}$ to $V_{OL-HPDB}$ or from $V_{OL-HPDB}$ to $V_{OH-HPDB}$ |

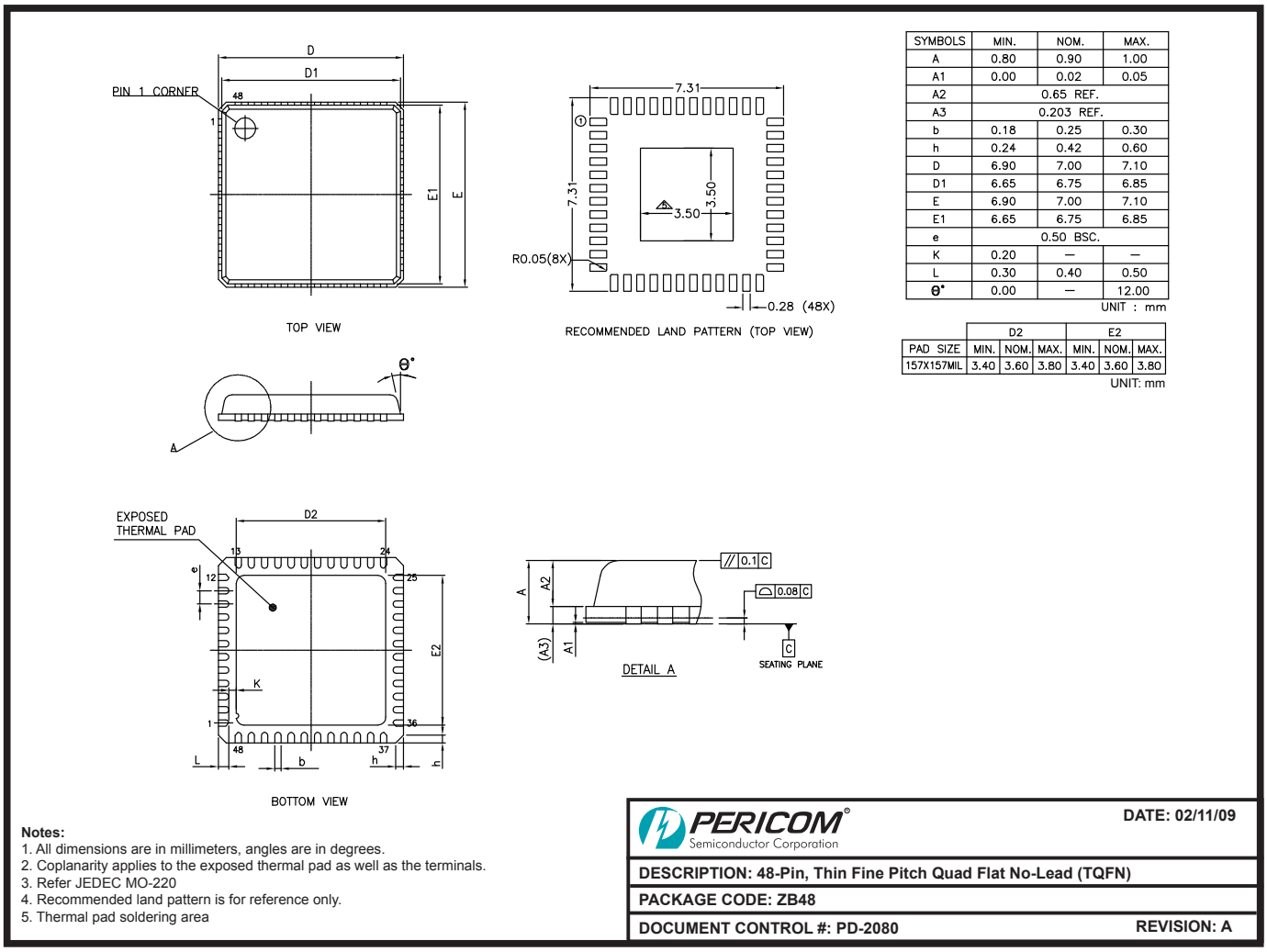
**Table 4: OE# Input, SQSEL and DDC_EN**

| Symbol | Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | 2.0 | | $V_{DD}$ | V | TMDS enable input changes state on cable plug/unplug |
| $V_{IL}$ | Input Low Level | 0 | | 0.8 | V | |
| $I_{IN}$ | Input Leakage Current | | | 10 | µA | Measured with input at $V_{IH-EN}$ max and $V_{IL-EN}$ min |

**Table 5: Termination Resistor**

| Symbol | Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $R_{HPD}$ | HPD_SINK input pull-down resistor. | 100K | | | Ω | Guarantees HPD_SINK is LOW when no display is plugged in. |

## Packaging Mechanical: 48-Pin TQFN (ZB)




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | | 0.65 REF. | |
| A3 | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| h | 0.24 | 0.42 | 0.60 |
| D | 6.90 | 7.00 | 7.10 |
| D1 | 6.65 | 6.75 | 6.85 |
| E | 6.90 | 7.00 | 7.10 |
| E1 | 6.65 | 6.75 | 6.85 |
| e | | 0.50 BSC. | |
| K | 0.20 | — | — |
| L | 0.30 | 0.40 | 0.50 |
| θ° | 0.00 | — | 12.00 |

UNIT : mm

| | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| PAD SIZE | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| 157X157MIL | 3.40 | 3.60 | 3.80 | 3.40 | 3.60 | 3.80 |

UNIT: mm

**Notes:**
1. All dimensions are in millimeters, angles are in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area

PERICOM Semiconductor Corporation

**DATE: 02/11/09**

**DESCRIPTION: 48-Pin, Thin Fine Pitch Quad Flat No-Lead (TQFN)**

**PACKAGE CODE: ZB48**

**DOCUMENT CONTROL #: PD-2080** **REVISION: A**

09-0091

**Note:**

**1.For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics**

**2.The exposed die paddle size is 3.6x3.6mm for PI3VDP411LSAZBE**

**3. Pad size (D2 * E2) is 157 x 157 mm**



All trademarks are property of their respective owners.

## Related Products

| Part Number | Product Description |
|---|---|
| PI3EQXDP1201 | DisplayPort 1.2 Re-driver with built-in AUX listener |
| PI3VDP1430 | Dual Mode DisplayPort to HDMI Level Shifter and Re-driver |
| PI3HDMI511 | 3.4G HDMI1.4 Re-driver for Source-side application, supporting Dual Mode DisplayPort |
| PI3HDMI611 | 3.4G HDMI1.4 Re-driver for Sink-side application, supporting Dual Mode DisplayPort |
| PI3VDP3212 | 2-Lane DisplayPort1.2 Compliant Switch |
| PI3VDP12412 | 4-Lane DisplayPort1.2 Compliant Switch |
| PI3HDMI412AD | 1:2 Active 3.4Gbps HDMI1.4 compliant Splitter/Re-driver |
| PI3HDMI521 | 2:1 3.4Gbps HDMI1.4 Switch/Re-driver with built-in ARC and Fast Switching support for Sink Application |
| PI3HDMI621 | 2:1 3.4Gbps HDMI1.4 Switch/Re-driver with built-in ARC and Fast Switching support for Sink Application |
| PI3HDMI336 | 3:1 Active 3.4Gbps HDMI Switch/Re-driver with $I^2C$ control and ARC Transmitter |

## Reference Information

| Document | Description |
|---|---|
| VESA | VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010<br>VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012<br>VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009 |
| HDMI | High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009 |

## Ordering Information

| Ordering Code | Package Code | Package Type |
|---|---|---|
| PI3VDP411LSAZBE | ZB | Pb-free & Green, 48-pin TQFN |

1. **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
2. **E = Pb-free and Green**
3. **Adding an X suffix = Tape/Reel**

## Revision History

| Date | Changes |
|---|---|
| 7/28/2012 | Actual pad size 157 x 157 mil in package drawing |