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DP/HDMI 1:2 De-multiplexer switches

Features

- DP/HDMI 1:2 De-multiplexer switch with 4 high speed differential channel and AUX/DDC, HPD and CAB_DET signal channels
- One passive output ports for DP1.2 at 5.4Gbps
- One active output port with integrated DP to HDMI re-driver (level shifter) supports HDMI 1.4 at 3.4Gbps
- Pin control mode supports auto port priority selection only
- Pin control mode supports port2 with DDC bi-direction buffer switch only
- I2C control mode supports both auto and manual port priority selection
- I2C control mode supports port2 with 8 levels equalization and 5 levels pre-emphasis
- I2C control mode supports port2 with either DDC bi-direction buffer switch or DDC passive switch
- Very low operating power when passive port1 is selected
- 3.3V power supply
- 2KV HBM ESD protection for all I/O pins of port1 and all control pins
- 8kV contact ESD (IEC61000-4-2) protection for all output pins in port2
- Packaging:

  60 pin TQFN package (5x9mm, 0.4mm pitch)

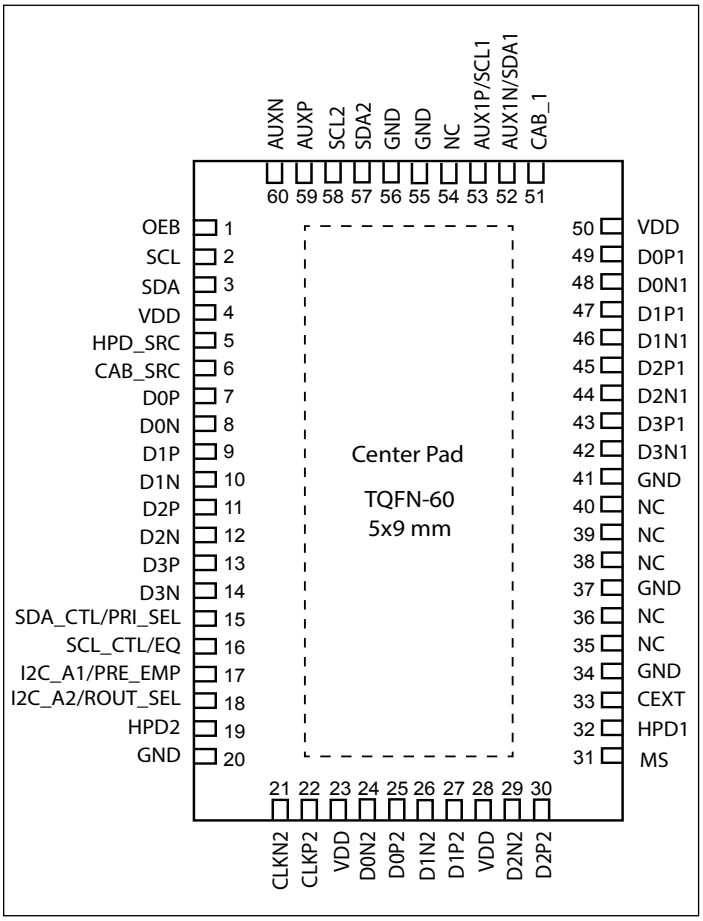
Description

PI3WVR31212 has one passive output port1, one active (DP to HDMI) output port2. Passive output supports DP1.2 at 5.4Gbps in I2C mode. Active port2 supports HDMI1.4b at 3.4Gbps.All two output ports support auto port priority selection. Input port accepts DP1.2 and HDMI2.0 (I2C control mode only) signals associated with output ports as described above.

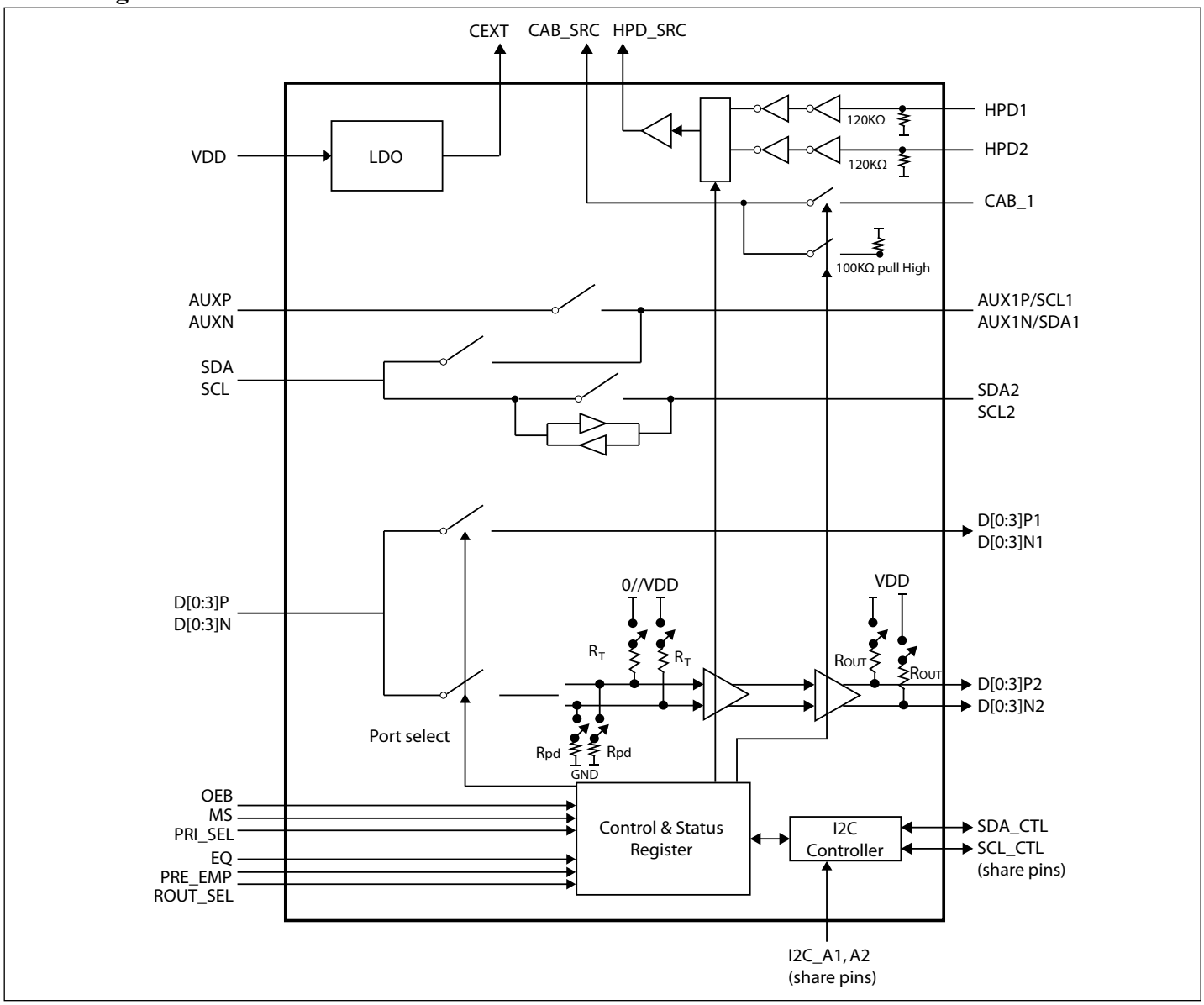
Application

- Notebook

Pin Configuration: TQFN-60



Block Diagram



Pin Description

pin#	pin Name	Signal Type	Description
7	D0P	IO	4 differential pair input (DP)
9	D1P		
11	D2P		
13	D3P		
8	D0N		
10	D1N		
12	D2N		
14	D3N		
49	D0P1	IO	4 differential pair output (DP) for port 1
47	D1P1		
45	D2P1		
43	D3P1		
48	D0N1		
46	D1N1		
44	D2N1		
42	D3N1		
25	D0P2	IO	4 differential pair output (HDMI) for port 2
27	D1P2		
30	D2P2		
22	CLKP2		
24	D0N2		
26	D1N2		
29	D2N2		
21	CLKN2		
52	AUX1N/SDA1	IO	AUX (DP) or DDC (HDMI) to three ports
53	AUX1P/SCL1		
57	SDA2		
58	SCL2		
60	AUXN	IO	AUX to DP-source
59	AUXP		
3	SDA	IO	DDC to DP-source
2	SCL		
32	HPD1	I	HPD1-2 for port1-2; HPD_SRC to DP-source.
19	HPD2	I	
5	HPD_SRC	O	

pin#	pin Name	Signal Type	Description
51 6	CAB_1 CAB_SRC	IO	CAB_1: CAB_DET to port1 CAB_SRC: CAB_DET to DP-source No CAB_DET for HDMI port2
1	OEB	I	OEB=0, device active; OEB=1, device shut down
15	SDA_CTL/PRI_SE	I	MS=0, PRI_SEL selects priority in pin control mode; MS=1, SDA_CTL as SDA in I2C control mode
16	SCL_CTL/EQ	IO	MS=0, EQ selects equalization in pin control mode; MS=1, SCL_CTL as SCL in I2C control mode
17	I2C_A1/PRE_EMP	I	MS=0, PRE_EMP selects Pre-emphasis in pin control mode; MS=1, I2C_A1 as I2C address A1 in I2C control mode
18	I2C_A2/ROUT_SEL	I	MS=0, ROUT_SEL selects source termination in pin control mode; MS=1, I2C_A2 as I2C address A2 in I2C control mode
31	MS	I	Mode Select: MS=0 for pin control mode MS=1 for I2C control mode
33	CEXT	O	Internal LDO bypass capacitance, 4.7uf to GND
4,23,28,50	VDD	Power	3.3V VDD
20,34,37,41,55,56, Center Pad	GND	Ground	Bottom GND EPAD
35,36,38,39,40,54	NC	NC	Not Connected

Pin mapping for dual mode DP source DEMUX to DP output

DP mode	HDMI/DVI mode	WVR31212 input pins	WVR31212 port1 output	WVR31212 port2 output
ML_lan0(P)	TX2+	D0P	D0P1	D2P2
ML_lan0(N)	TX2-	D0N	D0N1	D2N2
ML_lan1(P)	TX1+	D1P	D1P1	D1P2
ML_lan1(N)	TX1-	D1N	D1N1	D1N2
ML_lan2(P)	TX0+	D2P	D2P1	D0P2
ML_lan2(N)	TX0-	D2N	D2N1	D0N2
ML_lan3(P)	TXC+	D3P	D3P1	CLKP2
ML_lan3(N)	TXC-	D3N	D3N1	CLKN2

Function Description

The MS pin selects I2C or pin control mode.

The default input is DP in pin control mode and can be switched between DP or HDMI in I2C control mode.

Pin control mode has only automatic port selection. I2C control mode has both automatic and manual port selection.

In auto port selection, when only one HPD high detected, the port with HPD high will be selected. When multiple HPD high detected, the PRI_SEL pin (priority select) will determine the priority of the 2 ports. See priority selection table

When PRI_SEL=low or High, the port-priority will be port1-port2 from high to low; when PRI_SEL=M (open as not connected), the port priority will be port2-por1 from high to low.

When port 1 is selected and CAB_1 is low as in DP mode, the AUX/DDC channels will work as AUX channels. AUXP shall have 100Kohm external resistor to GND and AUXN shall have 100Kohm external resistor to VDD. The data rate of AUX channels will be >720Mbps.The internal DDC switch will be off.

When port 1 is selected and CAB_1 is high when DP to HDMI adapter plugged, the AUX/DDC channels will work as DDC channels. The internal DDC channels are on and the AUX channels are off. The input of DDC channels can tolerate 5V input and voltage of DDC to source will be limited about 3.3V or below.

When port 1 is selected (passive ports), port2 with HDMI re-driver will shut down.

When port 2 is selected, the internal DP to HDMI level shifter will be enabled. There will be 3 EQ and 3 Pre-emphasis settings in pin control mode, 8 EQ and 5 Pre-emphasis settings in I2C control mode.

When port 2 is selected, HDMI output can be standard TMDS-open-drain source, as well to be selected with internal source termination as 50 ohm pull up to 3.3V VDD, using ROUT_SEL pin control or I2C control.

When port 2 is active as DP to HDMP level shifter, the DDC channel can be selected between bi-direction DDC buffer and passive DDC switch in I2C mode.

HPD1, HPD2 are with internal CMOS buffers and can support 3.3V and 5V HPD inputs.

Squelch Mode

Squelch function will disable HDMI data output (as high impedance)when the voltage and frequency of input clock (TMDS) are below squelch threshold, which will prevent random noise presenting in HDMI data output, thereby prevent noise on sink display. Squelch function will enable-resume HDMI data output when input clock signals are above squelch threshold.

Truth Table for TMDS port2

EQ – three level pin control
PRE-EMP – three level pin control

EQ	Equalization value
0	1.5dB
open	4.0dB
1	6.5dB

PRE_SEL	TX pre-emphasis
0	0dB
open	1.5dB
1	2.5dB

ROUT_SEL

ROUT_SEL	Pull-Up Resistors on port2 D[0:2]P2/N2, CLKP2/N2
0	No Pull-up resistors
1	50Ω Pull-up resistors to VDD
1	6.5dB

Truth Table for AUX and DDC

PORT	DP/HDMI	CAB_1	AUXP	AUXN	SCL	SDA
When Port1 Selected	DP Mode	0	AUX1P	AUX1N	Hi-Z	Hi-Z
	DP Mode	1	Hi-Z	Hi-Z	SCL1	SDA1
	HDMI Mode	x	Hi-Z	Hi-Z	SCL1	SDA1

Priority Selection Table

PRI_SEL (Priority order)	HPD1	HPD2	HPD_SRC	CAB_SRC	AUXP/AUXN	SDA/SCL
0 or 1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0 or 1	1	x	HPD1	CAB1	AUX1P/AUX1N	SDA1/SCL1
0 or 1	0	1	HPD2	High	Hi-Z	SDA2/SCL2
M	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	1	0	HPD1	CAB1	AUX1P/AUX1N	SDA1/SCL1
M	x	1	HPD2	High	Hi-Z	SDA2/SCL2

Note: M=internal half VDD when input=HiZ

PRI_SEL (Priority order)	HPD1	HPD2	D0P	D1P	D2P	D3P	D0N	D1N	D2N	D3N
0 or 1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0 or 1	1	x	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
0 or 1	0	1	D2P2	D1P2	D0P2	CLKP2	D2N2	D1N2	D0N2	CLKN2
M	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	1	0	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
M	x	1	D2P2	D1P2	D0P2	CLKP2	D2N2	D1N2	D0N2	CLKN2

Note: M=internal half VDD when input=HiZ

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
High Speed Channel Input Voltage (DP Mode)	–0.5V to 2V
High Speed Channel Input Voltage (HDMI Mode)	2.4V to 3.6V
DDC and HPD channels Input Voltage	–0.5V to 6V
DC Output Current	180mA
Power Dissipation	0.6W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operation Conditions

(V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	VDD supply current (Port1 active)	VDD=3.3V		1		mA
	VDD Supply Current (Port2 active)	Output Enable (open drain 500mv signal-end 0dB pre-emphasis, not including 40mA current to source)		100		mA
		Output Enable (double termination, 500mv signal-end 0dB pre-emphasis, not including 40mA current to source)		175		mA
I_{DDQ}	VDD Quiescent Supply Current (port2 active w/o TMDS input)	TMDS Output Disable,		5.0		mA
Istb	Standby mode by I2C	V_{DD}=3.6V, Port1selection, HPD_1 =0, MS=1, DP_HDMI=0		0.5		mA
		V_{DD}=3.6V, Port2 selection, HPD_3=0,		2.0		mA
Isd1	Supply shut down current when OEB disable (MS=0)	V_{DD}=3.6V,OEB=high		50		uA
Isd2	Supply shut down current when OEB disable (MS=1)	V_{DD}=3.6V,OEB=high		0.5		mA

DC Electrical Characteristics for Switching over Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
OEB,MS,ROUT_SEL						
I_{IH}	High level digital input current	V_{IH} =VDD	-10		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage		2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
HPD_SRC						
$V_{OL\_HPD\_SRC}$	Buffer Output Low Voltage	I_{OL} = 4 mA			0.4	V
$V_{OH\_HPD\_SRC}$	Buffer Output Low Voltage	I_{OH} = 4 mA	2.4			V
HPD_sink						
I_{IH}	High level digital input current(1)	V_{IH} =VDD	-10		40	µA
I_{IL}	Low level digital input current(1)	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
CAB						
I_{LK}	Input leakage current	Switch is off, Vin=5.5v	-50		50	uA
C_{IO}	Input/Output capacitance when-passive switch on			10		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
V_{pass}	Switch Output voltage	V_I=3.3V, I_I=100uA	1.5	3.0	3.3	V
CI(source)	Source side CAB capacitance	V_I peak-peak = 1V, 100 KHz		3.5	TBD	pF
CI(sink)	Sink side CAB capacitance when			6.5	TBD	pF
SDA/SCL, SDA1/SCL1						
I_{LK}	Input leakage current	DDC switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on	V_I peak-peak = 1V, 100 KHz		8		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
Vpass	Switch Output voltage	V_I=5.0V, I_I=100uA V_{DD}=3.3V	1.5	3.0	3.6	V
CI(source)	Source side DDC capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		2.8		pF
CI(sink)	Sink side DDC capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		5		pF
SDA2/SCL2 (DDC buffer of port2 active)						
V_{IH}	High level input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level input voltage		0		0.8	V
I_{LK}	Input leakage current	DDC switch is off, Vin = 5.5V	-10		10	uA

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level input current	V_{IL} = 0.2V	-10		10	µA
V_{OL}	Low level output voltage	I_{OL} = 4mA			0.2	V
I_{LOH}	HIGH-level output leakage current	V_O=3.6V			10	µA
C_{IO}	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V or 0V				pF
SDA/SCL (DDC buffer of port2 active)						
V_{IH}	High level input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level input voltage		0		0.4	V
I_{LK}	Input leakage current	DDC switch is off, Vin = 5.5V	-10		10	uA
I_{IL}	Low level input current	V_{IL} = 0.2V	-10		10	µA
V_{OL}	Low level output voltage	I_{OL} = 4mA	0.47	0.52	0.6	V
I_{LOH}	HIGH-level output leakage current	V_O=3.6V	5		10	µA
C_{IO}	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V or 0V		8		pF
AUXP,AUXN, AUXnP/SCLn, AUXnN/SDAn						
I_{LK}	Input leakage current	DDC switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on	V_I peak-peak = 1V, 100 KHz		6		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.3V		5		Ω
		I_O = 3mA, V_O = 3.0V		10		Ω
V_{pass}	Switch Output voltage	V_I=5.5V, I_I=100uA V_{DD}=3.3V		3.8	4	V
CI(source)	Source side capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		2.5	TBD	pF
CI(sink)	Sink side capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		3.5	TBD	pF
High Speed Channel (D[0:3]P/N – D[0:3]P1N1)						
V_{IK}	Clamp Diode Voltage (HS Channel)	V_{DD} = Max., I_{IN} = –18mA		–1.6	–1.8	V
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±10	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±10	
R_{ON_HS}	On resistance between input to out- put for high speed signals	V_{INPUT},cm = 0V to 1.8V, V_{INPUT},diff < 1.0Vp-p, diff, V_{DD} = 3.0V, I_{INPUT} =		8		Ohm
		V_{INPUT},cm = 2.2V to 3.1V, V_{INPUT},diff < 1.2Vp-p, diff, V_{DD} = 3.0V, I_{INPUT} = 20mA		8		Ohm

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
High Speed Channel (D[0:3]P/N – D[0:2]P2/N2; CLKP2/N2)						
V_I(open)	Single-ended input voltage under high impedance input or open input	I_L=10uA	VDD-10		VDD+10	mV
R_T	Input termination resistance	V_{IN}=2.9V	45	50	66	ohm
I_{OZ}	Leakage current resistance	V_{DD}=3.6V, OEB=High		30	100	uA
Ioff	Power off leakage current	V_{DD}=0, V_{IN}=3.6V	-50		50	uA

Dynamic Electrical Characteristics over Operating Range

(T_A = -40° to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
TMDS Differential Pins						
t_{pd}	Propagation delay	V_{DD} = 3.3V, Rout = 50Ω off, open drain, 0dB pre-emphasis			2000	ps
t_r	Differential output signal rise time (20% - 80%)					
t_f	Differential output signal fall time (20% - 80%)			120		
t_{sk}(p)	Pulse skew				50	
t_{sk}(D)	Intra-pair differential skew			120	50	
t_{sk}(o)	Inter-pair differential skew(2)			15	100	
T_{jit_clk}(pp)	Peak-to-peak output jitter CLK residual jitter	Data Input = 3.4 Gbps HDMI data pattern from signal generation, short trace. CLK Input = 340 MHz clock		23	40	
T_{jit_dat}(pp)	Peak-to-peak output jitter DATA Residual Jitter				50	
t_{en}	Enable time			10	10	us
t_{dis}	Disable time			25	50	
SCL,SDA channel, AUX channel , CAB channel : passive switches						
t_{pd}(DDC)	Propagation delay from SCLn/ SDAn to SCL/SDA or SCL/SDA to SCLn/SDAn In passive SW on.	C_L = 10pF, in passive switch			5	ns
SCL2,SDA2- SCL,SDA channel : buffers						
t_{PLH}	LOW-to-HIGH propagation delay	SCL/SDA to SCL2/SDA2	50	100	150	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL/SDA to SCL2/SDA2	10	20	40	ns
t_{PLH}	LOW-to-HIGH propagation delay	SCL2/SDA2 to SCL/SDA	50	100	150	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL2/SDA2 to SCL/SDA	10	20	40	ns

Control and Status Pins (HPDn, HPD_SRC)						
tpd(HPD)	Propagation delay (from HPDx to the active port of HPD_SRC, high to low)	CL = 10pF		2		us
tsx(HPD)	Switch time (from port select to the latest HPD , manual selection mode)			2		us

Dynamic Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
High Speed Channel (D[0:3]P/N – D[0:3]P1/N1)							
X_{TALK}	Crosstalk on High Speed Channels	See Fig. 1 for Measurement Setup	f= 2.7 GHz		-32	-30	dB
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup	f= 2.7 GHz		-19	-17	
I_{LOSS}	Differential Insertion Loss on High Speed Channels	@2.7GHZ (see figure 3)		-1.8	-1.6		dB
R_{loss}	Differential Return Loss on High Speed Channels	@ 2.7GHz (5.4Gbps)			-18.0	-16.0	dB
BW_Dx±	Bandwidth -3dB for Main high speed path (Dx±)	See figure 3		5.0	5.6		GHz
BW_AUX	Bandwidth -3dB for AUX	See figure 3		1.0	1.2		GHz
Tstartup	V_{DD} valid to channel enable					10	us
Twakeup	Enabling output by changing OEB from High to Low					10	us
T_{pd}	Propagation delay (input pin to output pin) on all channels				80		ps
t_{b-b}	Bit-to-bit skew within the same differential pair of Dx± channels				5	7	ps
t_{ch-ch}	Channel-to-channel skew of Dx± channels					35	ps

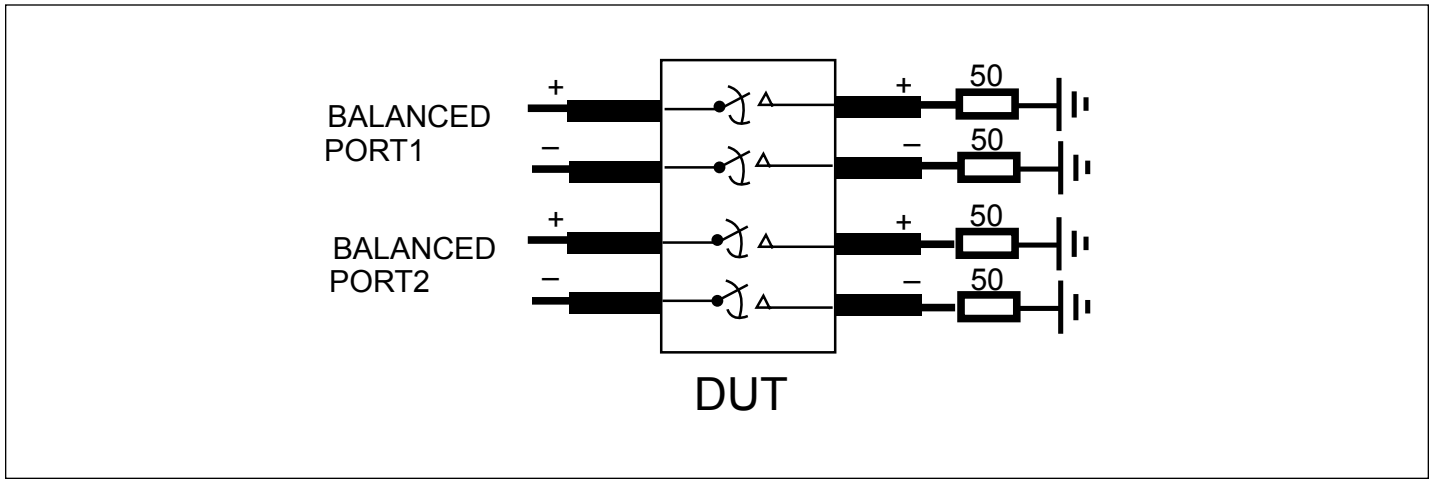


Fig 1. Crosstalk Setup

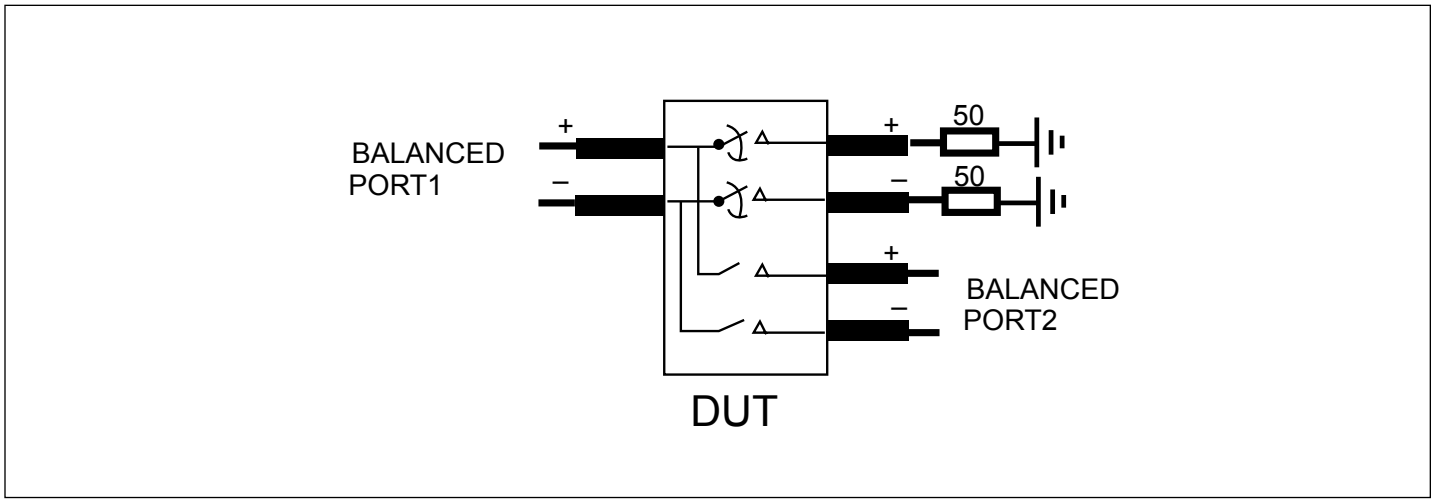


Fig 2. Off-isolation setup

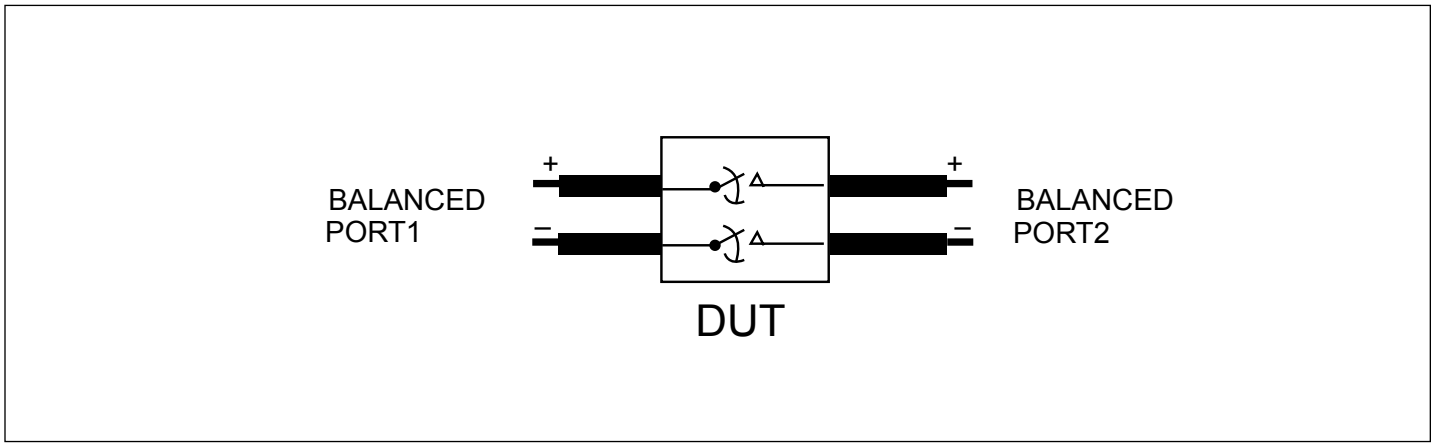


Fig 3. Differential Insertion Loss

HPD auto selection timing waveform

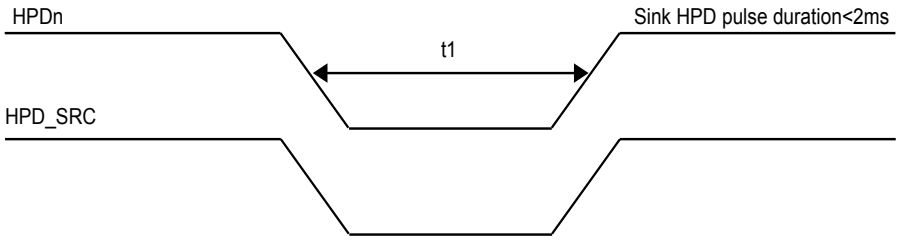


Fig 4. HPD timing t1

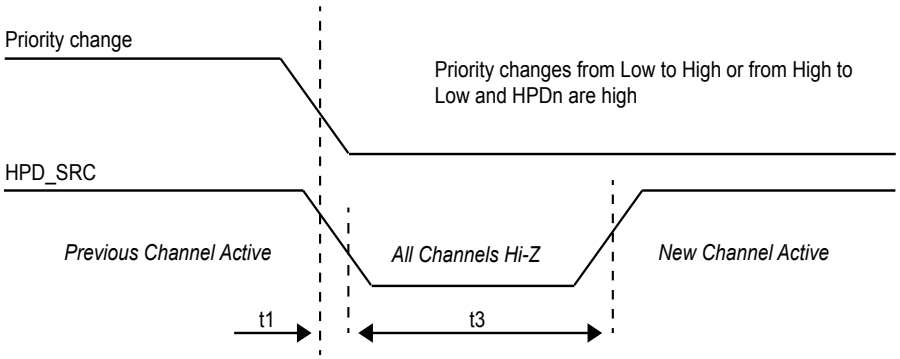


Fig 5. HPD timing t3

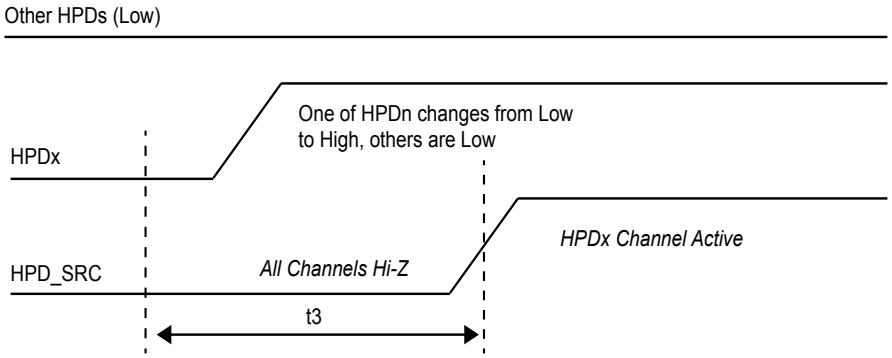


Fig 6. HPD timing t3

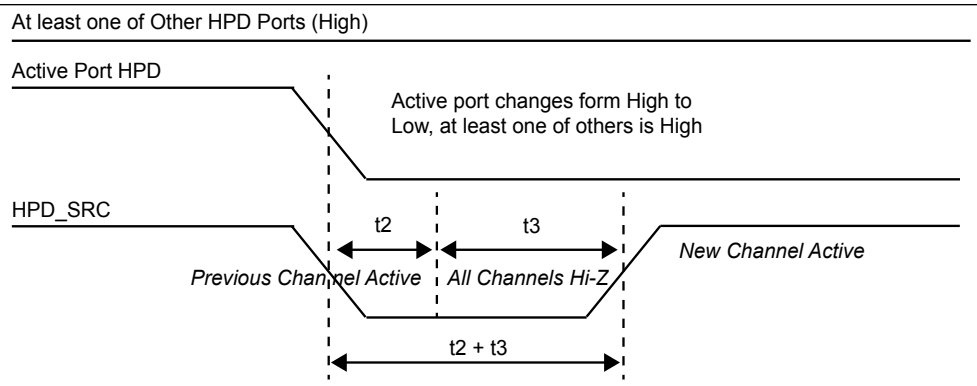


Fig 7. HPD timing

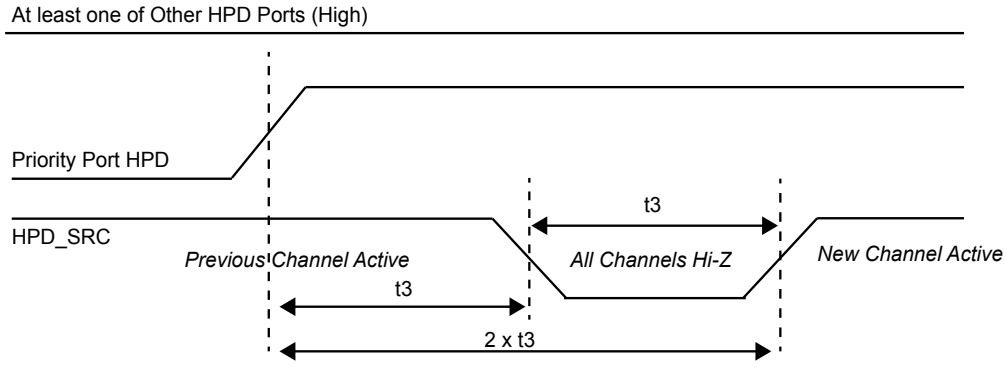


Fig 8. HPD timing

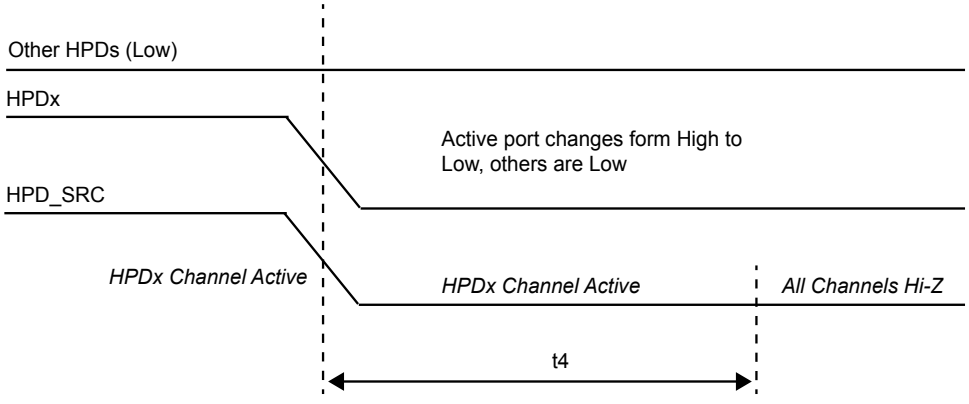


Fig 9. HPD timing t4

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HPD auto switching timing					
HPD pulse duration when treated as an IRQ –t1 (Figure 4)				2	ms
Propagation delay of HPDx Desertion –t2 (Figure 7)		50	125	200	ms
HPD_SRC low duration when the outputs are switched –t3(Figure 5,6,7,8); Propagation delay of HPDx assertion (Figure 8)		100	250	400	ms
Power down delay from HPDx de-assertion to chip power down –t4. (Figure 9)		400	1000	1600	ms

I2C Address Byte

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0 (R/W)
Address Byte	1	0	1	1	A2	A1	1	1/0*

* Read; 0:Write, A2 and A1 are two address bits setting

Data transmission format

Data is transmitted to the PI3WVR31212 registers using the Write mode as shown in Figure 1. Data is read from the PI3WVR31212 registers using the Read mode as shown in Figure 2.

Figure 1: I2C control register write condition

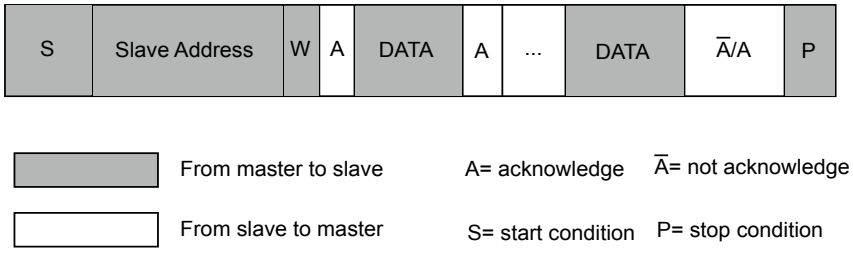
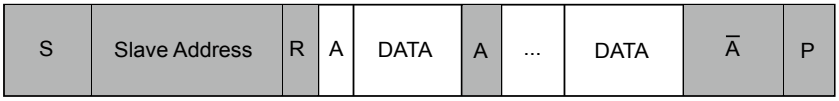


Figure 2: I2c control register read condition



I2C Control Register

The I2C control register uses index read or write for byte access.

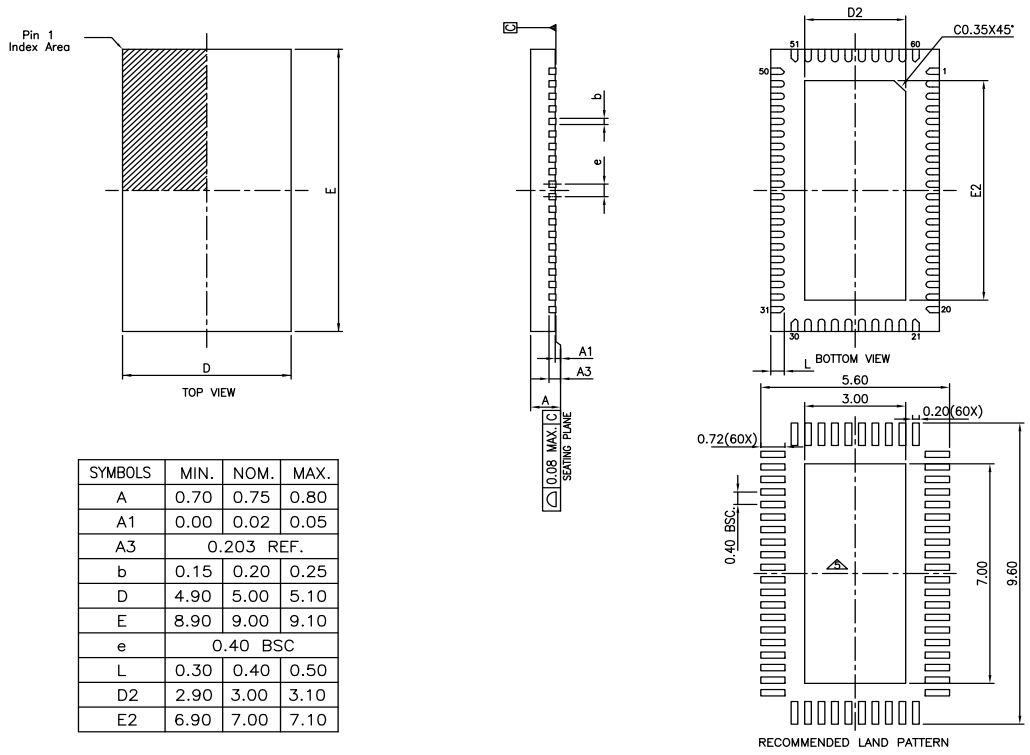
Offset	Name	Description	Power Up Condition	Type
0x00	CONFIG[7:0]	[7] Enable Standby 0: normal mode 1: standby mode In standby mode, all ports are powered down. [6:5] Port SEL1/SEL0 selection control 00 port 1 01all off 10 port 2 11 depends on priority selection [4:2] PRI_SEL priority selection control by HPDx 00x port1/port2 010 port1/port2 011 port2/port1 1xx port2/port1 [1] DP_HDMI selection control 0=DP input, 1=Reserved [0] Reserved	0x00	R/W

0x01	RX_SET[7:5] for port2; HPD auto selection time	[7:5] EQ programmable setting 000: 1.5 dB 001: 4 dB 010: 6.5 dB 011: 9 dB 100: 11.5 dB 101: 14 dB 110: 16.5 dB 111: 19 dB [4:3] HPD auto selection time source control 00: normal 01: -25% 10: +25% 11: test mode [2] HPD auto selection time t3 setting 0: 256ms 1: 128ms [1] HPD auto selection time t4 setting 0: 1024ms 1: 516ms [0] HPD pulse duration treated as IRQ time t1 setting 0: 2ms 1: 4ms	0x00	R/W

0x02	TX_SET[7:0] for port2	Output setting for HDMI re-driver/level shifter [7] HDMI output control 0: open drain 1: double termination [6:4] HDMI output Pre-emphasis settings 000: 0dB 001: 1.5dB 010: 2.5dB 011: 3.5dB 100: 6dB [3:2] TMDS output swing setting 00: 500mv as default 01: -10% 10: +10% 11: +20% [1] TMDS output slow rate setting 0: as default 1: +10% [0] Reserved to 0	0x00	R/W
0x03	Pericom ID	Pericom Vendor Register ID (refer to PCIE clock buffer) [7:4] Vendor ID 0101 [3:0] device revision 0001	0x51	R

0x04	HPDx/ CABx[6:0 Read only	[7] HPD_SRC output logic function (buffer) 0: HPD_SRC=HPDx 1: HPD_SRC=/HPDx [6] DDC function for port 2 0: Active buffer 1: passive switch [5] Port switching in manual selection 1: disable T3 time pulse when port switching, Port switch immediately 0: Enable T3 time pulse when port switching [4] Reserved [3] HPD2 status as read only [2] Reserved [1] HPD1 status as read only [0] Reserved for HPD1B	0x00	R/W [7:4] R [3:0]

Packaging Mechanical: ZL60



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	8.90	9.00	9.10
e		0.40 BSC	
L	0.30	0.40	0.50
D2	2.90	3.00	3.10
E2	6.90	7.00	7.10

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 04/08/14

DESCRIPTION: 60-Pin, TQFN 5X9mm

PACKAGE CODE: ZL (ZL60)

DOCUMENT CONTROL #: PD-2182 REVISION: –

14-0044

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR31212ZLE	ZL	60-Pin, (TQFN) 5X9mm

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging