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16-bit I²C-bus and SMBus low power I/O port with interrupt and reset

Features

- ➔ Operation power supply voltage from 2.3V to 5.5V
- ➔ 16-bit I²C-bus GPIO with interrupt and reset
- ➔ 5V tolerant I/Os
- ➔ Polarity inversion register
- ➔ Active LOW interrupt output
- ➔ Active LOW reset input
- ➔ Low current consumption
- ➔ 0Hz to 400KHz clock frequency
- ➔ Noise filter on SCL/SDA inputs
- ➔ Power-on reset
- ➔ ESD protection (4KV HBM and 1KV CDM)
- ➔ Offered in two different packages: TSSOP-24 and TQFN 4x4-24

Description

The PI4IOE5V9539 provide 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/ SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9539 consists of two 8-bit registers to configure the I/Os as either inputs or outputs, and two 8-bit polarity registers to change the polarity of the input port register data. The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

The PI4IOE5V9539 open-drain interrupt output is activated and indicate to the system when any input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The RESET pin causes the same reset/default I/O input configuration to occur without de-powering the device, holding the registers and I²C-bus state machine in their default state until the RESET input is once again HIGH.

Two hardware pins (A0, A1) vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus/SMBus.

Pin Configuration

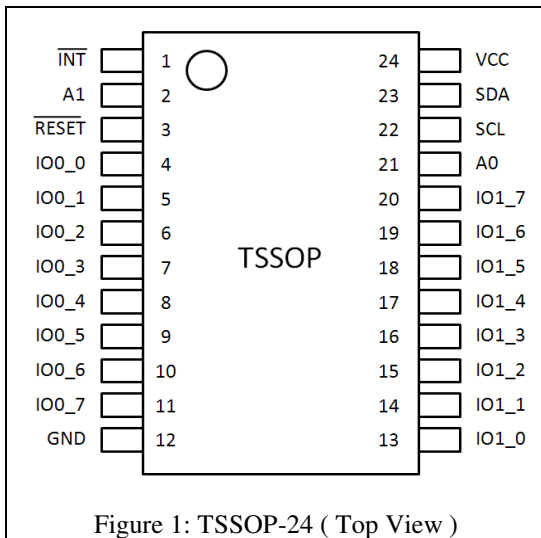


Figure 1: TSSOP-24 (Top View)

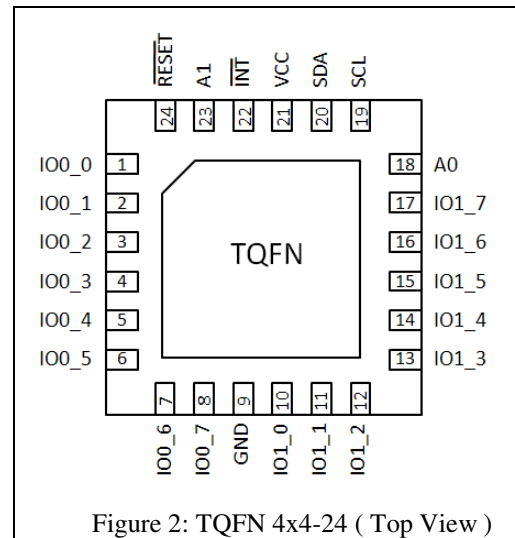


Figure 2: TQFN 4x4-24 (Top View)

Pin Description

Table 1: Pin Description

Pin		Name	Type	Description
TSSOP24	TQFN24			
1	22	$\overline{\text{INT}}$	O	Interrupt input (open-drain)
2	23	A1	I	Address input 1
3	24	$\overline{\text{RESET}}$	I	Active low reset pin. Driving this pin LOW causes: PI4IOE5V9539 to reset its state machine and register.
4	1	IO0_0	I/O	Port 0 input/output 0
5	2	IO0_1	I/O	Port 0 input/output 1
6	3	IO0_2	I/O	Port 0 input/output 2
7	4	IO0_3	I/O	Port 0 input/output 3
8	5	IO0_4	I/O	Port 0 input/output 4
9	6	IO0_5	I/O	Port 0 input/output 5
10	7	IO0_6	I/O	Port 0 input/output 6
11	8	IO0_7	I/O	Port 0 input/output 7
12	9	GND	G	Ground
13	10	IO1_0	I/O	Port 1 input/output 0
14	11	IO1_1	I/O	Port 1 input/output 1
15	12	IO1_2	I/O	Port 1 input/output 2
16	13	IO1_3	I/O	Port 1 input/output 3
17	14	IO1_4	I/O	Port 1 input/output 4
18	15	IO1_5	I/O	Port 1 input/output 5
19	16	IO1_6	I/O	Port 1 input/output 6
20	17	IO1_7	I/O	Port 1 input/output 7
21	18	A0	I	Address input 0
22	19	SCL	I	Serial clock line input
23	20	SDA	I	Serial data line open-drain
24	21	VCC	P	Supply voltage

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power supply.....	-0.5V to +6.0V
Voltage on an I/O pin.....	GND-0.5V to +6.0V
Input current.....	±20mA
Output current on an I/O pin.....	±50mA
Supply current.....	160mA
Ground supply current.....	200mA
Total power dissipation.....	200mW
Operation temperature.....	-40~85°C
Storage temperature.....	-65~150°C
Maximum Junction temperature, T _j (max).....	125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb = -40 °C to +85 °C; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I _{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; f _{SCL} = 100 kHz	-	135	200	μA
I _{sb}	Standby current	Standby mode; VCC = 5.5 V; no load; V _I = GND; f _{SCL} = 0 kHz; I/O = inputs	-	0.25	1	uA
		Standby mode; VCC = 5.5 V; no load; V _I = VCC; f _{SCL} = 0 kHz; I/O = inputs	-	0.25	1	μA
V _{POR}	Power-on reset voltage ^[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V _{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V _{IH}	High level input voltage		0.7VCC	-	5.5	V
I _{OL}	Low level output current	V _{OL} = 0.4V	3	-	-	mA
I _L	Leakage current	V _I = VCC = GND	-1	-	1	μA
C _i	Input capacitance	V _I = GND	-	6	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V _{IL}	Low level input voltage		-0.5	-	+0.81	V
V _{IH}	High level input voltage		+1.8	-	5.5	V
I _{OL}	Low level output current	VCC = 2.3 V to 5.5 V; V _{OL} = 0.5 V ^[2]	8	9	-	mA
		VCC = 2.3 V to 5.5 V; V _{OL} = 0.7 V ^[2]	10	11	-	mA
V _{OH}	High level output voltage	I _{OH} = -8mA; VCC = 2.3V ^[3]	1.8	-	-	V
		I _{OH} = -10mA; VCC = 2.3V ^[3]	1.7	-	-	V
		I _{OH} = -8mA; VCC = 3.0V ^[3]	2.6	-	-	V
		I _{OH} = -10mA; VCC = 3.0V ^[3]	2.5	-	-	V
		I _{OH} = -8mA; VCC = 4.75V ^[3]	4.1	-	-	V
		I _{OH} = -10mA; VCC = 4.75V ^[3]	4.0	-	-	V
I _{LIH}	High level input leakage current	VCC = 5.5V; V _I = VCC	-	-	1	μA
I _{LIL}	Low level input leakage current	VCC = 5.5V; V _I = GND	-	-	-1	μA
C _i	Input capacitance		-	3.7	10	pF
C _o	Output capacitance		-	3.7	10	pF
Interrupt $\overline{\text{INT}}$						
I _{OL}	Low level output current	V _{OL} = 0.4V	3	-	-	mA
Select inputs A0, A1 and $\overline{\text{RESET}}$						
V _{IL}	Low level input voltage		-0.5	-	+0.81	V
V _{IH}	High level input voltage		+1.8	-	5.5	V
I _L	Input leakage current		-1		1	μA

Note:
 [1]: VCC must be lowered to 0.2 V for at least 20 us in order to reset part.
 [2]: Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.
 [3]: The total current sourced by all I/Os must be limited to 160 mA.

Dynamic Characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I ² C		Fast mode I ² C		Unit
			Min	Max	Min	Max	
f _{SCL}	SCL clock frequency		0	100	0	400	kHz
t _{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t _{HD;STA}	hold time (repeated) START condition		4.0	-	0.6	-	μs
t _{SU;STA}	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t _{SU;STO}	set-up time for STOP condition		4.0	-	0.6	-	μs
t _{VD;ACK} ^[1]	data valid acknowledge time		-	3.45	-	0.9	μs
t _{HD;DAT} ^[2]	data hold time		0	-	0	-	ns
t _{VD;DAT}	data valid time		-	3.45	-	0.9	ns
t _{SU;DAT}	data set-up time		250	-	100	-	ns
t _{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	μs
t _{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t _f	fall time of both SDA and SCL signals		-	300	-	300	ns
t _r	rise time of both SDA and SCL signals		-	1000	-	300	ns
t _{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
t _{v(Q)}	Data output valid time ^[3]		-	200	-	200	ns
t _{su(D)}	Data input set-up time		150	-	150	-	ns
t _{h(D)}	Data input hold time		1	-	1	-	μs
Interrupt timing							
t _{v(INT)}	Valid time on pin $\overline{\text{INT}}$		-	4	-	4	μs
t _{rst(INT)}	Reset time on pin $\overline{\text{INT}}$		-	4	-	4	μs

Symbol	Parameter	Test Conditions	Standard mode I ² C		Fast mode I ² C		Unit
			Min	Max	Min	Max	
RESET timing							
$t_{w(rst)}$	Reset pulse width		25	-	25	-	ns
$t_{vrec(rst)}$	Reset recovery time ^[4]		0	-	0	-	ns
t_{rst}	Reset time		1	-	1	-	us

Note:

- [1]: $t_{VD:ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
- [2]: $t_{VD:DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
- [3]: $t_{v(Q)}$ measured from 0.7VCC on SCL to 50% I/O output.
- [4]: Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
Upon reset, the full delay will be the sum of t_{rst} and RC time constant of SDA bus.

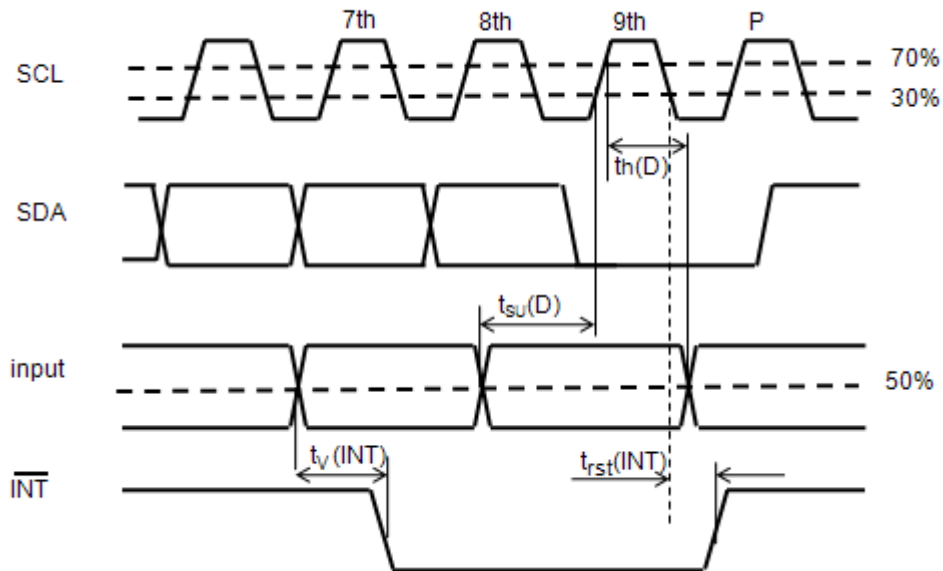
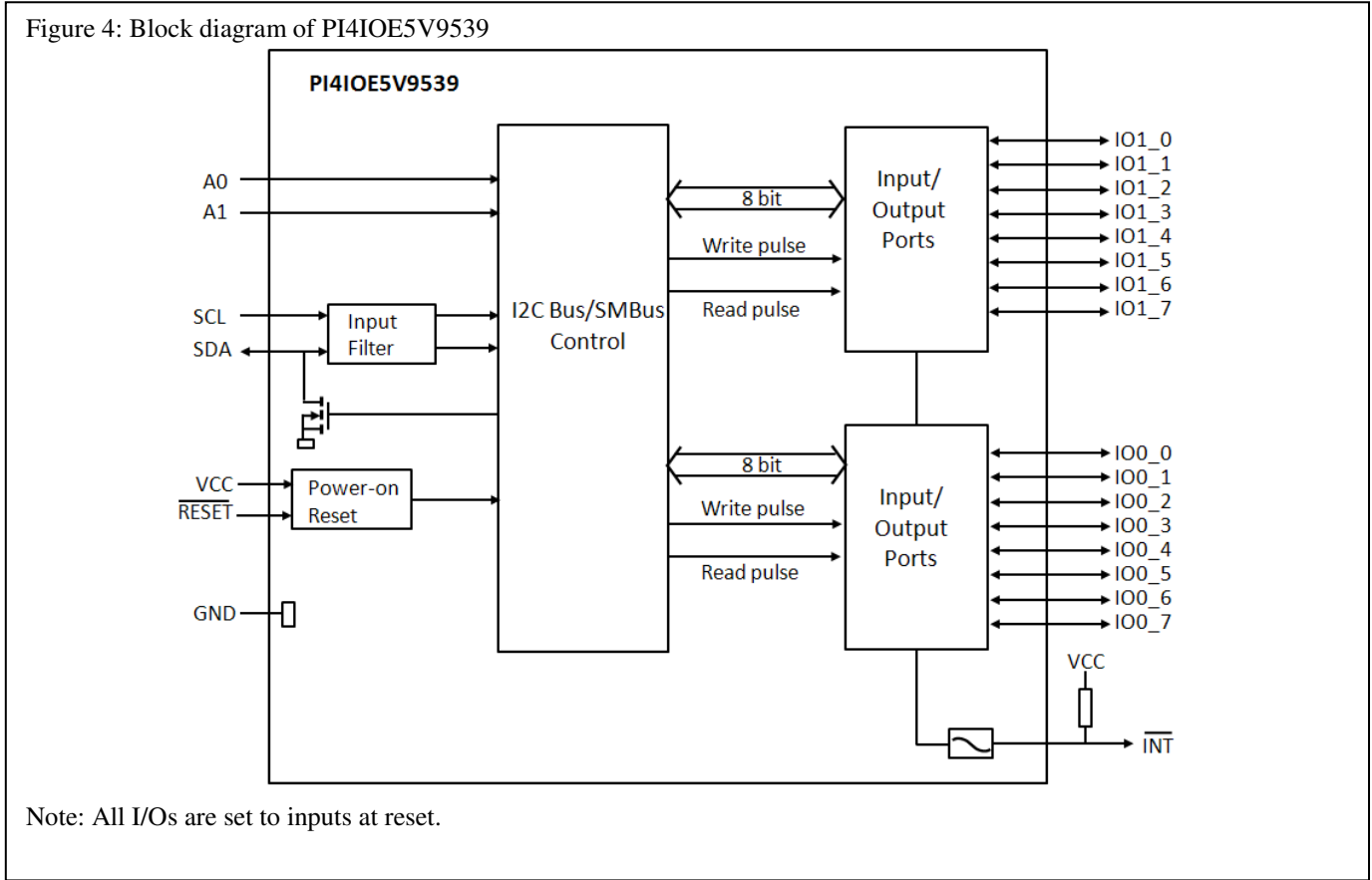


Figure 3: timing parameters for INT signal

PI4IOE5V9539 Block Diagram



Details Description

a. Device address

Table 4: Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	1	1	1	0	1	A1	A0	R/W

Note: Read “1”, Write “0”

b. Registers

i. Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 5: Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

ii. Register 0 and 1: input port registers

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Table 6: Input port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 7: Input port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

iii. Register 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 8: Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 9: Output port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

iv. Register 4 and 5: Polarity inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with ‘1’), the Input port data polarity is inverted. If a bit in this register is cleared (written with a ‘0’), the Input port data polarity is retained.

Table 10: Polarity Inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 11: Polarity Inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

v. Register 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with ‘1’), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with ‘0’), the corresponding port pin is enabled as an output. At reset, the IOs are configured as inputs.

Table 12: Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 13: Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

c. Power-on reset

When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9539 in a reset condition until VCC has reached V_{POR} . At that point, the reset condition is released and the PI4IOE5V9539 registers and SMBus state machine will initialize to their default states. Thereafter, VCC must be lowered below 0.2 V to reset the device. For a power reset cycle, VCC must be lowered below 0.2 V and then restored to the operating voltage.

d. $\overline{\text{RESET}}$ pin

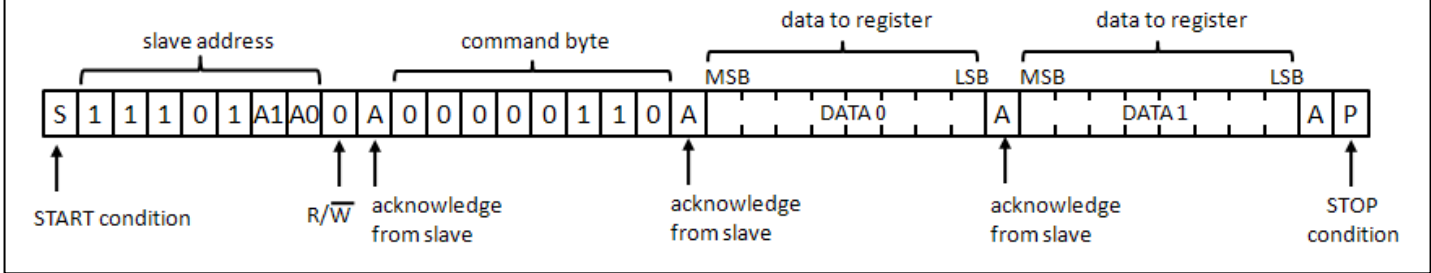
A reset can be accomplished by holding the RESET pin LOW for a minimum of $t_{w(rst)}$. In the PI4IOE5V9539 the registers and SMBus/I²C-bus state machine will be held in their default state until the RESET input is once again HIGH. This input typically requires a pull-up to VCC.

e. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above VCC to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

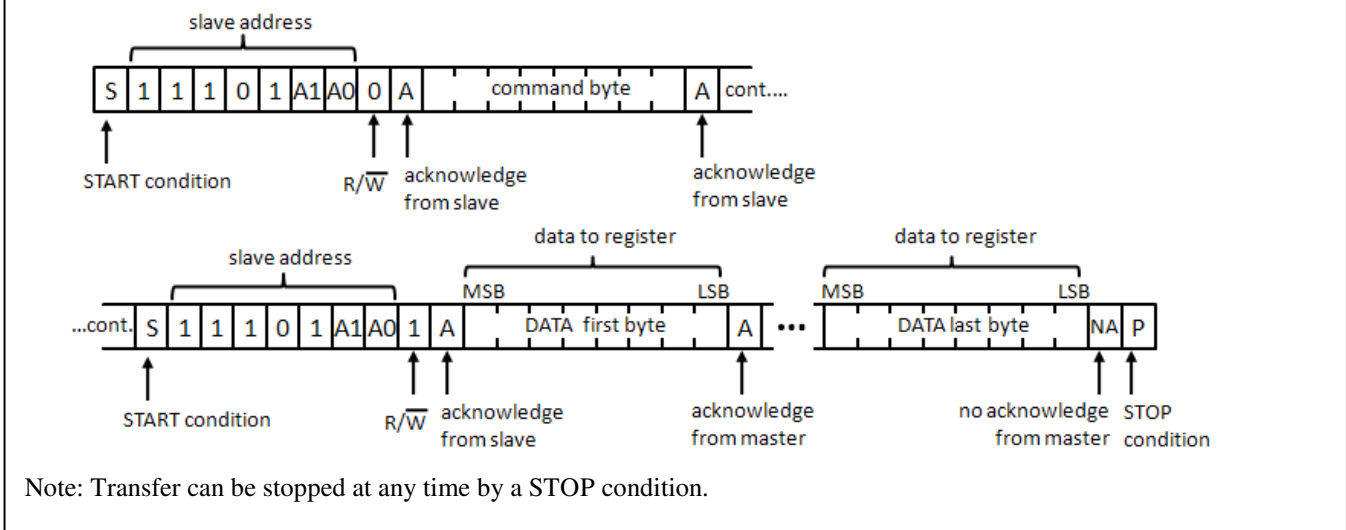
Figure 7: Write to configuration registers



ii. Reading the port registers

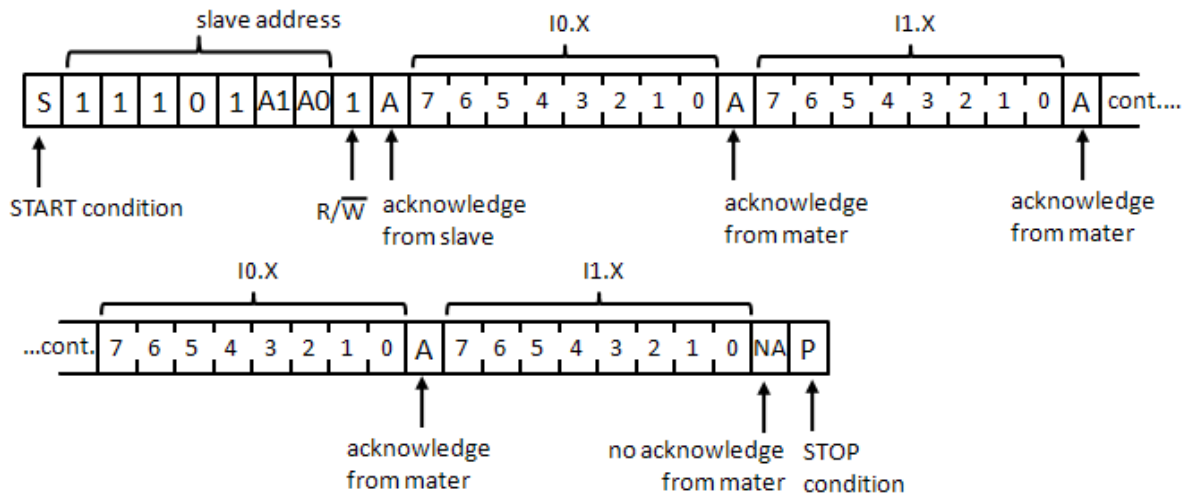
In order to read data from the PI4IOE5V9539, the bus master must first send the PI4IOE5V9539 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PI4IOE5V9539. Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input port 1, then the next byte read would be Input port 0. There is no limitation on the number of data bytes received in one read transmission.

Figure 8: Read from registers



Note: Transfer can be stopped at any time by a STOP condition.

Figure 9: Read Input port register



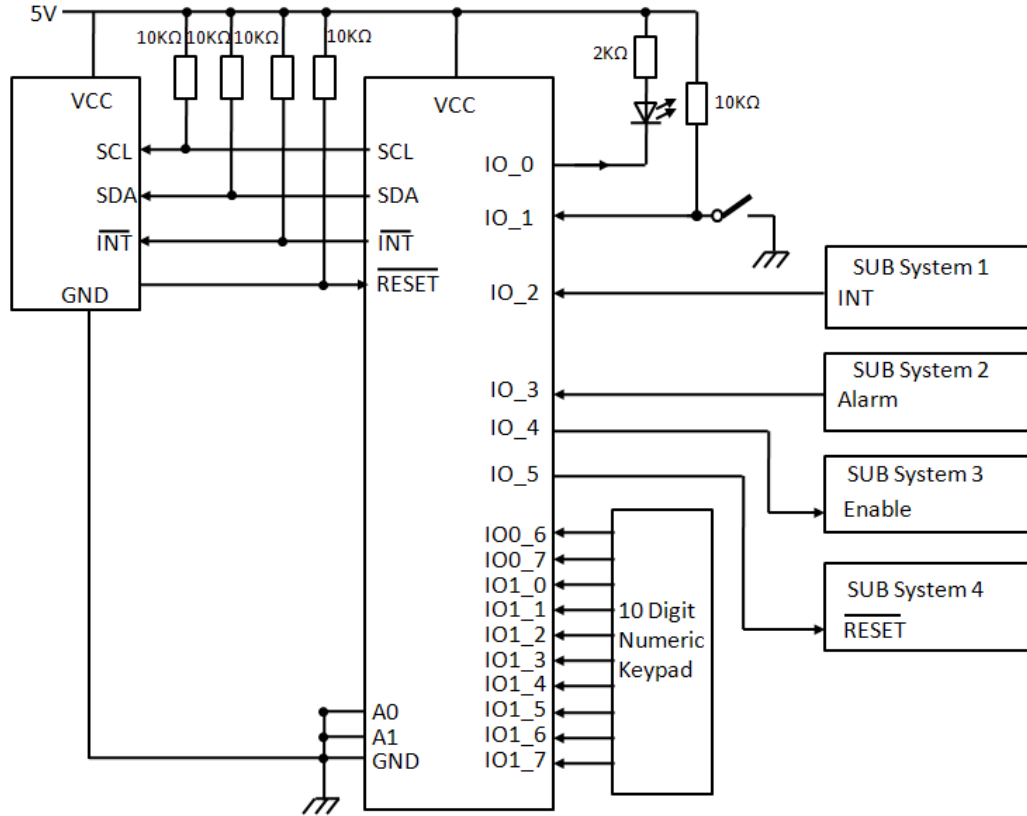
Note: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

The interrupt is deactivated when the input returns to its previous state or the Input Port register is read. A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Note: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

Application design-in information

Figure 10: Typical application



Device address configured as 1110 100xb for this example.
 IO0_0, IO0_4, IO0_5 configured as outputs.
 IO0_1, IO0_2, IO0_3 configured as inputs.
 IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

Minimizing ICC when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to VCC through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than VCC. The supply current, ICC, increases as V_I becomes lower than VCC.

Designs need minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to VCC when the LED is off. Figure 11 shows a high value resistor in parallel with the LED. Figure 12 shows VCC less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above VCC and prevent additional supply current consumption when the LED is off.

Figure 11: High value resistor in parallel with the LED

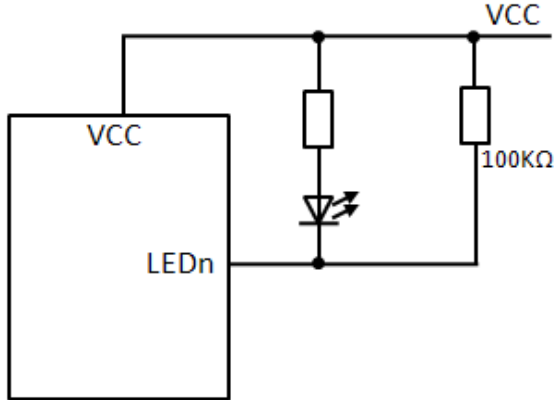
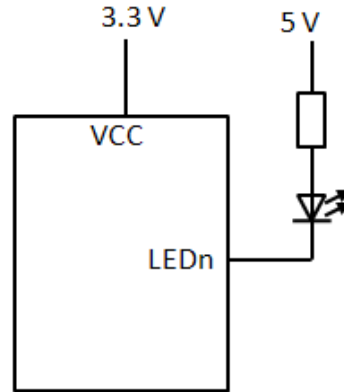
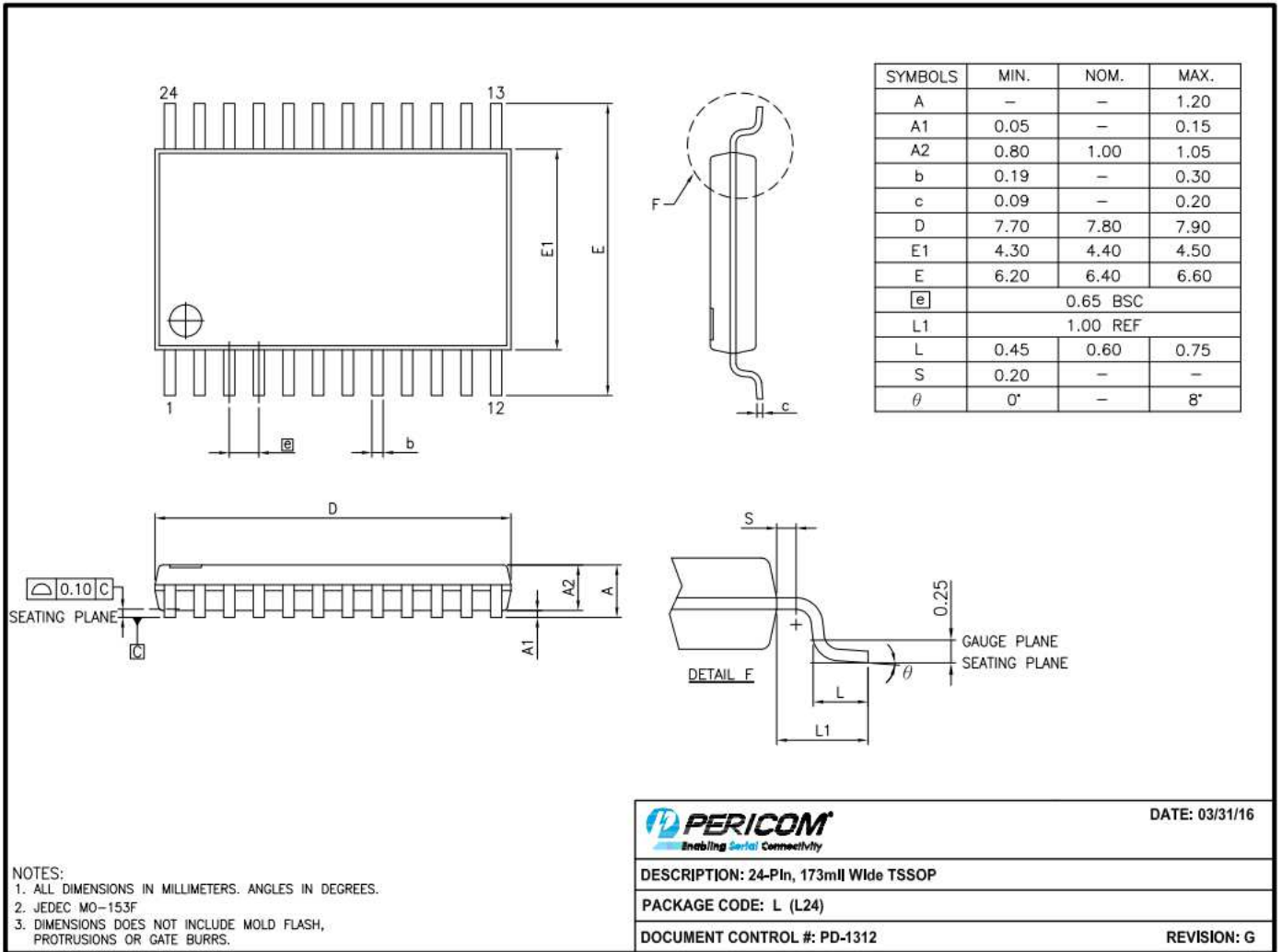


Figure 12: Device supplied by a lower voltage

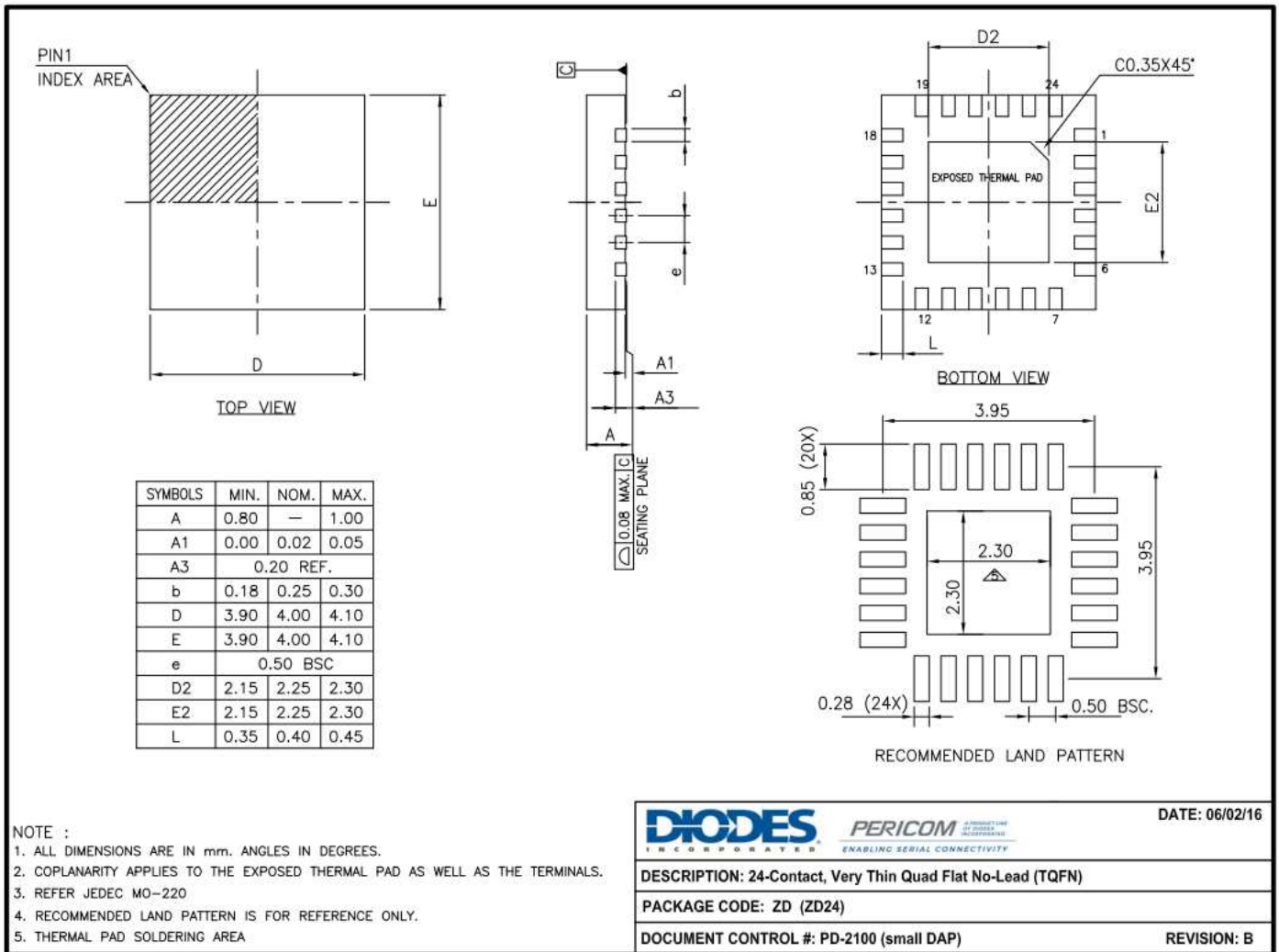


Mechanical Information

TSSOP-24(L)



TQFN 4x4-24(ZD)



Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Part Number	Package Code	Package
PI4IOE5V9539LE	L	24-pin, 173mil wide(TSSOP24)
PI4IOE5V9539LEX	L	24-pin, 173mil wide(TSSOP24), Tape & Reel
PI4IOE5V9539ZDE	ZD	24-Contact, Very Thin Quad Flat No-Lead (TQFN)
PI4IOE5V9539ZDEX	ZD	24-Contact, Very Thin Quad Flat No-Lead (TQFN), Tape & Reel

- Note:**
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
 - E = Pb-free and Green
 - Adding X Suffix= Tape/Reel