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## Features

- ➔ Operation power supply voltage from 2.3V to 5.5V
- ➔ 8-bit I<sup>2</sup>C-bus GPIO with interrupt and reset
- ➔ 5V tolerant I/Os
- ➔ Polarity inversion register
- ➔ Active LOW Reset Pin
- ➔ Low current consumption
- ➔ 0Hz to 400KHz clock frequency
- ➔ Noise filter on SCL/SDA inputs
- ➔ Power-on reset
- ➔ ESD protection (4KV HBM and 1KV CDM)
- ➔ Offered in three different packages:SOIC-16, TSSOP-16 and TQFN 4x4-16

## Description

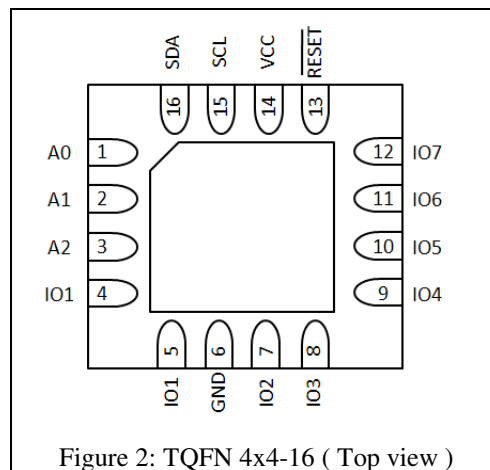
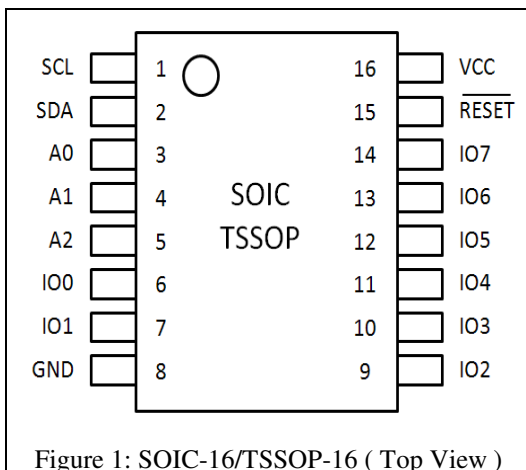
The PI4IOE5V9557 provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I<sup>2</sup>C-bus/SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9557 consists of an 8-bit register to configure the I/Os as either inputs or outputs, and an 8-bit polarity register to change the polarity of the input port register. The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

The power-on reset sets the registers to their default values and initializes the device state machine. The RESET pin causes the same reset/default I/O input configuration to occur without de-powering the device, holding the registers and I<sup>2</sup>C-bus state machine in their default state until the RESET input is once again HIGH.

Three hardware pins (A0, A1, A2) vary the fixed I<sup>2</sup>C-bus address and allow up to eight devices to share the same I<sup>2</sup>C-bus/SMBus.

## Pin Configuration



## Pin Description

Table 1: Pin Description

Pin		Name	Type	Description
SO16 TSSOP16	TQFN16			
1	15	SCL	I	Serial clock line
2	16	SCA	I	Serial data line
3	1	A0	I	Address input 0
4	2	A1	I	Address input 1
5	3	A2	I	Address input 2
6	4	IO0	I/O	input/output 0 (open-drain)
7	5	IO1	I/O	input/output 1
8	6	GND	G	Supply ground
9	7	IO2	I/O	input/output 2
10	8	IO3	I/O	input/output 3
11	9	IO4	I/O	input/output 4
12	10	IO5	G	input/output 5
13	11	IO6	I/O	input/output 6
14	12	IO7	I/O	input/output 7
15	13	$\overline{\text{RESET}}$	I	Active LOW reset input
16	14	VCC	P	Supply voltage

\* I = Input; O = Output; P = Power; G = Ground

## Maximum Ratings

Power supply.....	-0.5V to +6.0V
Voltage on an I/O pin.....	GND-0.5V to +6.0V
Input current.....	±20mA
Output current on an I/O pin.....	±50mA
Supply current.....	±160mA
Ground supply current.....	200mA
Total power dissipation.....	400mW
Operation temperature.....	-40~85°C
Storage temperature.....	-65~150°C
Maximum Junction temperature, T <sub>j(max)</sub> .....	125°C

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb = -40 °C to +85 °C; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Power supply</b>						
VCC	Supply voltage		2.3	-	5.5	V
I <sub>CC</sub>	Supply current	Operating mode; VCC = 5.5 V; no load; f <sub>SCL</sub> = 100 kHz	-	19	25	μA
I <sub>sb</sub>	Standby current	Standby mode; VCC = 5.5 V; no load; V <sub>I</sub> = GND; f <sub>SCL</sub> = 0 kHz; I/O = inputs	-	0.25	1	uA
		Standby mode; VCC = 5.5 V; no load; V <sub>I</sub> = VCC; f <sub>SCL</sub> = 0 kHz; I/O = inputs	-	0.25	1	μA
ΔI <sub>sb</sub>	Additional standby current	Standby mode; VCC = 5.5 V; every LED I/O at V <sub>I</sub> = 4.3V; f <sub>SCL</sub> = 0 kHz;	-	0.8	1	mA
V <sub>FOR</sub>	Power-on reset voltage <sup>[1]</sup>		-	1.16	1.41	V
<b>Input SCL, input/output SDA</b>						
V <sub>IL</sub>	Low level input voltage		-0.5	-	+0.3VCC	V
V <sub>IH</sub>	High level input voltage		0.7VCC	-	5.5	V
I <sub>OL</sub>	Low level output current	V <sub>OL</sub> = 0.4V; VCC = 2.3V	3	-	-	mA
I <sub>L</sub>	Leakage current	V <sub>I</sub> = VCC or GND	-1	-	1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = GND	-	6	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>I/Os</b>						
V <sub>IL</sub>	Low level input voltage		-0.5	-	+0.81	V
V <sub>IH</sub>	High level input voltage		+1.8	-	5.5	V
I <sub>OL</sub>	Low level output current	VCC =2.3 V; V <sub>OL</sub> = 0.5 V <sup>[2]</sup>	8	10	-	mA
I <sub>OH</sub>	High level output current	Except pin IO0; V <sub>OH</sub> =2.4V <sup>[3]</sup>	4	-	-	mA
		pin IO0; V <sub>OH</sub> =4.6V <sup>[3]</sup>	-	-	1	uA
		pin IO0; V <sub>OH</sub> =3.3V <sup>[3]</sup>	-	-	1	uA
I <sub>LI</sub>	Low level input leakage current	VCC=5.5V; V <sub>I</sub> =GND	-1	-	1	μA
C <sub>i</sub>	Input capacitance		-	3.7	10	pF
C <sub>o</sub>	Output capacitance		-	3.7	10	pF
<b>Select inputs A0,A1,A2 and <math>\overline{\text{RESET}}</math></b>						
V <sub>IL</sub>	Low level input voltage		-0.5	-	+0.81	V
V <sub>IH</sub>	High level input voltage		+1.8	-	5.5	V
I <sub>L</sub>	Input leakage current		-1		1	μA

Note:

[1]: VCC must be lowered to 0.2 V for at least 20us in order to reset part.

[2]: The total mount sunk by all I/Os must be limited to 100mA and 25 mA per bit.

[3]: The total current sourced by all I/Os must be limited to 85mA and 20mA to bit

## Dynamic Characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I <sup>2</sup> C		Fast mode I <sup>2</sup> C		Unit
			Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>VD;ACK</sub> <sup>[1]</sup>	data valid acknowledge time		-	3.45	-	0.9	μs
t <sub>HD;DAT</sub> <sup>[2]</sup>	data hold time		0	-	0	-	ns
t <sub>VD;DAT</sub>	data valid time		-	3.45	-	0.9	us
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	-	300	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	-	300	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
<b>Port timing</b>							
t <sub>v(Q)</sub>	Data output valid time <sup>[3]</sup>	Pin IO0	-	250	-	250	ns
		Pin IO1 to IO7	-	200	-	200	ns
t <sub>su(D)</sub>	Data input set-up time		0	-	0	-	ns
t <sub>h(D)</sub>	Data input hold time		200	-	200	-	ns
<b>Reset timing</b>							
t <sub>w(rst)</sub>	Reset pulse width		25	-	25	-	ns
t <sub>rec(rst)</sub>	Reset recovery time		0	-	0	-	ns
t <sub>rst</sub>	Reset time		1	-	1	-	us



Note:

- [1]:  $t_{VD:ACK}$  = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
- [2]:  $t_{VD:DAT}$  = minimum time for SDA data out to be valid following SCL LOW.
- [3]:  $t_{V(Q)}$  measured from 0.7VCC on SCL to 50% I/O output.

**PI4IOE5V9557 Block Diagram**

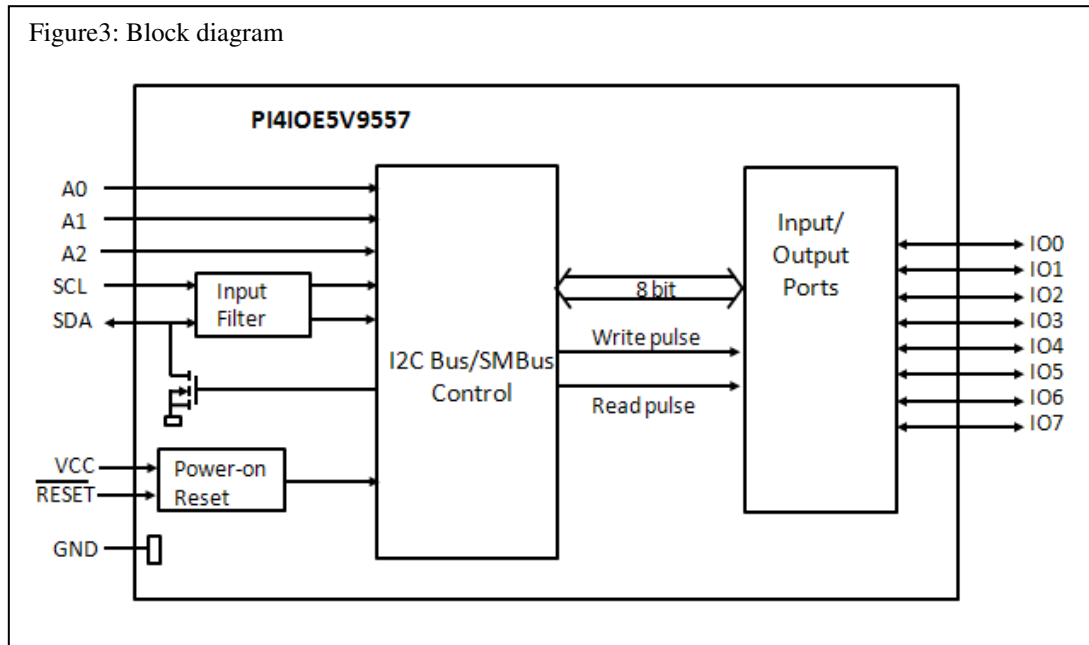


Figure 4: Simplified schematic of IO0

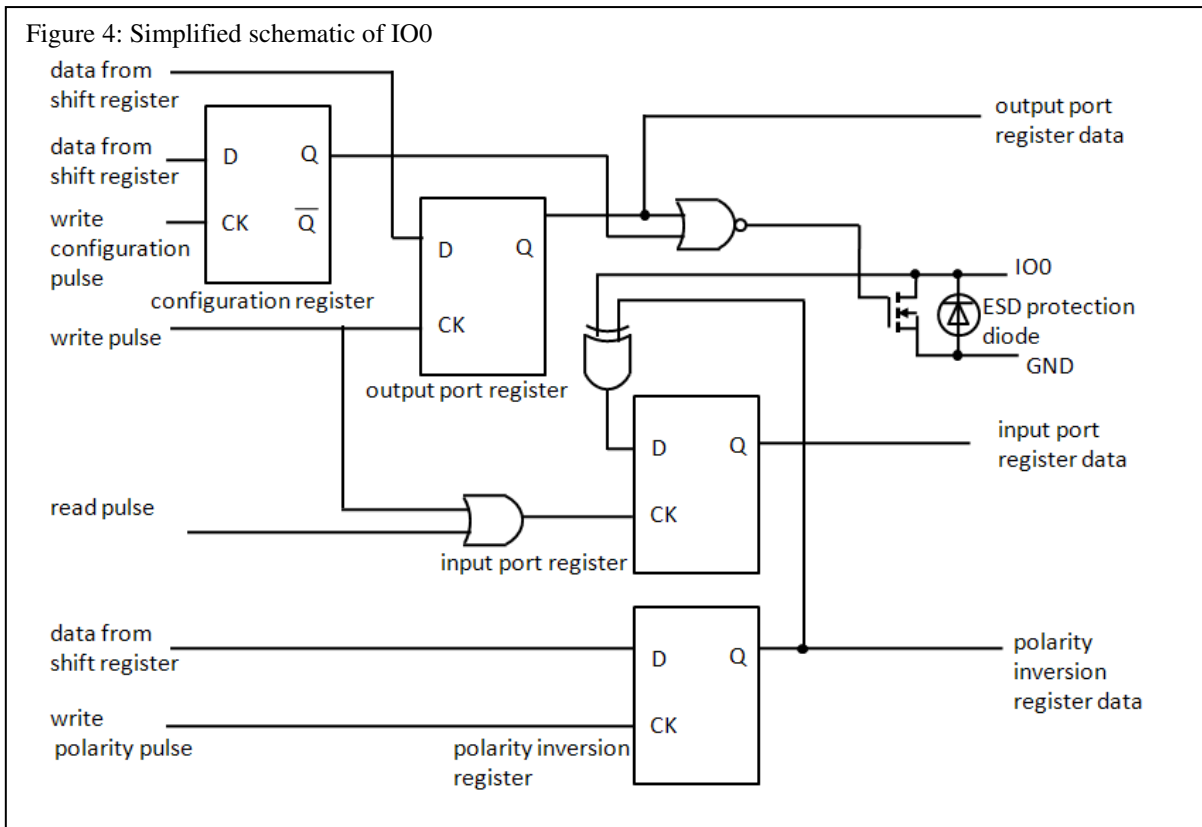
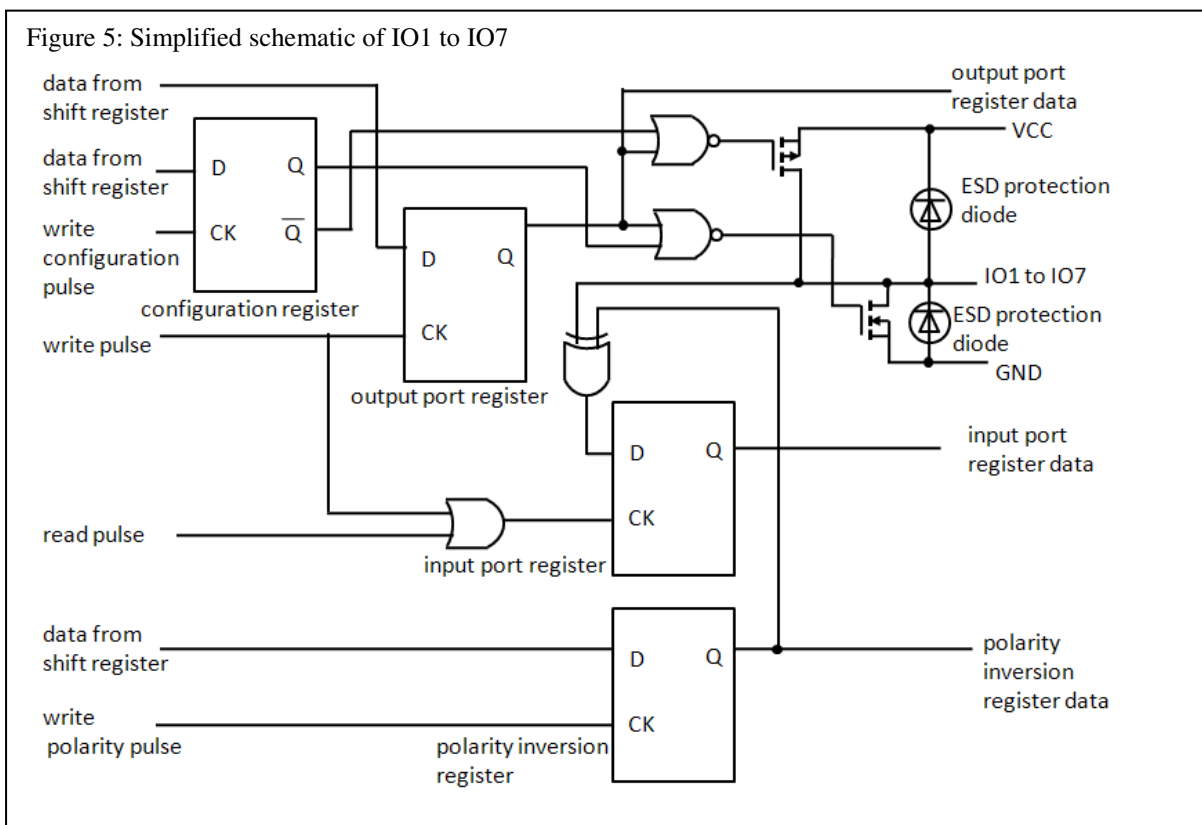


Figure 5: Simplified schematic of IO1 to IO7





## Details Description

### a. Device address

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PI4IOE5V9557 is shown in. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

Table 4: Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	0	1	1	A2	A1	A0	R/W

Note: Read “1”, Write “0”

### b. Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PI4IOE5V9557, which will be stored in the control register. This register can be written and read via the I<sup>2</sup>C-bus.

Table 5: Control register

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	0	0	0	0	0	D1	D0

Table 6: D0 and D1 definition

D1	D0	Name	Access	Description
0	0	Register 0	Read-only	Input port register
0	1	Register 1	Read/write	Output port register
1	0	Register 2	Read/write	Polarity inversion register
1	1	Register 3	Read/write	Configuration register

### c. Register description

#### i. Register 0: Input port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. Writes to this register have no effect.

Table 7: Input port register

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0

**ii. Register 1: Output port register**

This register reflects the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 8: Output port register

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	0	0	0	0	0	0	0	0

**iii. Register 2: Polarity inversion register**

This register enables polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with logic 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with logic 0), the corresponding port pin's original polarity is retained.

Table 9: Polarity inversion register

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	1	1	1	1	0	0	0	0

**iv. Register 3: Configuration register**

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output.

Table 10: Configuration register

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

**d. Power-on reset**

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4IOE5V9557 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V9557 registers and I<sup>2</sup>C-bus/SMBus state machine will initialize to their default states. Thereafter, VCC must be lowered below 0.2 V to reset the device.

**e.  $\overline{\text{RESET}}$  input**

A reset can be accomplished by holding the RESET pin LOW for a minimum of  $t_{w(\text{rst})}$ . The PI4IOE5V9557 registers and SMBus/I<sup>2</sup>C-bus state machine will be held in their default state until the RESET input is once again HIGH. This input requires a pull-up resistor to VCC if no active connection is used.

**i. Bus transactions**

Data is transmitted to the PI4IOE5V9557 registers using Write Byte transfers. Data is read from the PI4IOE5V9557 registers using Read and Receive Byte transfers.

Figure 6: Write to output registers

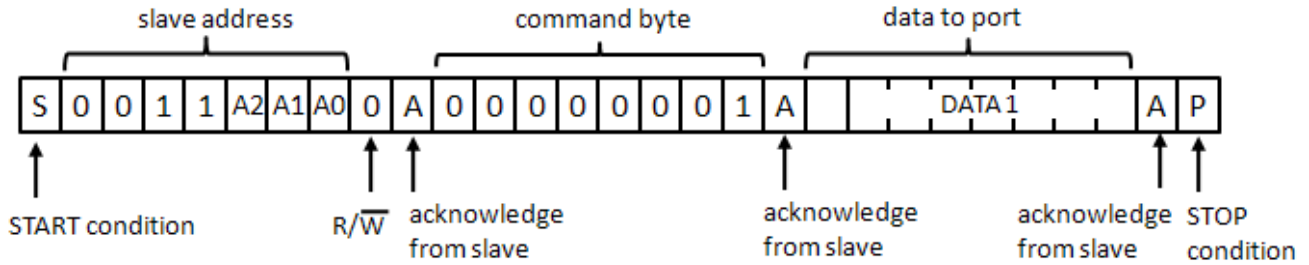


Figure 7: Write to I/O configuration or polarity inversion registers

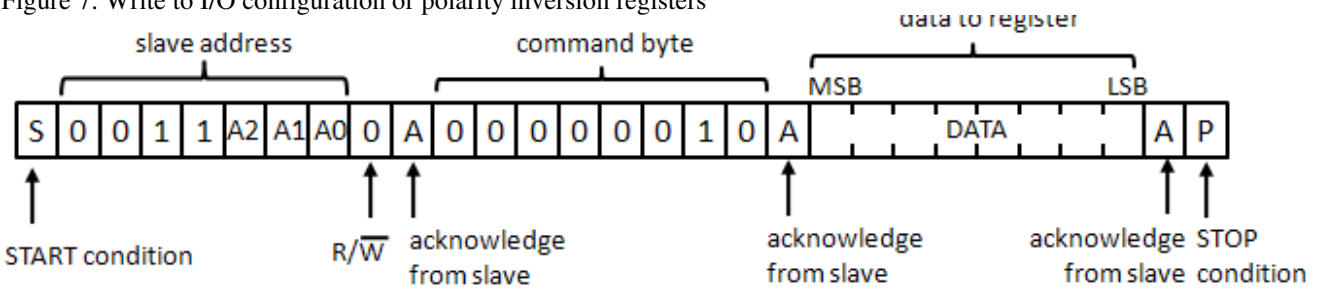


Figure 8: Read from register

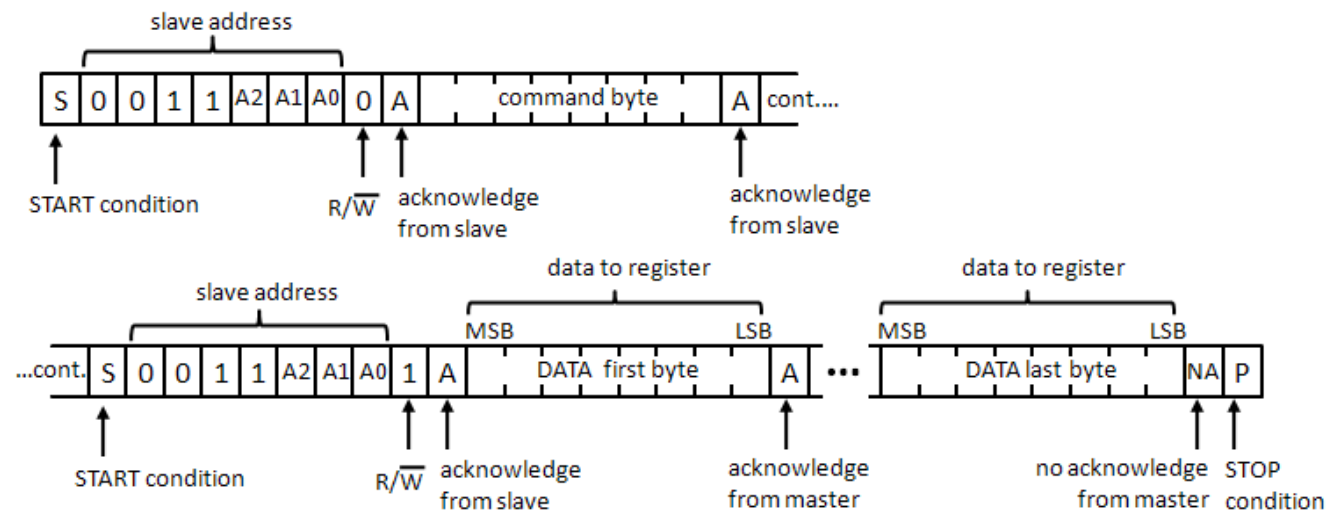
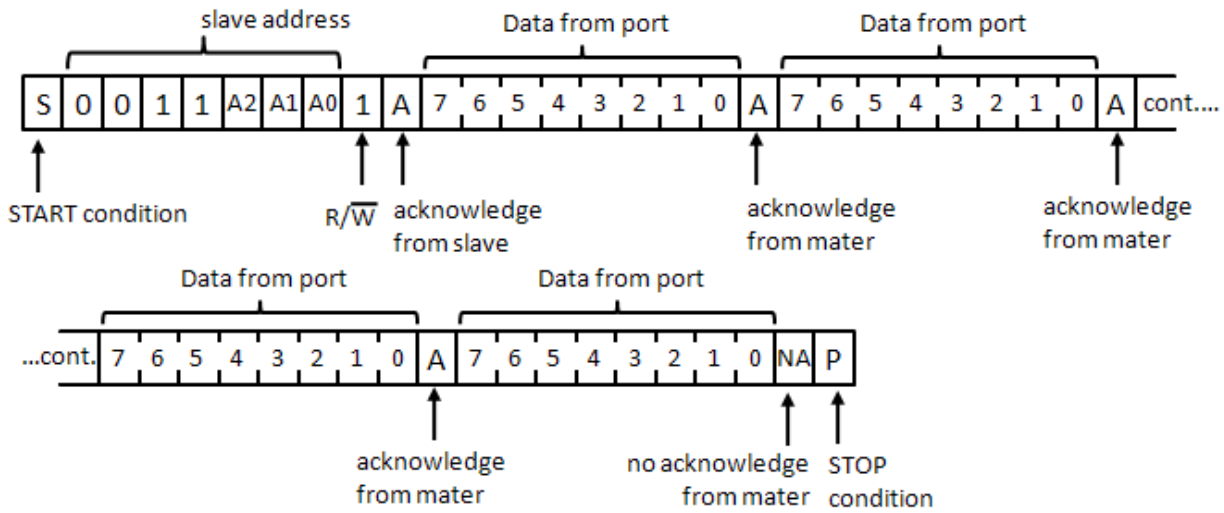


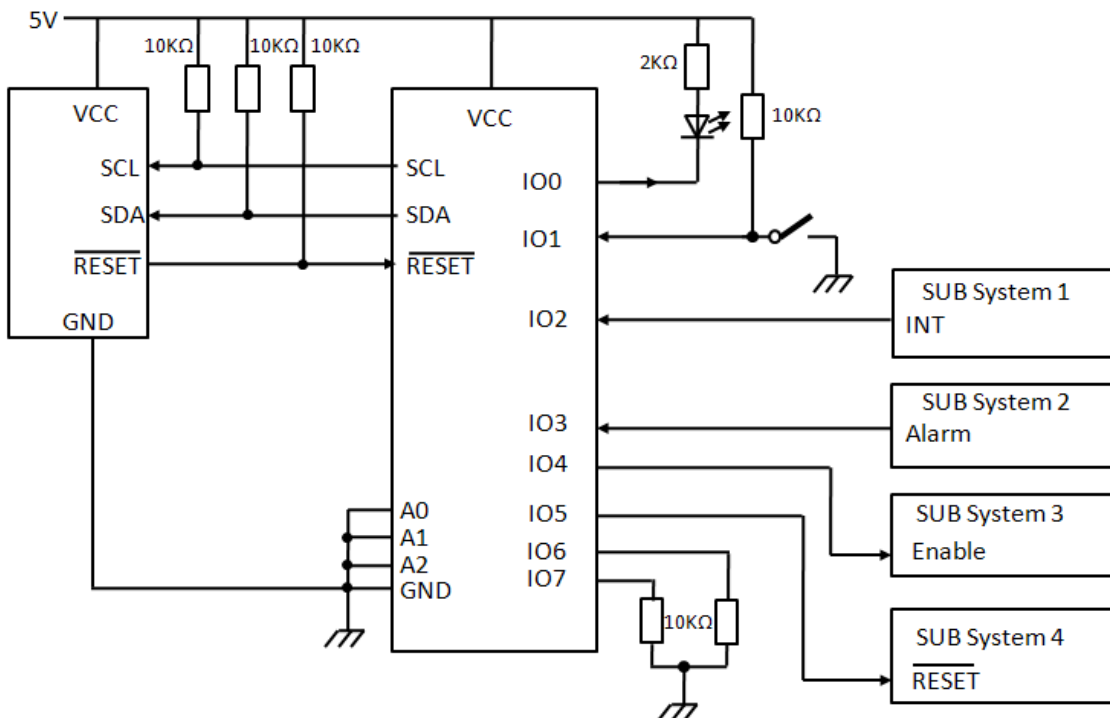
Figure 9: Read input port register



Note: This figure assumes the command byte has previously been programmed with 00h. Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

**Application design-in information**

Figure 10: Typical application

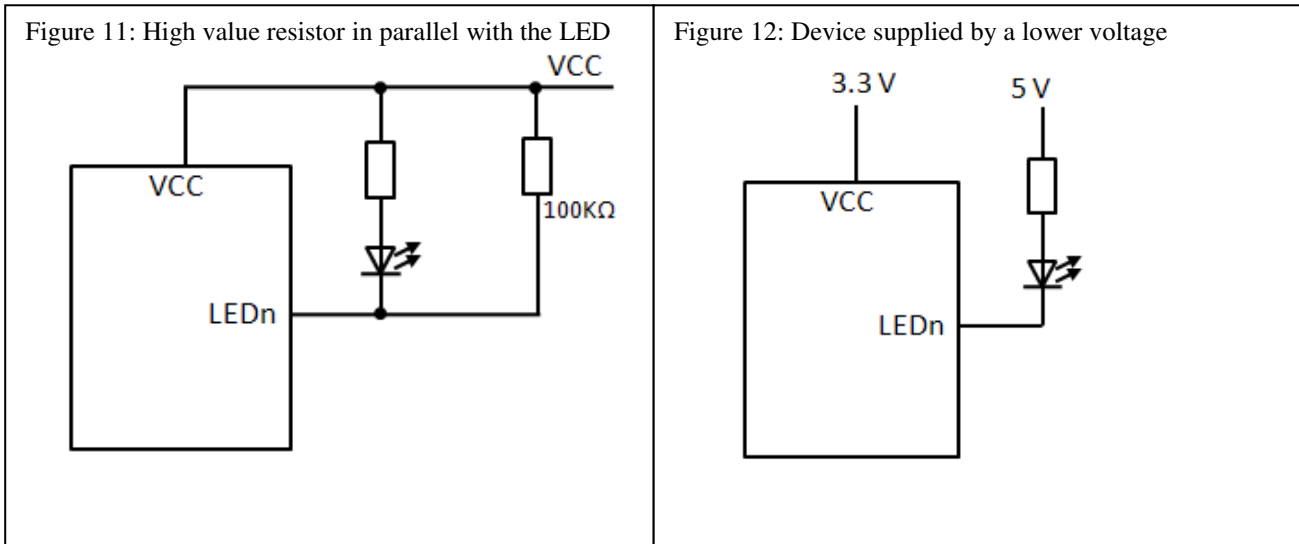


Device address configured as 0011100x for this example.  
 IO0, IO4, IO5 configured as outputs.  
 IO1, IO2, IO3 configured as inputs.  
 IO6, IO7 are not used.

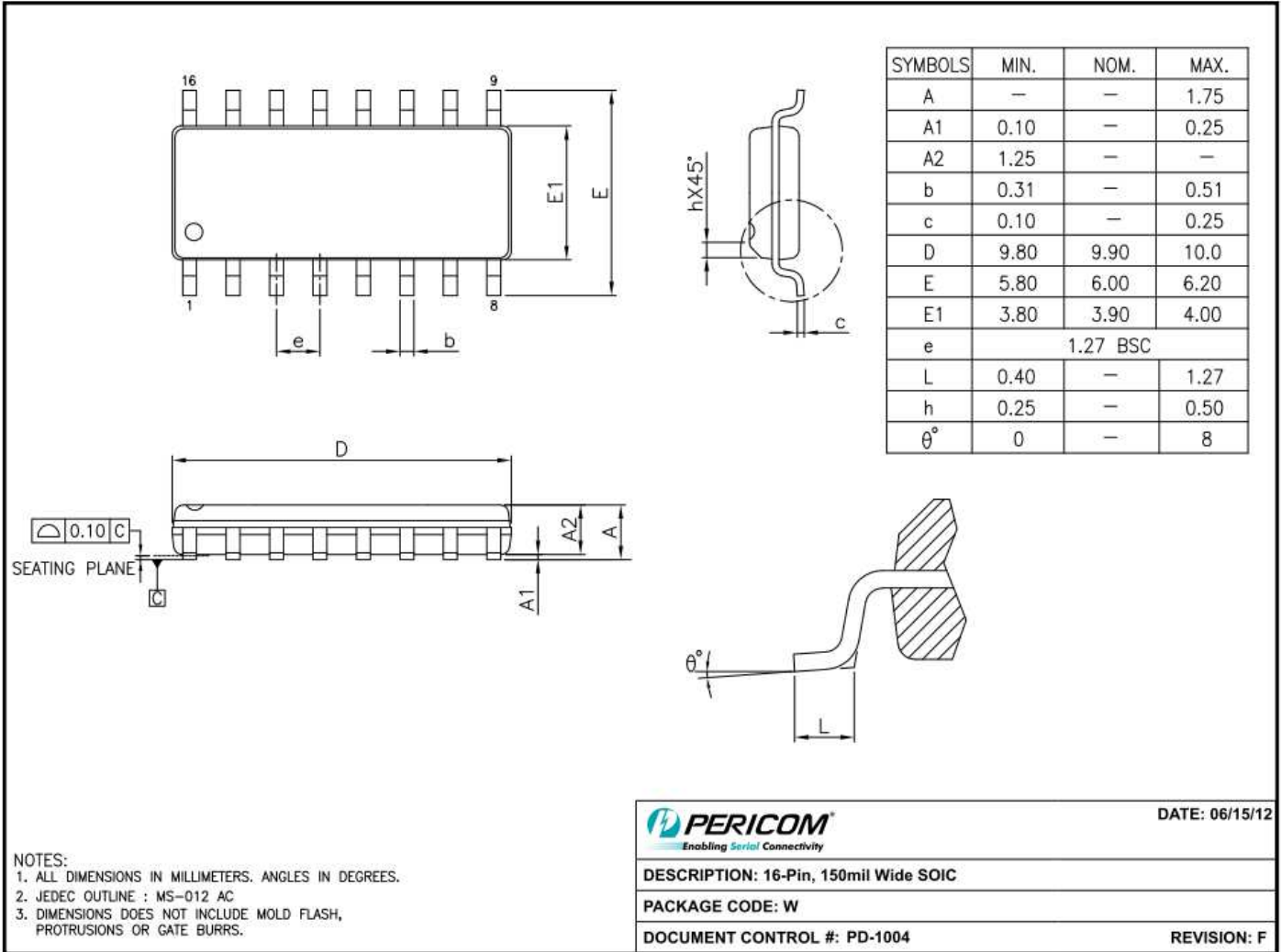
**Minimizing ICC when the I/Os are used to control LEDs**

When the I/Os are used to control LEDs, they are normally connected to VCC through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than VCC. The supply current, ICC, increases as V<sub>I</sub> becomes lower than VCC.

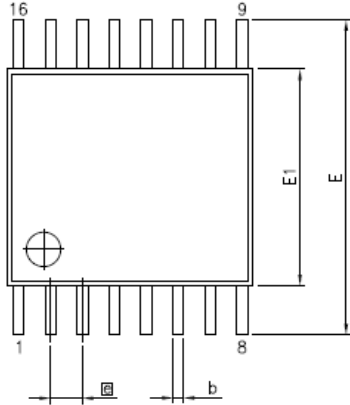
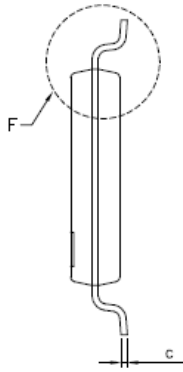
Designs need minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to VCC when the LED is off. Figure 11 shows a high value resistor in parallel with the LED. Figure 12 shows VCC less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above VCC and prevent additional supply current consumption when the LED is off.



**Mechanical Information**  
**SOIC-16(W)**

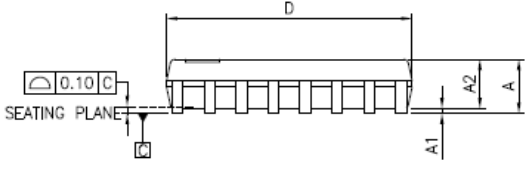


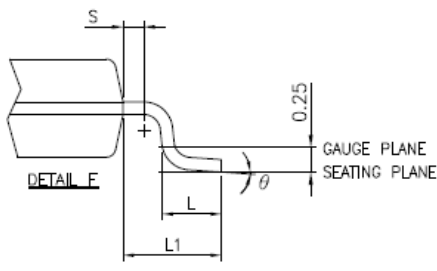
TSSOP-16(L)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
$\theta$	0°	–	8°





**Notes:**

1. Refer JEDEC MO-153F/AB
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

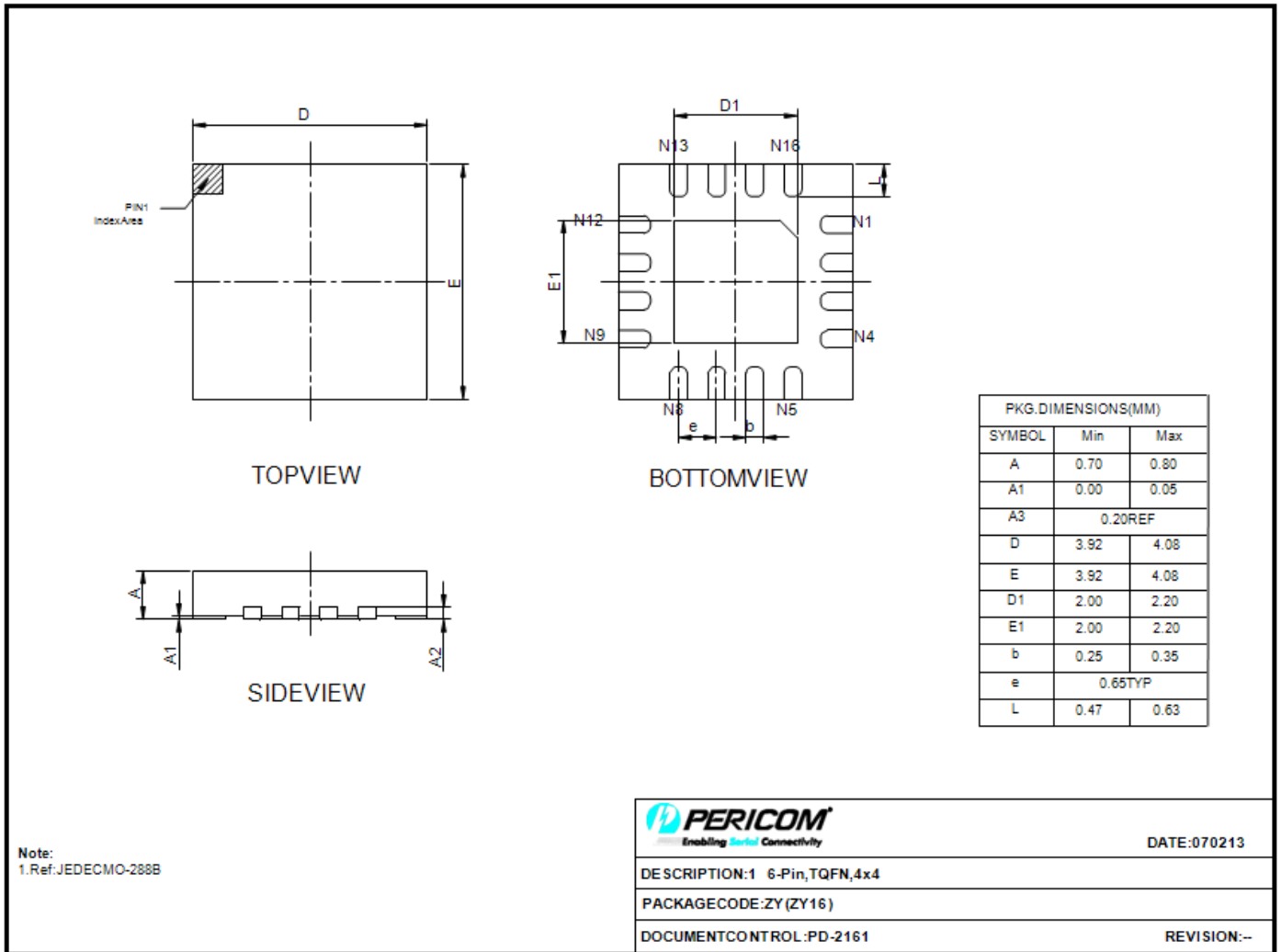


DATE: 05/03/12

DESCRIPTION: 16-Pin, 173mil Wide TSSOP
PACKAGE CODE: L
DOCUMENT CONTROL #: PD-1310
REVISION: F



TQFN 4x4-16(ZY)



## Ordering Information

Part No.	Package Code	Package
PI4IOE5V9557WE	W	16-Pin,150 mil Wide SOIC
PI4IOE5V9557WEX	W	16-Pin,150 mil Wide SOIC,Tape & Reel
PI4IOE5V9557LE	L	Lead free and Green 16-pin TSSOP16(173mil wide)
PI4IOE5V9557LEX	L	Lead free and Green 16-pin TSSOP16(173mil wide) Tape &Reel
PI4IOE5V9557ZYEX	ZY	Lead free and Green 16-pin TQFN4.0x4.0, Tape & Reel

**Note:**

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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