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A product Line of
Diodes Incorporated

PI5A100

Precision, Wide-Bandwidth Quad SPDT Analog Switch

Features

- Single Supply Operation (+2V to +6V)
- Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance (6Ω typ with 5V supply) Minimizes Distortion and Error Voltages
- On-Resistance Matching Between Channels, 0.4Ω Typ.
- On-Resistance Flatness, <2Ω Typ.
- Low Charge Injection Reduces Glitch Errors, Q = 6pC Typ.
- Replaces Mechanical Relays
- High Speed. t_{ON}, 8ns Typ.
- Low Crosstalk: -100dB @ 10 MHz
- Low Off-Isolation: -57dB @ 10 MHz
- Wide -3dB Bandwidth: 230 MHz
- High-Current Channel Capability: >100mA
- TTL/CMOS Logic Compatible
- Low Power Consumption (0.5µW typ.)
- Packaging (Pb-free & Green Available):
  -16-pin SOIC (W)
  -16-pin QSOP (Q)

Applications

- Audio, Video Switching and Routing
- LAN Switches
- Telecommunication Systems
- Battery-Powered Systems

Truth Table

$\overline{EN}$	IN	ON Switch
0	0	NC_1, NC_2, NC_3, NC_4
0	1	NO_1, NO_2, NO_3, NO_4
1	X	None. Disabled

Description

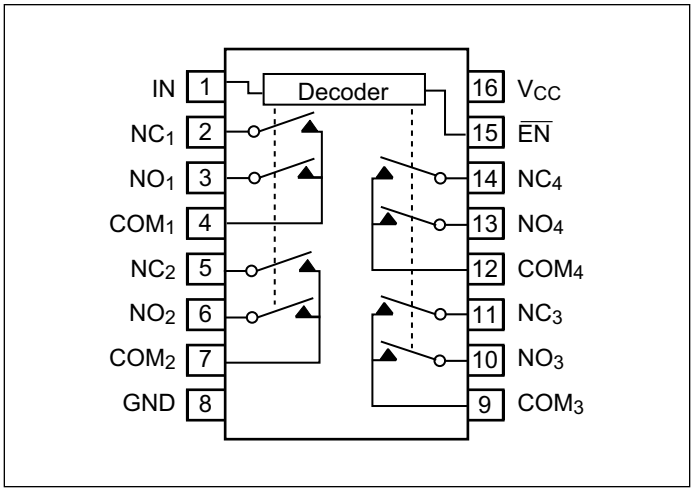
The PI5A100 is an improved Quad Single-pole double-throw (4SPDT) CMOS analog switch designed to operate with a single +2V to +6V power supply. The $\overline{EN}$ pin may be used to place all switches in a high-impedance state. This high precision device is ideal for low-distortion audio, video, and data switching and routing.

Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

The PI5A100 is fully specified with +5V, and +3.3V supplies. With +5V, it guarantees less than 10Ω On-Resistance. On-Resistance matching between channels is within 2Ω. On-Resistance flatness is less than 4Ω over the specified range. The PI5A100 guarantees fast switching speeds (t_{ON} < 12ns).

The PI5A100 is available in the narrow-body SOIC and QSOP packages for operation over the industrial (-40°C to +85°C) temperature range.

Block Diagram/Pin Configuration



Notes:
1. Switches shown for logic "0" input.
2. NC = Normally Closed; NO = Normally Open

Absolute Maximum Ratings

Voltages Referenced to Gnd
V_{CC} ..... -0.5V to +7V
V_{IN}, V_{COM}, V_{NC}, V_{NO} (1) ..... -0.5V to V_{CC} +2V
..... or 30mA, whichever occurs first
Current (any terminal except COM, NO, NC)..... 30mA
Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle)..... 120mA

Thermal Information

Continuous Power Dissipation
Narrow SOIC & QSOP
(derate 8.7mW/ºC above +70ºC) 650mW
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (soldering, 10s) . . . . . +300°C

Notes:

1. Signals on NC, NO, COM, or IN exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.
2. Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this speci fication is not implied.

Electrical Specifications - Single +5V Supply (V_{CC} = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Symbol	Parameter	TestConditions	Temp.	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
V_{ANALOG}	Analog Switch Range(1)		Full	0		V_{CC}	V
R_{ON}	On-Resistance	V_{CC} = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		8	10	Ω
			Full			12	
ΔR_{ON}	On-Resistance Match Between Channels(6)		25		0.8	2	
			Full			4	
$R_{FLAT(ON)}$	On-Resistance Flatness(5)	V_{CC} = 5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		2	3	
			Full			4	
$I_{NO(OFF)}$ or $I_{NC(OFF)}$	NO or NC OFF Leakage(6)	V_{CC} = 5.5C, I_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25		0.07		
			Full	-80		80	nA
$I_{COM(OFF)}$	COM OFF Leakage Current(6)	V_{CC} = 5.5V, I_{COM} = 4.5V, V_{NO} or V_{NC} = ± 4.5V	25		0.01		
			Full	-80		80	
$I_{COM(ON)}$	COM ON Leakage Current(6)	V_{CC} = 5.5V, I_{COM} = 4.5V, V_{NO} or V_{NC} = ± 4.5V	25		0.016		
			Full	-80		80	

Electrical Specifications - Single +5V Supply (V_{CC} = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V) CONTINUED

Symbol	Parameter	TestConditions	Temp.	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
V_{IH}	Input High Voltage	Guaranteed logic High Level	Full	2			V
V_{IL}	Input Low Voltage	Guaranteed logic Low Level				0.8	
I_{INH}	Input Current with Input Voltage High	V_{IN} = 2.4V, all others = 0.8V	Full	-1	0.005	1	µA
I_{INL}	Input Current with Input Voltage Low	V_{IN} = 0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
t_{ON}	Turn-On Time	V_{CC} = 5V, See Figure 1	25		8	15	ns
			Full			20	
t_{OFF}	Turn-Off Time		25		3.5	7	
			Full			10	
Q	Charge Injection(3)	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, See Figure 2	25			10	pC
O_{IRR}	Off Isolations	R_L = 50Ω, C_L = 5pF, f = 10MHz, See Figure 3			-57		dB
X_{TALK}	Crosstalk(8)	R_L = 50Ω, C_L = 5pF, f = 10MHz, See Figure 4			-100		
$C_{(OFF)}$	NC or NO Capacitance	f=1kHz, See Figure 5			8		pF
$C_{COM(OFF)}$	COM OFF Capacitance				14		
$C_{COM(ON)}$	COM ON Capacitance	f = 1kHz, See Figure 6			18		
BW	-3db Bandwidth	R_L = 50Ω See Figure 7	Full		230		MHz
D	Distortion	R_L = 10kΩ			0.2		%
Supply							
V_{CC}	Power-Supply		Full	2		6	V
I_{CC}	Postitive Supply Current	V_{CC} = 5.5V, V_{IN} = 0V or V_{CC}, all channels on or off				1	µA

Notes:

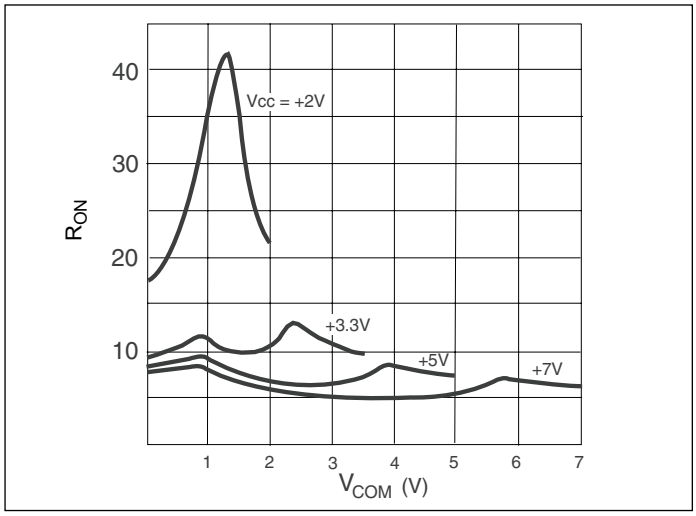
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See figure 3.
8. Between any two switches. See figure 4.-

Electrical Specifications - Single +3.3V Supply (V_{CC} = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

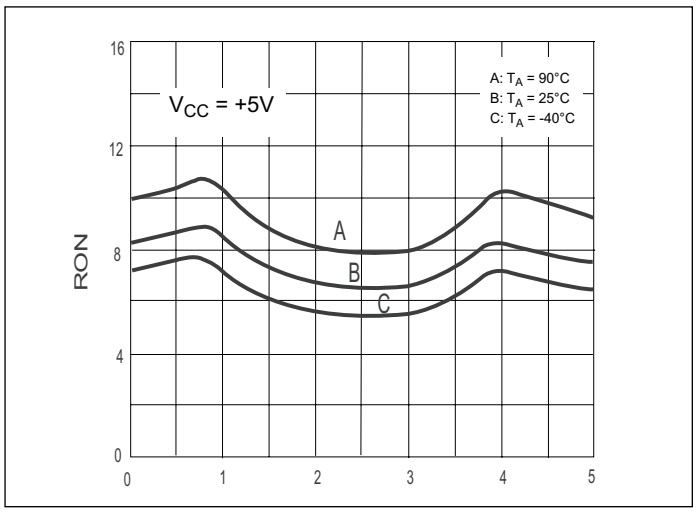
Symbol	Parameter	TestConditions	Temp.	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
	Analog Switch Range(1)			0		V_{CC}	V
R_{ON}	On-Resistance	V_{CC} = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		12	18	Ω
			Full				
ΔR_{ON}	On-Resistance Match Between Channels(6)		25		5		
			Full				
$R_{FLAT(ON)}$	On-Resistance Flatness(5)	V_{CC} = 5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		2	4	
			Full			5	
Dynamic							
t_{ON}	Turn-On Time	V_{CC} = 5V, See Figure 1	25		14	25	ns
			Full			40	
t_{OFF}	Turn-Off Time		25		4.5	12	
			Full			20	
Q	Charge Injection(3)	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, See Figure 2	25		5	10	pC
Supply							
I_{CC}	Postitive Supply Current	V_{CC} = 3.6V, V_{IN} = 0V or V_{CC}, all channels on or off	Full			1	µA

Typical Operating Characteristics (T_A=+25ºC, unless otherwise noted)

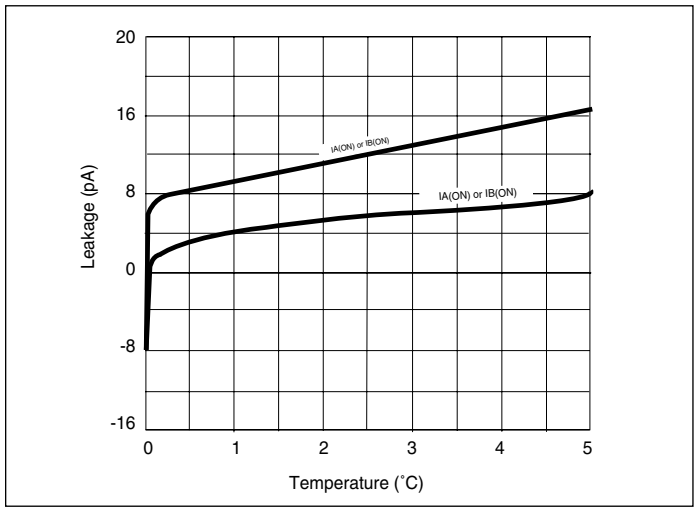
R_{ON} vs. V_{COM}



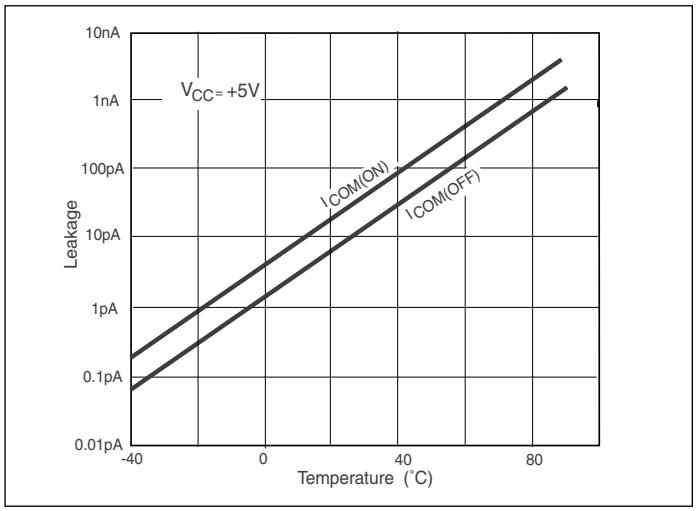
R_{ON} vs. V_{COM} and Temperature



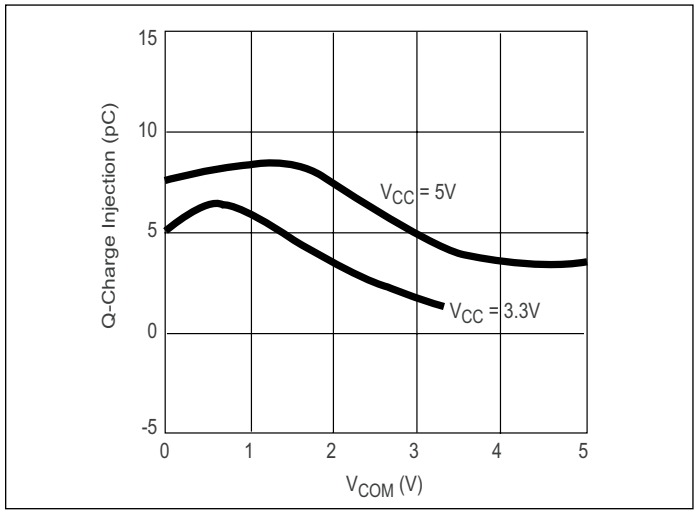
Leakage Currents vs. Analog Voltage



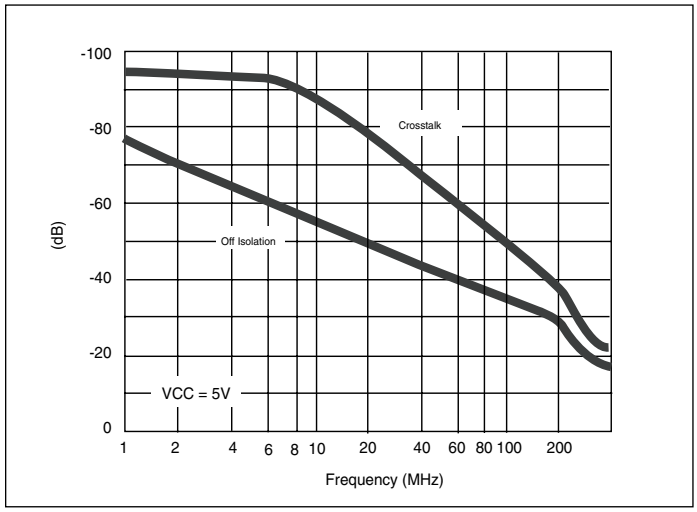
Leakage Current vs. Temperature



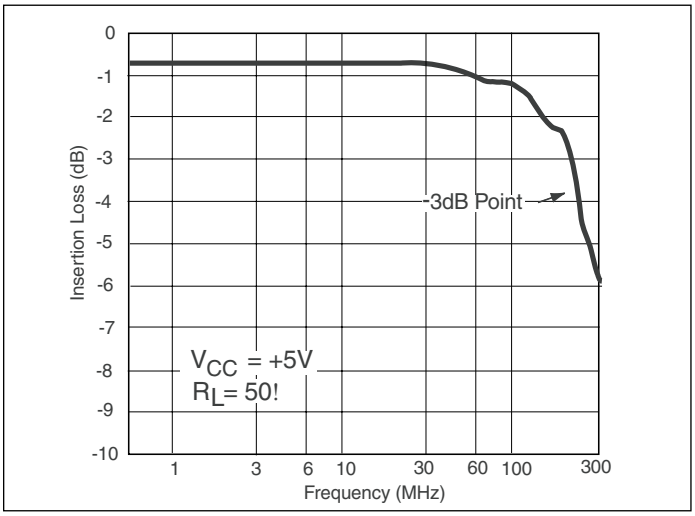
Charge Injection vs. Analog Voltage



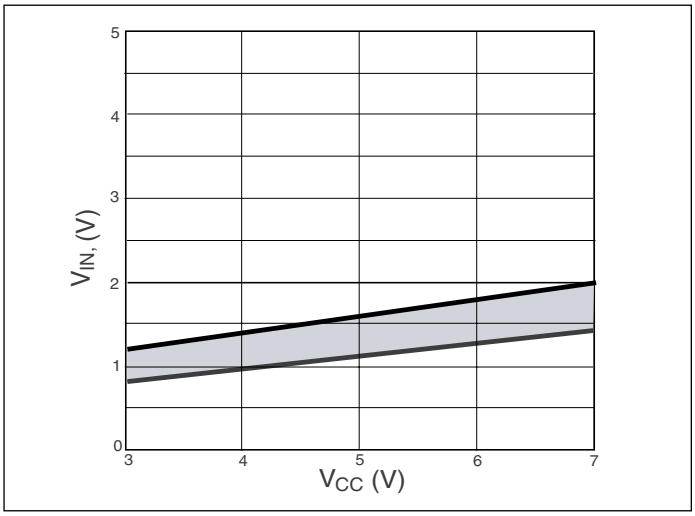
Crosstalk and Off-Isolation vs. Frequency



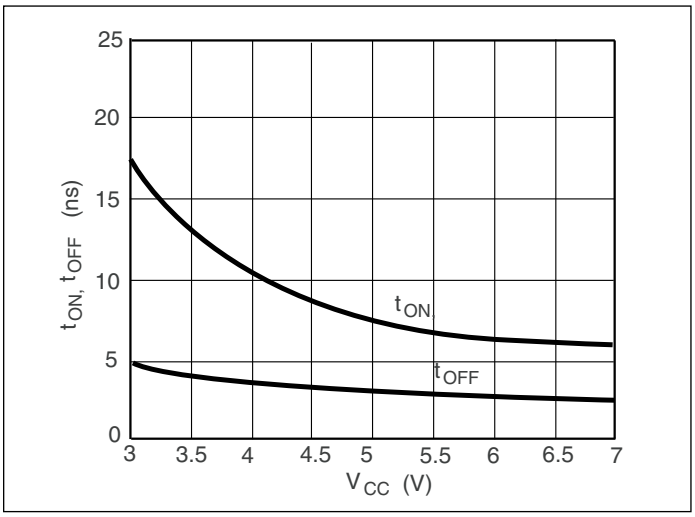
Insertion Loss vs. Frequency



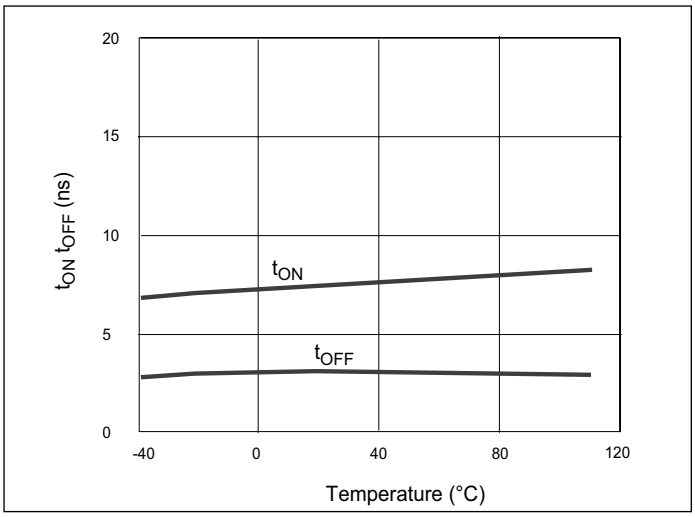
Input Switching Threshold vs. Supply Voltage



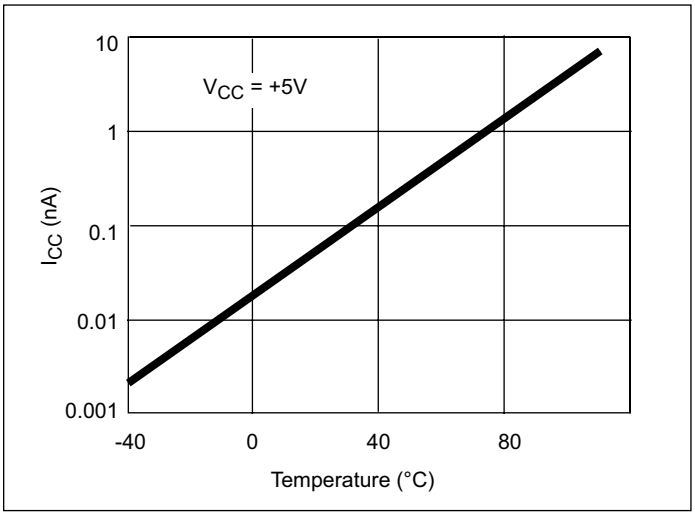
RON vs. VCOM and Single Supply



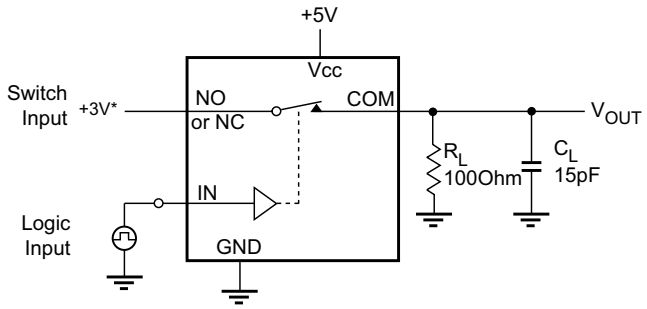
Switching Times vs. Temperature



Supply Current vs. Temperature

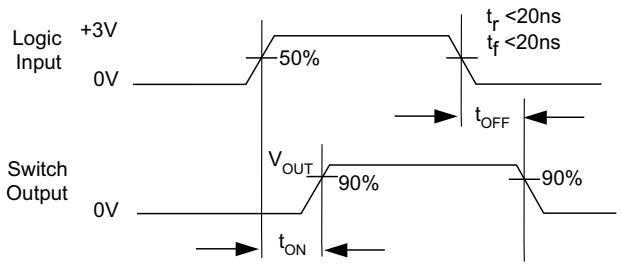


Test Circuits/Timing Diagrams



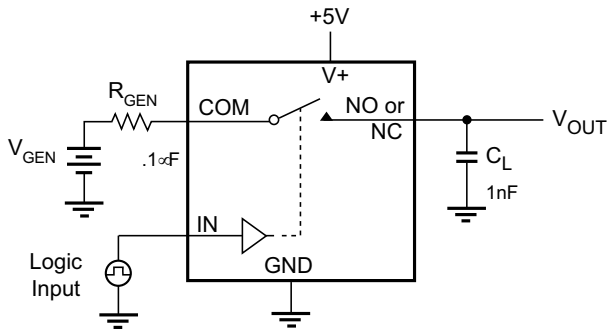
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

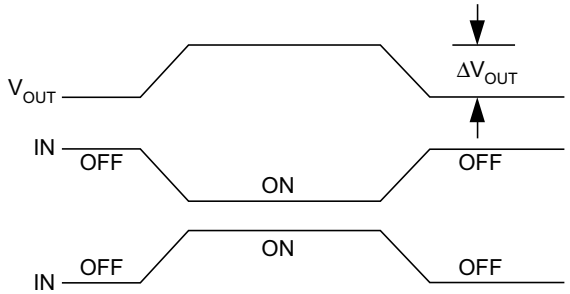
$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time





$$Q = (\Delta V_{OUT})(C_L)$$

Figure 2. Charge Injection

Test Circuits/Timing Diagrams (cont.)

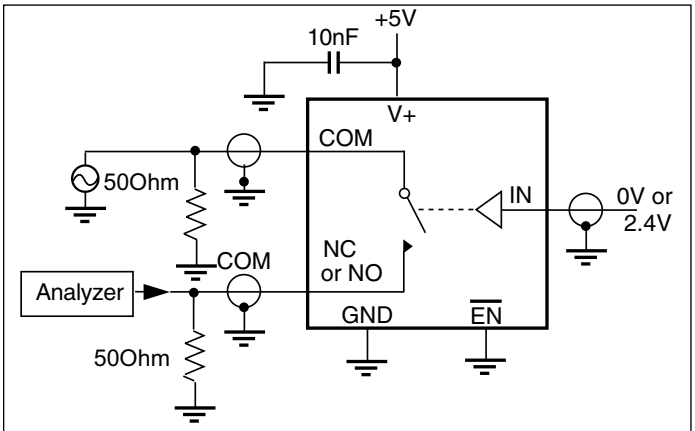


Figure 3. Off Isolation

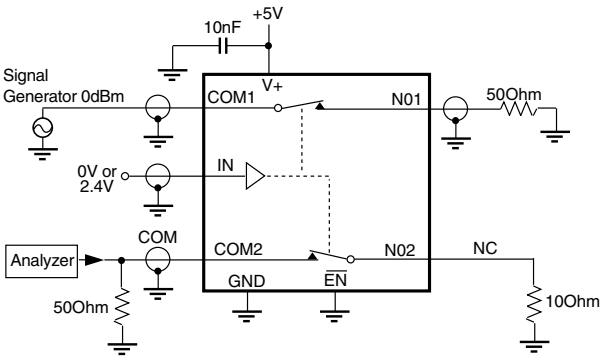


Figure 4. Crosstalk

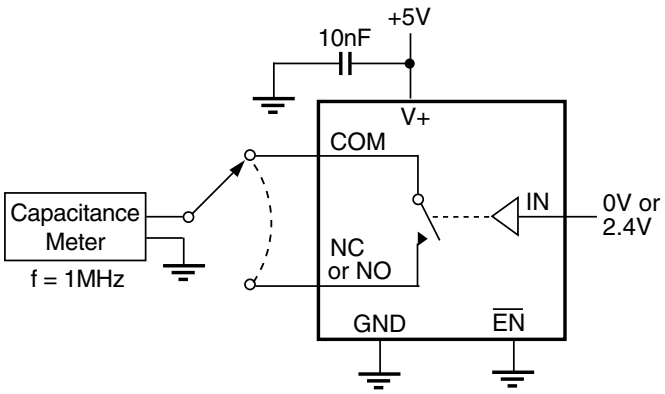


Figure 5. Channel-Off Capacitance

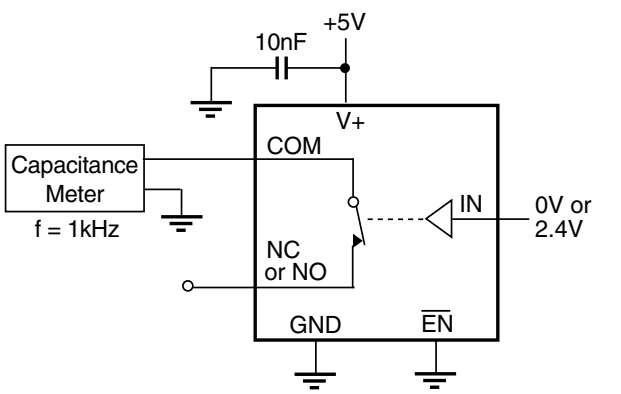


Figure 6. Channel-On Capacitance

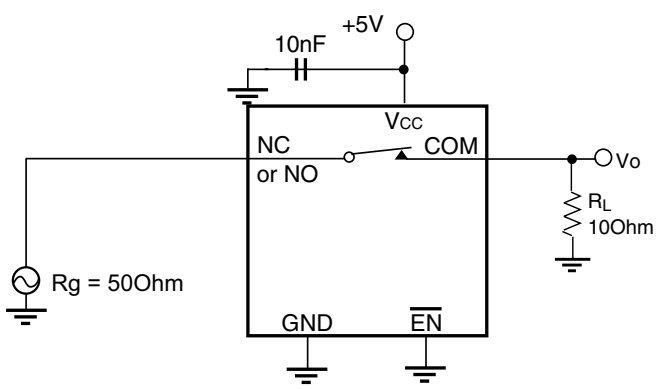


Figure 7. Bandwidth

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 8). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

RGB Switch

Figure 9 illustrates a simple low cost RGB switch. The RGB -to-Composite Decoder produces either NTSC or S-VHS video from an RGB source. Asingle PI5A100 selects one of the two video sources to produce either SVHS, Composite or RGB video outputs. The low insertion loss of the PI5A100 eliminates the need for expensive input/output buffers.

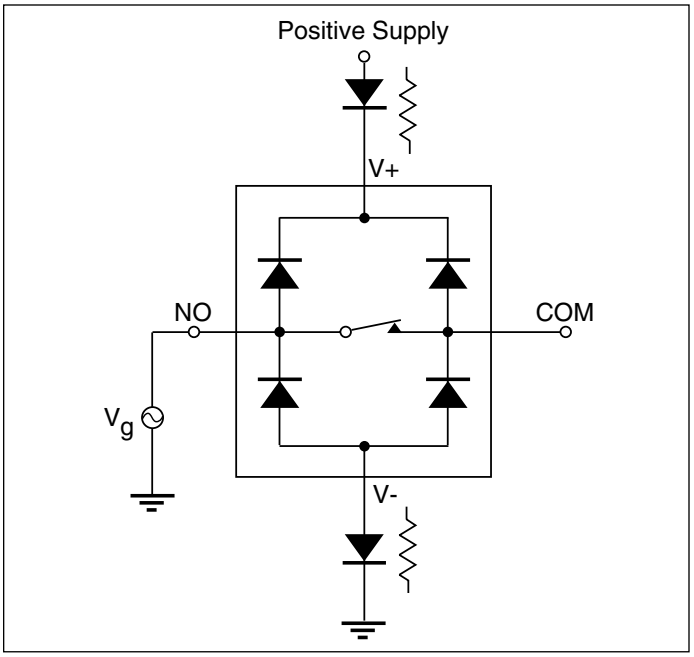


Figure 8: Overvoltage protection is accomplished using two external blocking diodes or two current limiting resistors.

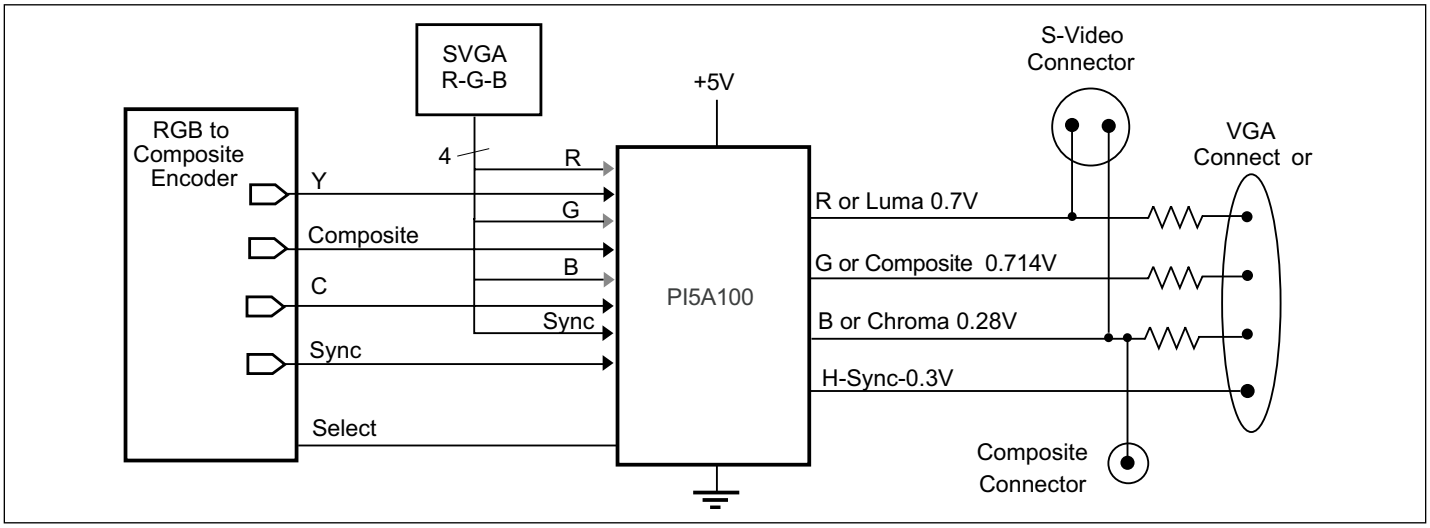


Figure 9: The single PI5A100 is used to select SVHS, VGA or Composite video outputs.

Applications

Audio Muting Function

Figure 8 shows the PI5A100 in an audio card muting application. The original problem was one of excessive popping/clicking noise appearing when connecting disconnecting external loads, and at power on/off. The PI5A100 performs a muting function by grounding the outputs at power on/off and during the transition time. The 32Ω headset impedance demands a very low and very flat switch-on resistance to reduce THD and signal loss.

Paralleling two sections of the PI5A100 produces a Ron of 2.5Ω *with an unsurpassed* ±0.5Ω flatness.

To handle AC signals it was necessary to power the device with ±3V provided by two Zener diodes: Z1 and Z2. The select and Enable control signals are shifted by using twpo 2.5V Zener diodes Z3,Z4 and pull down resistors connected to -3V.

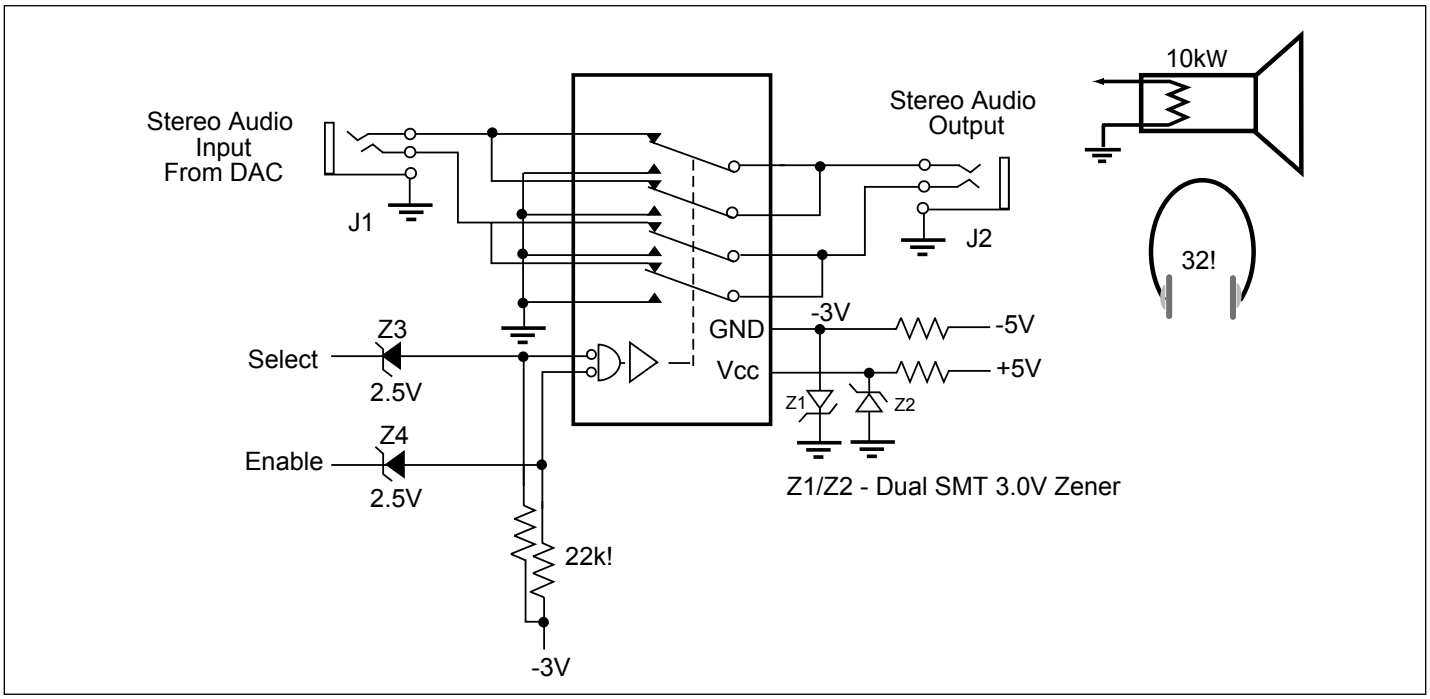


Figure 10: The PI5A100 momentarily mutes the stereo outputs by connecting them to ground during transition times.

Part Marking

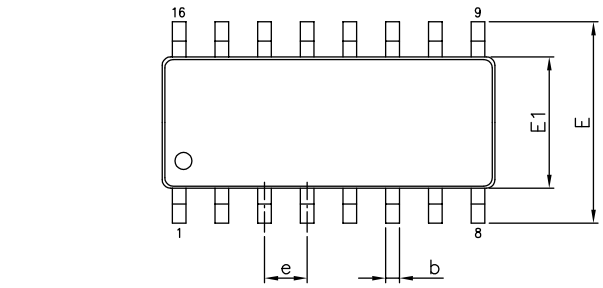
W Package

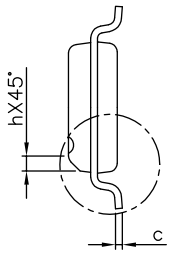
*: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above fab code means Cu wire

Q Package

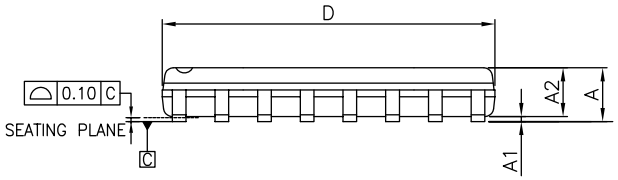
Z: Die Rev
YW: Year & Workweek
1st X: Assembly Code
2nd X: Fab Code

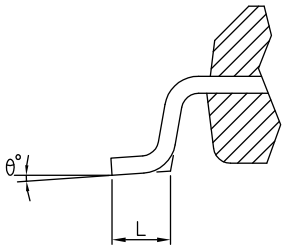
Packaging Mechanical: 16-SOIC (W)





SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.00	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	9.80	9.90	10.0
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	—	1.27
h	0.15	—	0.50
θ°	0	—	8





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC OUTLINE : MS-012 AC
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MIN. DIMENSION OF A2 AND h ARE OUT OF JEDEC SPEC.

DIODES INCORPORATED PERICOM ENABLING SERIAL CONNECTIVITY

DATE: 06/30/16

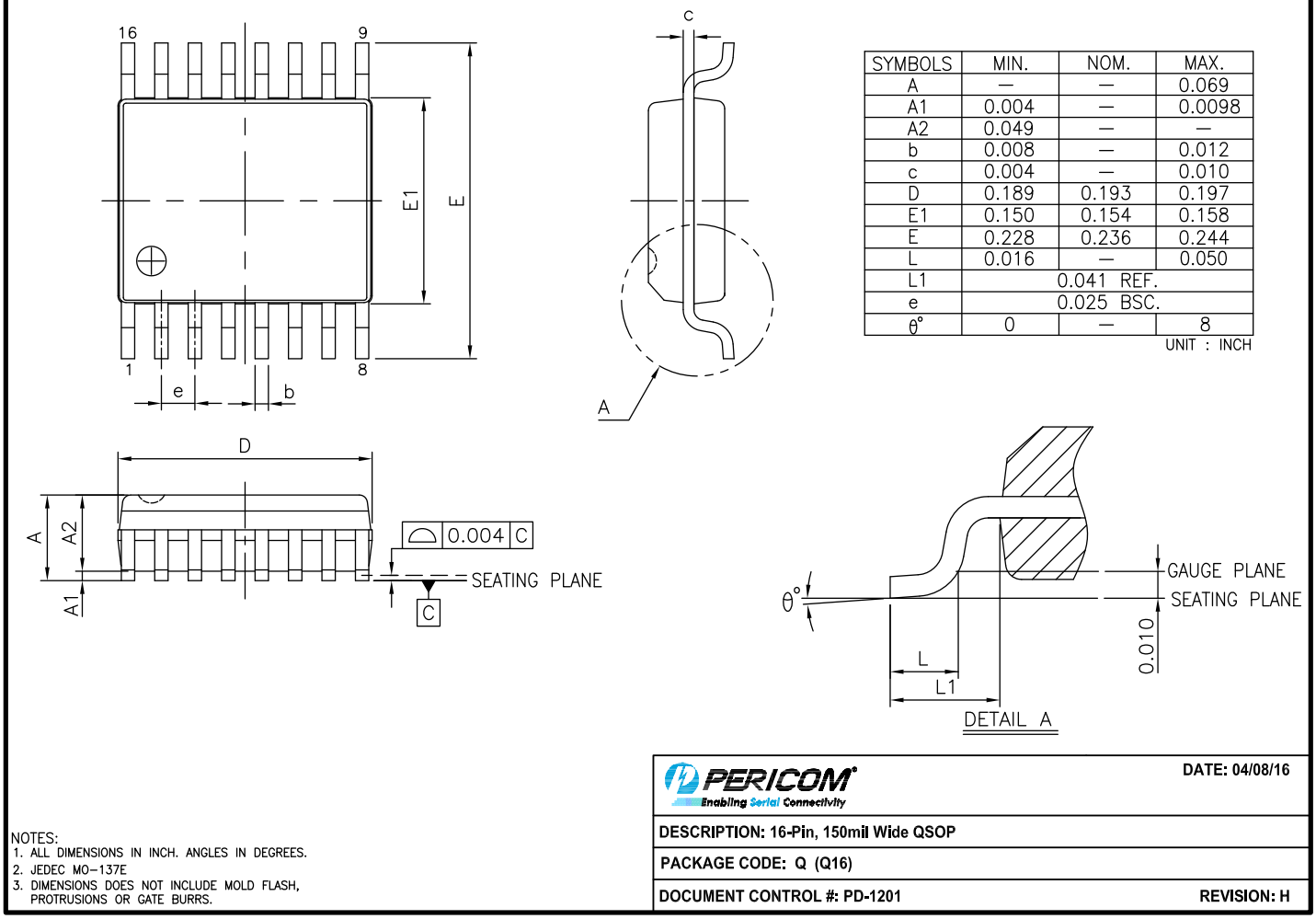
DESCRIPTION: 16-Pin, 150mil Wide SOIC

PACKAGE CODE: W

DOCUMENT CONTROL #: PD-1004 REVISION: G

16-0145

Packaging Mechanical: 16-QSOP (Q)



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	0.069
A1	0.004	—	0.0098
A2	0.049	—	—
b	0.008	—	0.012
c	0.004	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.158
E	0.228	0.236	0.244
L	0.016	—	0.050
L1		0.041 REF.	
e		0.025 BSC.	
θ°	0	—	8

UNIT : INCH

NOTES:
1. ALL DIMENSIONS IN INCH. ANGLES IN DEGREES.
2. JEDEC MO–137E
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 04/08/16

DESCRIPTION: 16-Pin, 150mil Wide QSOP

PACKAGE CODE: Q (Q16)

DOCUMENT CONTROL #: PD-1201 REVISION: H

16-0056

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI5A100WEX	W	16-pin, 150mil Wide (SOIC)
PI5A100QEX	Q	16-pin, 150mil Wide (QSOP)

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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