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## Features

- Single-Supply Operation (+2V to +6 V )
- Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance ( $6 \Omega$ typ. with 5 V supply) Minimizes Distortion and Error Voltages
- On-Resistance Flatness, $3 \Omega$ typ.
- Low Charge Injection Reduces Glitch Errors. $Q=4 p C$ typ.
- High Speed. $\mathrm{t}_{\mathrm{ON}}=10 \mathrm{~ns}$ typ.
- Wide -3dB Bandwidth: 326 MHz (typ.)
- High-Current Channel Capability: $>100 \mathrm{~mA}$
- TTL/CMOS Logic Compatible
- Low Power Consumption ( $0.5 \mu \mathrm{~W}$ typ)
- Small outline transistor package minimizes board area
- Packaging ( Pb -free \& Green available):
- 5-pin 65-mil wide SOT23 (T) for PI5A121 and PI5A122
- 6-pin 65-mil wide SOT23 (T) for PI5A124
- 5-pin 50-mil wide SC70 (C) for PI5A121/PI5A122


## Applications

- Audio, Video Switching, and Routing
- Battery-Powered Communication Systems
- Computer Peripherals
- Telecommunications
- Portable Instrumentation
- Mechanical Relay Replacement
- Cell Phones
- PDAs


## Description

The PI5A121/PI5A122/PI5A124 are analog switches designed for single-supply operation. These high-precision devices are ideal for low-distortion audio, video, signal switching and routing.
The PI5A121 is a single-pole throw (SPST) normally open (NO) switch. The switch is open when IN is LOW. The PI5A122 is a single-pole single-throw (SPST) normally closed (NC) switch.
Each switch conducts current equally well in either direction when on. When off, they block voltages up to V + .

These switches are fully specified with +5 V , and +3.3 V supplies. With +5 V , they guarantee $<10 \Omega$ On-Resistance. On-Resistance matching between channels is within $2 \Omega$. On-Resistance flatness is less than $55 \Omega$ over the specified range. These switches also guarantee fast switching speeds ( $\mathrm{t}_{\mathrm{ON}}<20 \mathrm{~ns}$ ).
These products are available in 5-pin SC70 and/or 6-pin SOT23 plastic packages for operation over the industrial $\left(-40^{\circ} \mathrm{C}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ temperature range.

## Functional Diagrams, Pin Configurations and Truth Tables



Switches shown for Logic "0" input

| IN | PI5A121 | PI5A122 |
| :---: | :---: | :---: |
| 0 | OFF | ON |
| 1 | ON | OFF |


|  | PI5A124 |  |
| :---: | :---: | :---: |
| LOGIC | NC | NO |
| 0 | ON | OFF |
| 1 | OFF | ON |

Absolute Maximum Ratings
Voltages Referenced to Gnd V+ $\qquad$ -0.5 V to +7 V
$\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\mathrm{COM}}, \mathrm{V}_{\mathrm{NC}}, \mathrm{V}_{\mathrm{NO}}$ (Note 1 ) $\qquad$ -0.5 V to $\mathrm{V}_{\mathrm{CC}}+2 \mathrm{~V}$
or 30 mA , whichever occurs first
Current (any terminal) $\qquad$ $\pm 25 \mathrm{~mA}$
Peak Current, COM, NO, NC
(Pulsed at $1 \mathrm{~ms}, 10 \%$ duty cycle) $\qquad$ $\pm 25 \mathrm{~mA}$

## Thermal Information

Continuous Power Dissipation
SOT23-6 (derate $7 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+70^{\circ} \mathrm{C}$ )
550 mW
Storage Temperature $\qquad$ $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Lead Temperature (soldering, 10s) $\qquad$ $+300^{\circ} \mathrm{C}$

Note 1 :
Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30 mA .

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

## Electrical Specifications - Single +5 V Supply

$\left(\mathrm{V}+=+5 \mathrm{~V} \pm 10 \%, G N D=0 \mathrm{~V}, \mathrm{~V}_{\text {INH }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {INL }}=0.8 \mathrm{~V}\right)$

| Parameter | Symbol | Conditions | Temp. $\left({ }^{\circ} \mathrm{C}\right)$ | Min. ${ }^{(1)}$ | Typ. ${ }^{(2)}$ | Max. ${ }^{(1)}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Analog Switch |  |  |  |  |  |  |  |
| Analog Signal Range ${ }^{(3)}$ | Vanalog |  | Full | 0 |  | V+ | V |
| On-Resistance | $\mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=4.5 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{COM}}=-30 \mathrm{~mA}, \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=+2.5 \mathrm{~V} \end{aligned}$ | 25 |  | 7.2 | 10 | $\Omega$ |
|  |  |  | Full |  |  | 12 |  |
| On-Resistance Match Between Channels ${ }^{(4)}$ | $\Delta \mathrm{R}_{\mathrm{ON}}$ |  | 25 |  | 0.2 | 2 |  |
|  |  |  | Full |  |  | 4 |  |
| On-Resistance Flatness ${ }^{(5)}$ | $\mathrm{R}_{\text {FLAT(ON) }}$ | $\begin{aligned} & \mathrm{V}+=5 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{COM}}=-30 \mathrm{~mA}, \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=1 \mathrm{~V}, 2.5 \mathrm{~V}, 4 \mathrm{~V} \end{aligned}$ | 25 |  | 2.72 | 3.5 |  |
|  |  |  | Full |  |  | 4 |  |
| NO or NC Off Leakage Current ${ }^{(6)}$ | $\mathrm{I}_{\mathrm{NO}(\mathrm{OFF})}$ or $\mathrm{I}_{\mathrm{NC}(\mathrm{OFF})}$ | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{COM}}=0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=4.5 \mathrm{~V} \\ & \hline \end{aligned}$ | 25 |  | 0.18 |  | nA |
|  |  |  | Full | -80 |  | 80 |  |
| COM Off Leakage Current ${ }^{(6)}$ | $\mathrm{I}_{\text {COM }}(\mathrm{OFF})$ | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}}=+4.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}= \pm 0 \mathrm{~V} \end{aligned}$ | 25 |  | 0.20 |  |  |
|  |  |  | Full | -80 |  | 80 |  |
| COM On Leakage Current ${ }^{(6)}$ | $\mathrm{I}_{\text {COM }}(\mathrm{ON})$ | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{COM}}=+4.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=+4.5 \mathrm{~V} \end{aligned}$ | 25 |  | 0.20 |  |  |
|  |  |  | Full | -80 |  | 80 |  |

Electrical Specifications - Single +5V Supply (continued)
$\left(\mathrm{V}+=+5 \mathrm{~V} \pm 10 \%, \mathrm{GND}=0 \mathrm{~V}, \mathrm{~V}_{\text {INH }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {INL }}=0.8 \mathrm{~V}\right)$

| Parameter | Symbol | Conditions | Temp $\left({ }^{\circ} \mathrm{C}\right)$ | Min. ${ }^{(1)}$ | Typ. ${ }^{(2)}$ | Max. ${ }^{(1)}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Logic Input |  |  |  |  |  |  |  |
| Input High Voltage | $\mathrm{V}_{\mathrm{IH}}$ | Guaranteed logic High Level | Full | 2 |  |  | V |
| Input Low Voltage | $\mathrm{V}_{\text {IL }}$ | Guaranteed logic Low Level |  |  |  | 0.8 |  |
| Input Current with Voltage High | $\mathrm{I}_{\text {INH }}$ | $\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}$, all others $=0.8 \mathrm{~V}$ |  | -1 | 0.005 | 1 | $\mu \mathrm{A}$ |
| Input Current with Voltage Low | $\mathrm{I}_{\text {INL }}$ | $\mathrm{V}_{\mathrm{IN}}=0.8 \mathrm{~V}$, all others $=2.4 \mathrm{~V}$ |  | -1 | 0.005 | 1 |  |

## Dynamic

| Turn-On Time | ton | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$, Figure 1 | 25 | 7 | 15 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Full |  | 20 |  |
| Turn-Off Time | toFF |  | 25 | 1 | 7 |  |
|  |  |  | Full |  | 10 |  |
| Charge Injection ${ }^{(3)}$ | Q | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=1 \mathrm{nF}, \mathrm{~V}_{\mathrm{GEN}}=0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{GEN}}=0 \Omega, \text { Figure } 2 \end{aligned}$ | 25 | 1.6 | 10 | pC |
| Off Isolation | $\mathrm{O}_{\text {IRR }}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & \mathrm{f}=10 \mathrm{MHz}, \text { Figure } 3 \end{aligned}$ |  | -43 |  | dB |
| Crosstalk ${ }^{(8)}$ | $\mathrm{X}_{\text {TALK }}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & \mathrm{f}=10 \mathrm{MHz}, \text { Figure } 4 \end{aligned}$ |  | -43 |  |  |
| NC or NO Capacitance | $\mathrm{C}_{\text {(OFF) }}$ | $\mathrm{f}=1 \mathrm{kHz}$, Figure 5 |  | 5.5 |  | pF |
| COM Off Capacitance | $\mathrm{C}_{\text {COM(OFF) }}$ |  |  | 5.5 |  |  |
| COM On Capacitance | $\mathrm{C}_{\text {COM }(\mathrm{ON})}$ | $\mathrm{f}=1 \mathrm{kHz}$, Figure 6 |  | 13 |  |  |
| -3dB Bandwidth | BW | $\mathrm{R}_{\mathrm{L}}=50 \Omega$, Figure 7 | Full | 326 |  | MHz |

## Supply

| Power-Supply Range | V+ |  | Full | 2 | 6 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Positve Supply Current | I+ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V}$ or $\mathrm{V}+$ |  |  | 1 | $\mu \mathrm{A}$ |

## Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta \mathrm{R}_{\mathrm{ON}}=\mathrm{R}_{\mathrm{ON}} \max -\mathrm{R}_{\mathrm{ON}} \min$
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are $100 \%$ tested at maximum rated hot temperature and guaranteed by correlation at $+25^{\circ} \mathrm{C}$.
7. Off Isolation $=20 \log _{10}\left[\mathrm{~V}_{\mathrm{COM}} /\left(\mathrm{V}_{\mathrm{NO}}\right.\right.$ or $\left.\left.\mathrm{V}_{\mathrm{NC}}\right)\right]$. See Figure 3.
8. Between any two switches. See Figure 4.

Electrical Specifications - Single + 3.3V Supply
$\left(\mathrm{V}+=+3.3 \mathrm{~V} \pm 10 \%, \mathrm{GND}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{INH}}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}\right)$

| Parameter | Symbol | Conditions | Temp. $\left({ }^{\circ} \mathrm{C}\right)$ | Min.(1) | Typ.(2) | Max.(1) | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Analog Switch |  |  |  |  |  |  |  |
| Analog Signal Range ${ }^{(3)}$ | VaNALOG |  |  | 0 |  | V+ | V |
| On-Resistance | $\mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=3 \mathrm{~V}, \mathrm{I}_{\mathrm{COM}}=-30 \mathrm{~mA}, \mathrm{~V}_{\mathrm{NO}} \text { or } \\ & \mathrm{V}_{\mathrm{NC}}=1.5 \mathrm{~V} \end{aligned}$ | 25 |  | 12 | 18 |  |
|  |  |  | Full |  |  | 22 |  |
| On-Resistance Match Between Channels ${ }^{(4)}$ | $\Delta \mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=3.3 \mathrm{~V}, \mathrm{I}_{\mathrm{COM}}=-30 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=0.8 \mathrm{~V}, 2.5 \mathrm{~V} \end{aligned}$ | 25 |  | 1 | 1 | ת |
|  |  |  | Full |  |  | 2 | $\Omega$ |
| On-Resistance Flatness ${ }^{(3,5)}$ | $\mathrm{R}_{\text {FLAT(ON) }}$ |  | 25 |  | 0.5 | 4 |  |
|  |  |  | Full |  |  | 5 |  |

## Dynamic

| Turn-On Time | ton | $\begin{aligned} & \mathrm{V}+=3.3 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=1.5 \mathrm{~V}, \end{aligned}$ <br> Figure 1 | 25 | 15 | 25 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Full |  | 40 |  |
| Turn-Off Time | toff |  | 25 | 1.5 | 12 |  |
|  |  |  | Full |  | 20 |  |
| Charge Injection ${ }^{(3)}$ | Q | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=1 \mathrm{nF}, \mathrm{~V}_{\mathrm{GEN}}=0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{GEN}}=0 \mathrm{~V}, \text { Figure } 2 \\ & \hline \end{aligned}$ | 25 | 1.3 | 10 | pC |

## Supply

| Positve Supply Current | I + | V+=3.6V, V IN $=0 \mathrm{~V}$ or V+ All <br> Channels on or off | Full |  | 1 | $\mu \mathrm{~A}$ |
| :--- | :---: | :--- | :--- | :--- | :--- | :--- |

Logic Input

| Input High Voltage | $\mathrm{V}_{\mathrm{IH}}$ | Guaranteed logic high level | Full | 2 |  |  | V |
| :--- | :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| Input Low Voltage | $\mathrm{V}_{\mathrm{IL}}$ | Guaranteed logic low level | Full |  |  | 0.8 |  |
| Input High Current | $\mathrm{I}_{\mathrm{INH}}$ | $\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}$, all others $=0.8 \mathrm{~V}$ | Full | -1 |  | 1 | $\mu \mathrm{~A}$ |
| Input Low Current | $\mathrm{I}_{\mathrm{INL}}$ | $\mathrm{V}_{\mathrm{IN}}=0.8 \mathrm{~V}$, all others $=2.4 \mathrm{~V}$ | Full | -1 |  | 1 | $\mu$ |

## Test Circuits/Timing Diagrams


$\mathrm{C}_{\mathrm{L}}$ INCLUDES FIXTURE AND STRAY CAPACITANCE
$v_{\text {OUT }}=V_{\text {NO }}\left(\frac{R_{L}}{R_{L+} R_{O N}}\right)$


LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC * 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time


Figure 2. Charge Injection

Test Circuits/Timing Diagrams (continued)


Figure 3. Off Isolation


Figure 5. Channel-Off Capacitance


Figure 7. Bandwidth


Figure 4. Crosstalk (124 only)


Figure 6. Channel-On Capacitance

Packaging Mechanical: 5-pin SOT-23 (T)


Packaging Mechanical: 5-pin SC70 (C)


Packaging Mechanical: 6-pin SOT-23 (T)


## Ordering Information

| Ordeing Code | Packaging Code | Package Type | Top Marking |
| :--- | :---: | :--- | :---: |
| PI5A121TX | T | 5-pin, 65-mil wide SOT-23 | ZV |
| PI5A121TEX | T | Pb-free \& Green, 5-pin, 65-mil wide SOT-23 | $\overline{\mathrm{Z} V}$ |
| PI5A121CX | C | 5-pin, 50-mil wide SOT-23 | ZV |
| PI5A121CEX | C | Pb-free \& Green, 5-pin, 50-mil wide SOT-23 | $\overline{\mathrm{Z} V}$ |
| PI5A122TX | T | 5-pin, 65-mil wide SOT-23 | ZU |
| PI5A122TEX | T | Pb-free \& Green, 5-pin, 65-mil wide SOT-23 | $\overline{\mathrm{Z} U}$ |
| PI5A122CX | C | 5-pin, 50-mil wide SOT-23 | ZU |
| PI5A122CEX | C | Pb-free \& Green, 5-pin, 50-mil wide SOT-23 | $\overline{\mathrm{Z} U}$ |
| PI5A124TX | T | 6-pin, 65-mil wide SOT-23 | ZT |
| PI5A124TEX | T | Pb-free \& Green, 6-pin, 65-mil wide SOT-23 | $\overline{\mathrm{Z} T}$ |

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. $\mathrm{X}=$ Tape/Reel
