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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



10-Bit Bus Switch with Precharged Outputs

Features

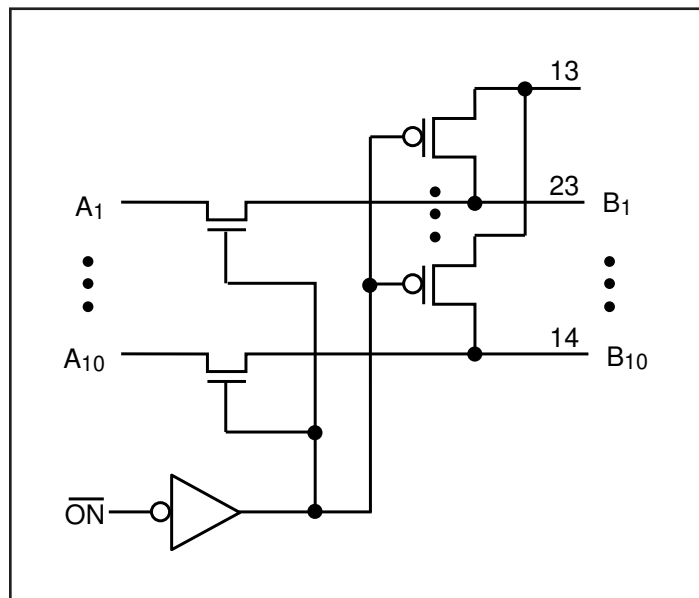
- Near-Zero propagation delay
- 5Ω switch connection between two ports
- Ultra low quiescent power (0.2μA typical)
- Ideally suited for Notebook Applications
- A port is hot swappable
- Packaging (Pb-free & Green available):
 - 24-pin 150-mil wide QSOP (Q)
 - 24-pin 173-mil wide TSSOP (L)

Description

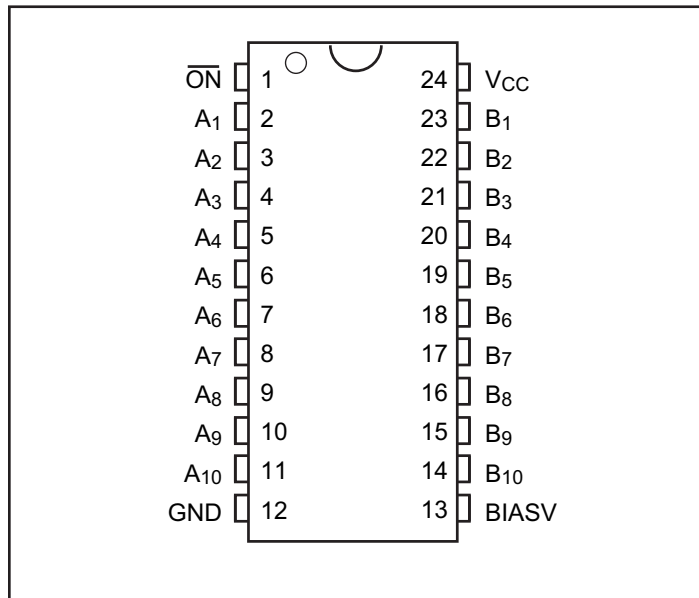
Pericom's Semiconductor's The PI5C6800C is a 10-bit bus switch with low On-State resistance. The bus switch creates no additional propagation delay.

The switch is turned on by a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is LOW, the switch is on and port A is connected to port B. When $\overline{\text{ON}}$ is HIGH, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10k-ohm resistor.

Block Diagram



Pin Configuration



Truth Table⁽¹⁾

Function	$\overline{\text{ON}}$	B ₁ - B ₁₀
Connect	L	A ₁ - A ₁₀
Precharge	H	BIASV

Note:

1. H = High Voltage Level, L = Low Voltage Level

Absolute Maximum Ratings Over Free-Air Temperature Range⁽¹⁾

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	–65°C to +150°C
Supply Voltage Range	–0.5V to +7V
DC Input Voltage ⁽²⁾	–0.5V to +7V
Input Clamp Current, I_{IK} ($V_I < 0$)	–50mA
DC Output Current	120mA
Power Dissipation ⁽³⁾	0.5W

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Parameters	Description	Min.	Typ.	Units
V_{CC}	Supply Voltage	2.3	5.5	V
BIASV	Supply Voltage	1.3	V_{CC}	
V_{IH}	High-level input voltage	2		
V_{IL}	Low-level input voltage		0.8	
T_A	Operating free-air voltage	–40	85	°C

Electrical Characteristics (Over Recommended Operating Free-air Temperature Range)

Parameters	Test Condition		Min.	Typ. ⁽³⁾	Max.	Units
V_{IK}	$V_{CC} = 4.5V$, $I_I = -18mA$				–1.8	V
I_I	$V_{CC} = 5.5V$, $V_I = 5.5V$ or GND				±5	μA
I_O	$V_{CC} = 4.5V$, BIASV = 2.4V, $V_O = 0$		–0.20			mA
I_{CC}	$V_{CC} = 5.5V$, $I_O = 0$, $V_I = V_{CC}$ or GND				100	μA
$\Delta I_{CC}^{(2)}$	$V_{CC} = 3.6V$, One input at 2.7V Other at V_{CC} or GND				2.5	mA
C_{IN}	$V_I = 3V$ or 0			3.5		pF
C_{OFF}	$V_O = 3V$ or 0, Switch Off			4.5		
$R_{ON}^{(1)}$	$V_{CC} = 4V$	$V_I = 2.4V$, $I_I = 15mA$		9	28	Ω
	$V_{CC} = 4.5V$	$V_I = 0V$, $I_I = 64mA$		5.5	8	
		$V_I = 0V$, $I_I = 30mA$		5	8	
		$V_I = 2.4V$, $I_I = 15mA$		9	16	

Notes:

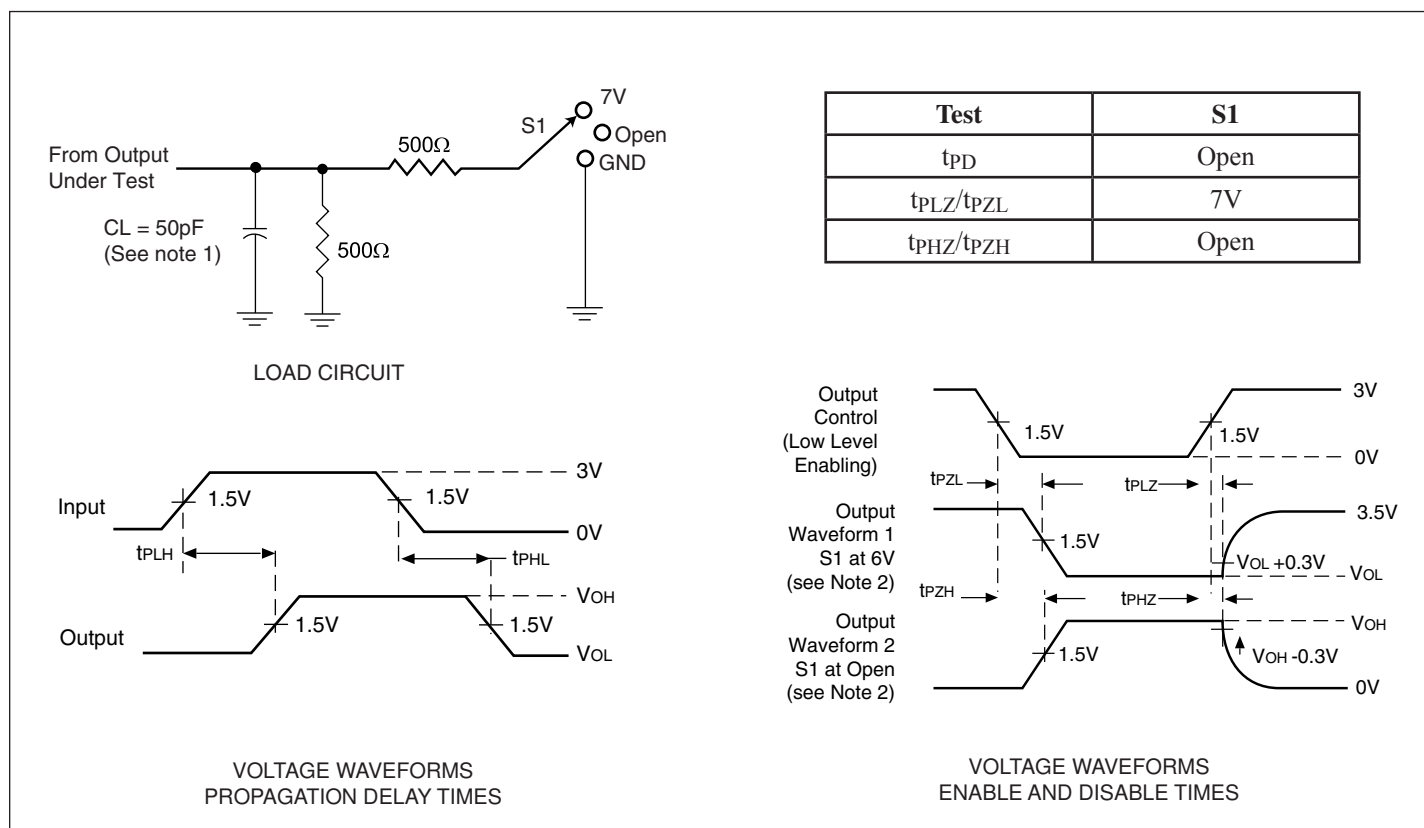
1. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-State resistance is determined by the lower of the voltages of the two (A or B) terminals.
2. This is the increase in supply current for control input.
3. All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Switching Characteristics (Over Recommended Operating Free-air Temperature Range, $C_L = 50\text{pF}$)

Parameter	Test Conditions	From (Input)	To (Input)	$V_{CC} = 5V \pm 0.5V$		$V_{CC} = 4V$		Units
				Min.	Max.	Min.	Max.	
$t_{PD}^{(1)}$		A or B	B or A		0.25		0.25	ns
t_{PZH}	BIASV = GND	ON	A or B	3.1	5		6	
t_{PZL}	BIASV = 3V			3.6	5		6	
t_{PHZ}	BIAS = GND	ON	A or B	2.7	5		5.5	
t_{PLZ}	BIAS = 3V			3	5		5.5	

Notes:

- This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical On-State resistance of the switch and a load capacitance of 50pF, when driven by an ideal voltage source (zero output impedance).

Parameter Measurements

Notes:

- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR < 10\text{MHz}$, $Z_0 = 50\Omega$, $t_r \leq 2.5\text{ns}$, $t_f \leq 2.5\text{ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Applications Information

Logic Inputs

The logic control inputs can be driven up to +5.5V regardless of the supply voltage. For example, given a +5.0V supply, the control input(s) may be driven low to 0V and high to 5.5V. Driving the control input(s) Rail-to-Rail® minimizes power consumption.

Power-Supply Sequencing

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying V_{BIAS} and signals to the input/output or control pins.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Packaging Mechanical: 24-pin TSSOP (L)

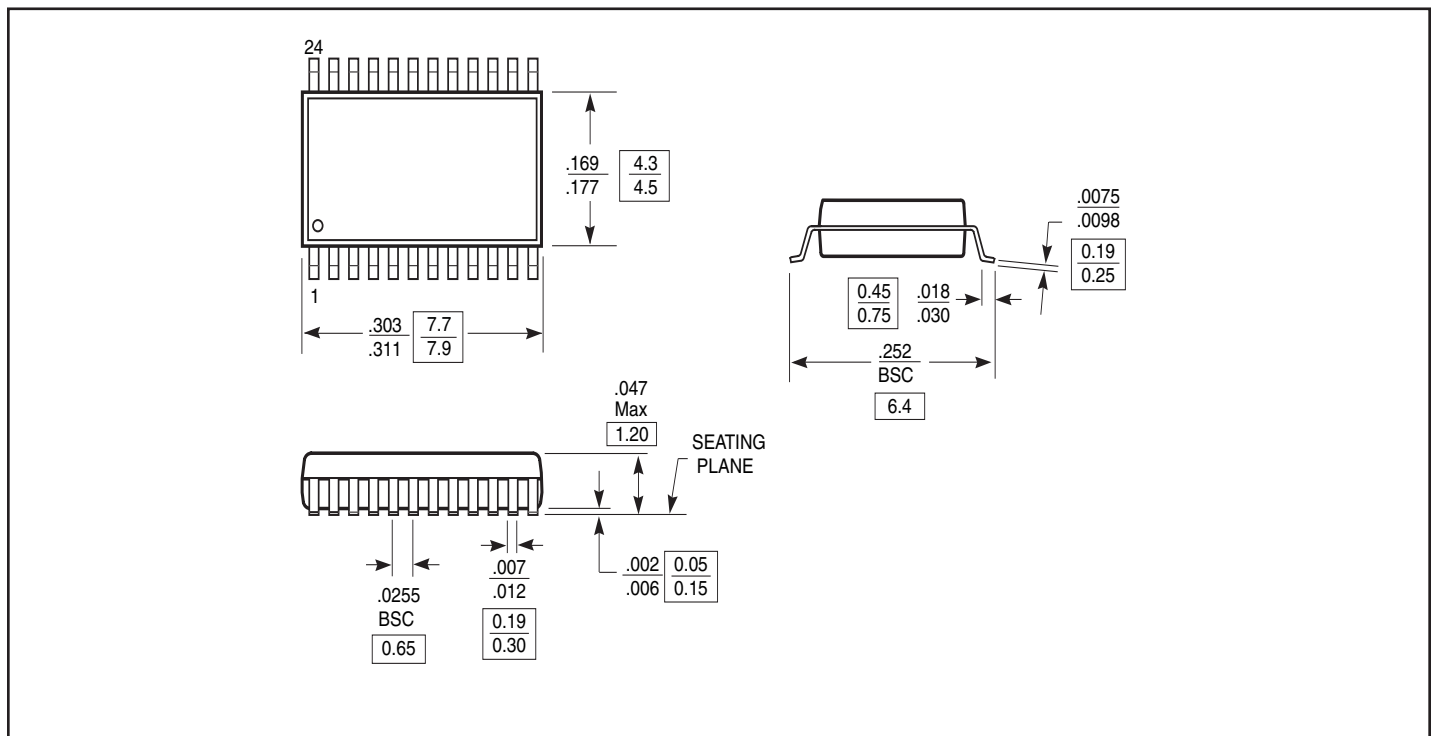


Figure 1: Dimensional drawings of the 100-pin connector. The top drawing is a top view showing a rectangular component with 24 pins on each of the two long sides. Dimensions include a total width of .337 to .344 inches (8.56 to 8.74 mm), a pin pitch of .010 inches (0.254 mm), and a body height of .150 to .157 inches (3.81 to 3.99 mm). The bottom drawing is a side view showing the profile of the component. It includes dimensions for the top width (.033 to 0.84 mm), the body height (.053 to .069 inches / 1.35 to 1.75 mm), the pin height (.025 typical / 0.635 mm), and the pin pitch (.008 to .012 inches / 0.203 to 0.305 mm). A 'SEATING PLANE' is indicated at the base of the pins. The bottom right drawing is a detail view of the pin and body interface, showing a .015 x 45 degree chamfer, a .007 to .010 inch gap, and a .016 to .050 inch dimension for the pin base. A 'Detail A' callout points to the chamfered edge.

Ordering Code	Package Code	Package Description
PI5C6800CL	L	24-Pin 173-mil TSSOP
PI5C6800CLE	L	Pb-free & Green, 24-Pin 173-mil TSSOP
PI5C6800CQ	Q	24-Pin 150-mil QSOP
PI5C6800CQE	Q	Pb-free & Green, 24-Pin 150-mil QSOP

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel