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Features

- High-speed, to 140 MHz
- Low-noise non-inverting 1-18 buffer
- Supports up to four SDRAM DIMMs
- Low skew (< 250ps) between any two output clocks
- I²C Serial Configuration interface
- Multiple V_{DD}, V_{SS} pins for noise reduction
- 3.3V power supply voltage
- Separate Hi-Z pin for testing
- Packaging: (Pb-free and Green)
— 48-pin SSOP (V48)

Description

The PI6C180B, a high-speed low-noise 1-18 noninverting buffer designed for 140 MHz SDRAM clock buffer applications.

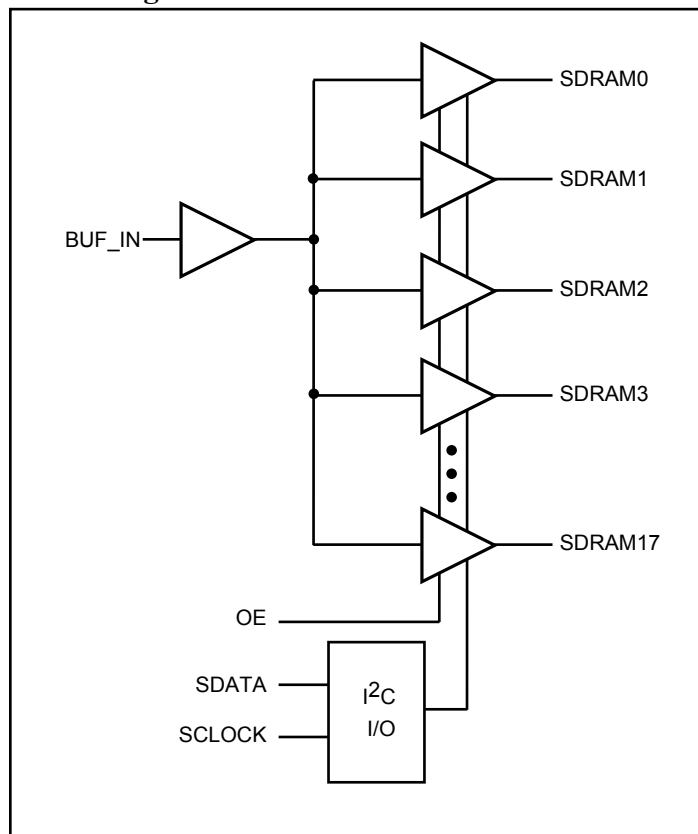
At power up all SDRAM output are enabled and active. The I²C Serial control may be used to individually activate/deactivate any of the 18 output drivers.

The output enable (OE) pin may be pulled low to put all outputs in a Hi-Z state.

Note:

Purchase of I²C components from Pericom conveys a license to use them in an I²C system as defined by Philips.

Block Diagram



Pin Configuration

NC	1	48	NC
NC	2	47	NC
V _{DD0}	3	46	V _{DD9}
SDRAM0	4	45	SDRAM15
SDRAM1	5	44	SDRAM14
V _{SS0}	6	43	V _{SS9}
V _{DD1}	7	42	V _{DD8}
SDRAM2	8	41	SDRAM13
SDRAM3	9	40	SDRAM12
V _{SS1}	10	39	V _{SS8}
BUF_IN	11	38	OE
V _{DD2}	12	37	V _{DD7}
SDRAM4	13	36	SDRAM11
SDRAM5	14	35	SDRAM10
V _{SS2}	15	34	V _{SS7}
V _{DD3}	16	33	V _{DD6}
SDRAM6	17	32	SDRAM9
SDRAM7	18	31	SDRAM8
V _{SS3}	19	30	V _{SS6}
V _{DD4}	20	29	V _{DD5}
SDRAM16	21	28	SDRAM17
V _{SS4}	22	27	V _{SS5}
VDDIIC	23	26	V _{SSIIC}
SDATA	24	25	SCLOCK

Pin Description

Pin	Symbol	Type	Qty	Description
4, 5, 8, 9	SDRAM[0-3]	O	4	SDRAM Byte 0 clock output
13, 14, 17, 18	SDRAM[4-7]	O	4	SDRAM Byte 1 clock output
31, 32, 35, 36	SDRAM[8-11]	O	4	SDRAM Byte 2 clock output
40, 41, 44, 45	SDRAM[12-15]	O	4	SDRAM Byte 3 clock output
21, 28	SDRAM[16-17]	O	4	SDRAM clock outputs usable for feedback
11	Buf_IN	I	1	Input for 1-18 buffer
38	OE	I	1	Hi-Z all outputs when held LOW. Has a >100kΩ internal pull-up resistor
24	S _{DATA}	I/O	1	Data pin for I ² C circuitry. Has a >100kΩ internal pull-up resistor
25	S _{CLOCK}	I/O	1	Clock pin for I ² C circuitry. Has a >100kΩ internal pull-up resistor
3, 7, 12, 16, 20, 29, 33, 37, 42, 46	V _{DD} [0-9]	Power	10	3.3V power supply for SDRAM buffers
6, 10, 15, 19, 22, 27, 30, 34, 39, 43	V _{SS} [0-9]	Ground	10	Ground for SDRAM buffers
23	V _{DDIIC}	Power	1	3.3V power supply for I ² C circuitry
26	V _{SSIIC}	Ground		Ground for I ² C circuitry
1, 2, 47, 48	NC	Reserved	4	Reserved for future modifications. No connects

OE Functionality

OE	SDRAM[0-17]	Notes
0	Hi-Z	1
1	BUF_IN	2

Notes:

- Used for test purposes only
- Buffers are non-inverting

I²C Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0

Serial Configuration Map

Byte0: SDRAM Active/Inactive Register

(1 = enable, 0 = disable)

Bit	Pin	Description
7	18	SDRAM7 (Active/Inactive)
6	17	SDRAM6 (Active/Inactive)
5	14	SDRAM5 (Active/Inactive)
4	13	SDRAM4 (Active/Inactive)
3	9	SDRAM3 (Active/Inactive)
2	8	SDRAM2 (Active/Inactive)
1	5	SDRAM1 (Active/Inactive)
0	4	SDRAM0 (Active/Inactive)

Note:

- Inactive means outputs are held LOW and are disabled from switching.

2-Wire I²C Control

The I²C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C180B is a slave receiver device. It can not be read back. Sub addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Every bite put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device. During normal data transfers SDATA changes only when SCLOCK is LOW. Exceptions: A HIGH to LOW transition on SDATA while SCLOCK is HIGH indicates a “start” condition. A LOW to HIGH transition on SDATA while SCLOCK is HIGH is a “stop” condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW = write to addressed device). If the device’s own address is detected, PI6C180B generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (D2), two more bytes must be sent:

1. “Command Code” byte, and
2. “Byte Count” byte.

Although the data bits on these two bytes are “don’t care,” they must be sent and acknowledged.

Byte1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin	Description
7	45	SDRAM15 (Active/Inactive)
6	44	SDRAM14 (Active/Inactive)
5	41	SDRAM13 (Active/Inactive)
4	40	SDRAM12 (Active/Inactive)
3	36	SDRAM11 (Active/Inactive)
2	35	SDRAM10 (Active/Inactive)
1	32	SDRAM9 (Active/Inactive)
0	31	SDRAM8 (Active/Inactive)

Byte2: Optional Register for Possible Future Requirements (1 = enable, 0 = disable)

Bit	Pin	Description
7	28	SDRAM17 (Active/Inactive)
6	21	SDRAM16 (Active/Inactive)
5		(Reserved)
4		(Reserved)
3		(Reserved)
2		(Reserved)
1		(Reserved)
0		(Reserved)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	–65°C to +150°C
Ambient Temperature with Power Applied.....	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
DC Input Voltage.....	–0.5V to +4.6V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Supply Current (V_{DD} = +3.465V, C_{LOAD} = Max.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I _{DD}	Supply Current	BUF_IN = 0 MHz			2	mA
I _{DD}		BUF_IN = 66.66 MHz			230	
I _{DD}		BUF_IN = 100.00 MHz			360	

DC Operating Specifications ($V_{DD} = +3.3V \pm 5\%$, $T_A = 0^\circ C - 70^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input Voltage						
V_{IH}	Input High voltage	V_{DD}	2.0		$V_{DD} + 0.3$	V
V_{IL}	Input Low voltage		$V_{SS} - 0.3$		0.8	
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DD}$	-5		5	mA
$V_{DD} [0-9] = 3.3V \pm 5\%$						
V_{OH}	Output High voltage	$I_{OH} = -1mA$	2.4			V
V_{OL}	Output Low voltage	$I_{OL} = 1mA$			0.4	
C_{OUT}	Output pin capacitance			6		pF
C_{IN}	Input pin capacitance			5		
L_{PIN}	Pin Inductance			7		nH
T_A	Ambient Temperature	No Airflow	0		70	$^\circ C$

SDRAM Clock Buffer Operating Specification

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	$V_{OUT} = 2.0V$	-40			mA
I_{OHMAX}	Pull-up current	$V_{OUT} = 3.135V$			36	
I_{OLMIN}	Pull-down current	$V_{OUT} = 1.0V$	40			
I_{OLMAX}	Pull-down current	$V_{OUT} = 0.4V$			38	
$t_{RHSDRAM}$	Output rise edge rate SDRAM only	$3.3V \pm 5\% @ 0.4V - 2.4V$	1.5		4	V/ns
$t_{THSDRAM}$	Output fall edge rate SDRAM only	$3.3V \pm 5\% @ 2.4V - 0.4V$	1.5		4	

AC Timing

Symbol	Parameter	66 MHz		100 MHz		133 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SDRISE}	SDRAM CLK rise time	1.5	4.0	1.5	4.0	1.5	4.0	V/ns
t_{SDFALL}	SDRAM CLK fall time	1.5	4.0	1.5	4.0	1.5	4.0	
t_{PLH}	SDRAM Buffer LH prop delay	1.0	5.5	1.0	5.5	1.0	5.5	ns
t_{PHL}	SDRAM Buffer HL prop delay	1.0	5.5	1.0	5.5	1.0	5.5	
t_{PZL}, t_{PZH}	SDRAM Buffer Enable delay ⁽¹⁾	1.0	8.0	1.0	8.0	1.0	8.0	
t_{PLZ}, t_{PHZ}	SDRAM Buffer DIsable delay ⁽¹⁾	1.0	8.0	1.0	8.0	1.0	8.0	
Duty Cycle	Measured at 1.5V	45	55	45	55	45	55	%
t_{SDSKW}	SDRAM Output-to-Output skew		250		250		250	ps

Note:

- This Parameter specified at 5MHz input frequency.

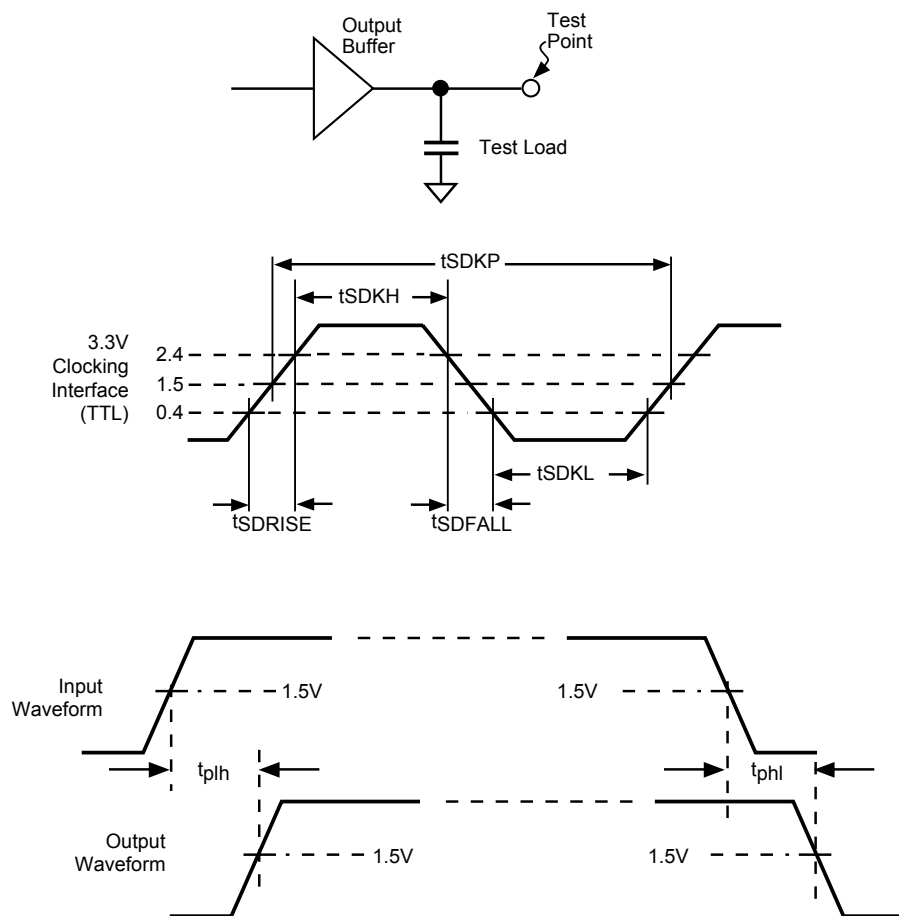


Figure 1. Clock Waveforms

Minimum and Maximum Expected Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
SDRAM	15	20	pF	SDRAM DIMM Specification

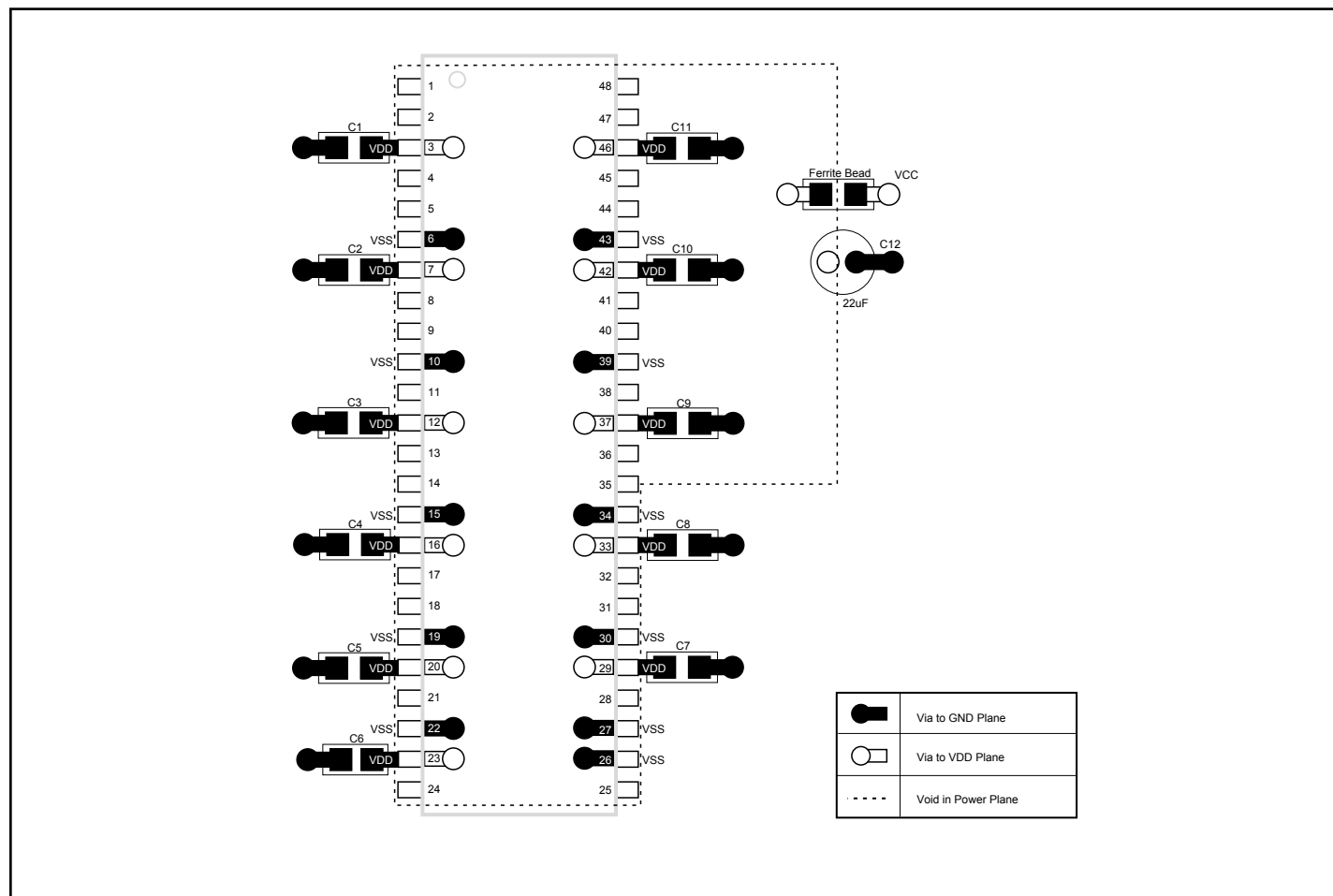
Notes:

- Maximum rise/fall times are guaranteed at maximum specified load.
- Minimum rise/fall times are guaranteed at minimum specified load.
- Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

- Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
- Minimize the number of “vias” of the clock traces.
- Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
- Position clock signals away from signals that go to any cables or any external connectors.

PCB Layout Suggestion



Note:

1. This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.
2. As a general rule, C1-C11 should be placed as close as possible to their respective VDD.
3. Recommended capacitor values:
C1-C11 0.1µF, ceramic
C12 22µF

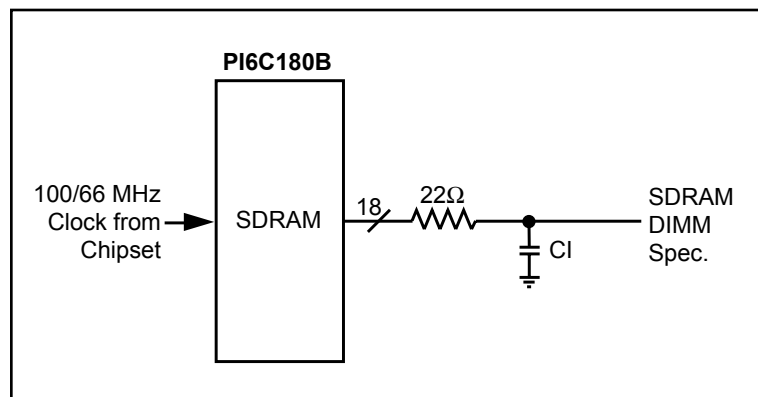
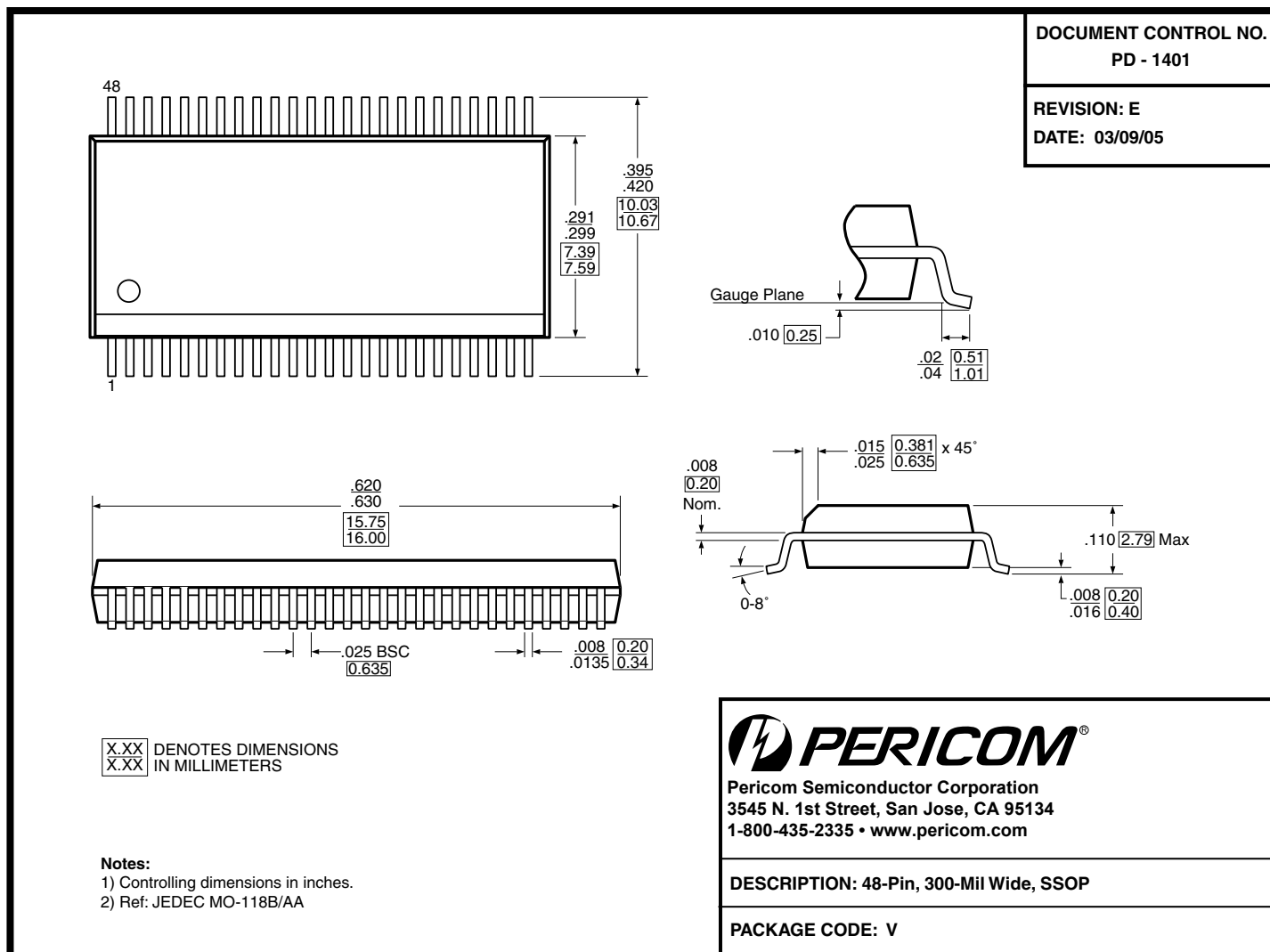


Figure 2. Design Guidelines



Ordering Information⁽¹⁻³⁾

Ordering Code	Package Code	Package Type
PI6C180BVE	V	Pb-free and Green, 48-pin SSOP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Lead-free and Green
- X suffix = tape/reel