Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PI6C485352

2.5V/3.3V, 500 MHz Twelve 2-to-1 Differential LVPECL Clock Multiplexer

Features

- Pin-to-pin compatible to ICS85352I
- FMAX ≤ 500 MHz
- Propagation Delay < 4ns
- Output-to-output skew < 100ps
- 12 pairs of differential LVPECL outputs
- Selectable differential CLK and /CLK inputs
- CLK, /CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- Select input accept CMOS/LVTTL levels
- 2.5V/3.3V power supply
- Operating Temperature: -40°C to +85°C
- Packaging (Pb-free & Green):
  - 48-pin TQFP (FA)

Description

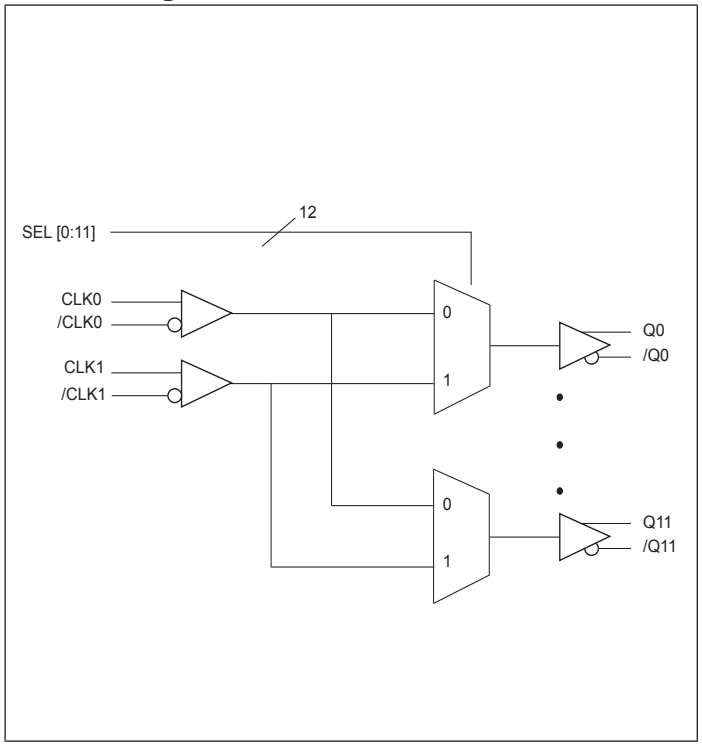
The PI6C485352 is a high-performance low-skew LVPECL fanout buffer. PI6C485352 features two selectable differential inputs and translates to twelve LVPECL output pairs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LVPECL, LVDS, LVHSTL, SSTL or HCSL signals. The PI6C485352 is ideal for differential to LVPECL translations and/or LVPECL clock distribution.

Typical clock translation and distribution applications are data-communications and telecommunications.

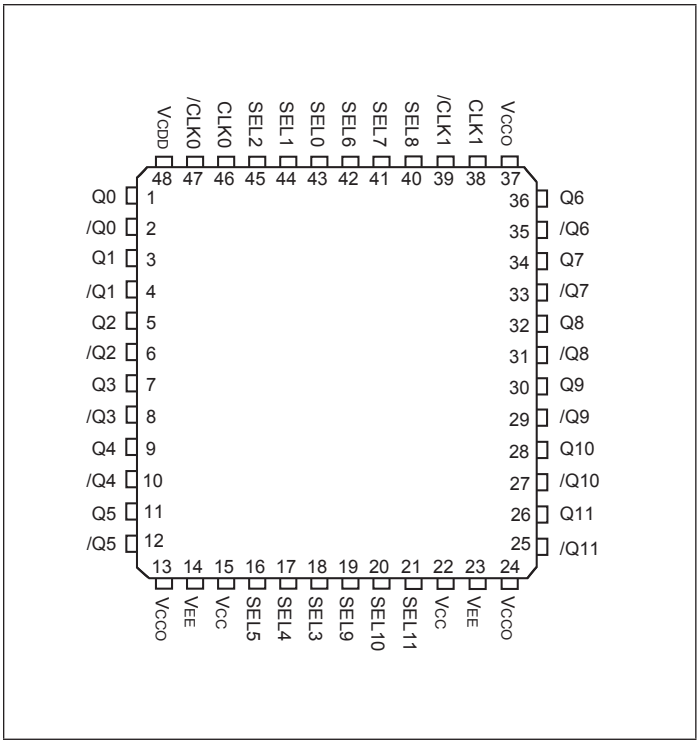
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (48-Pin TQFP)



Pinout Table

Pin #	Pin Name	Type		Description
1, 2 3, 4 5, 6 7, 8 9, 10 11, 12 25, 26 27, 28 29, 30 31, 32 33, 34 35, 36	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 /Q11, Q11 /Q10, Q10 /Q9,Q9 /Q8,Q8 /Q7,Q7 /Q6,Q6	Output		Differential LVPECL Output pairs. LVPECL interface levels
13, 24 37, 48	V_{CCO}	Power		Output supply pins
14, 23	V_{EE}			Ground pins
15, 22	V_{CC}			Core supply pins
16, 17 18, 19 20, 21 40, 41 42, 43 44, 45	SEL5, SEL4, SEL3, SEL9, SEL10, SEL11, SEL8, SEL7, SEL6, SEL0, SEL1, SEL2	Pulldown		Clock select inputs. LVCMOS/LVTTL interface levels
38	CLK1	Pulldown		Non-inverting differential clock input
39	/CLK1	Pullup/Pulldown		Inverting differential clock input
46	CLK0	Pulldown		Non-inverting differential clock input
47	/CLK0	Pullup/Pulldown		Inverting differential clock input

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CC}/ V_{CCo}	Supply Voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{CC}+0.5V	
Outputs, I_O	Surge current				100	mA
TSTG	Storage temperature		-65		150	°C
θ_{jA}	Package thermal impedence				73	°C/W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
CIN	Input Capacitance				4	pF
Rpullup	Input Pullup Resistance			50		kΩ
Rpulldown	Input Pulldown Resistance			50		kΩ

Control Input Function Table

SELX	Selected Clock Inputs
0	CLK0, /CLK0
1	CLK1, /CLK1

Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
V_{CCO}	Output Power Supply Voltage		2.375		3.6	V
T_A	Ambient Temperature		-40		85	°C
I_{EE}	Power Supply Current				200	mA

LVCMOS/LVTTL DC Characteristics (TA = -40°C to +85°C, VCC = 3.3V ±10%, VCCO = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High voltage	SEL0:SEL11		2		V_{CC}+0.3	V
V_{IL}	Input Low voltage	SEL0:SEL11		-0.3		0.8	
I_{IH}	Input High current	SEL0:SEL11	VIN = VCC = 3.6V			150	µA
I_{IL}	Input Low current	SEL0:SEL11	VIN = 0V, VCC = 3.6V	-5			µA

Differential DC Characteristics (TA = -40°C to +85°C, VCC = 3.3V ±10%, VCCO = 2.5V ±5% to 3.3V ±10%)

Parameter	Description		Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{CC} = 3.6V$			150	µA
		/CLK0, /CLK1	$V_{IN} = V_{CC} = 3.6V$			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	$V_{CC} = 3.6V, V_{IN} = 0V$	-5			µA
		/CLK0, /CLK1	$V_{CC} = 3.6V, V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage(1)			V_{EE}+0.5		V_{CC}-0.85V	V
V_{OH}	Output High Voltage(2)		V_{CCO} = 3.3V or 2.5V	V_{CCO}-1.4		V_{CCO}-0.9	V
V_{OL}	Output Low Voltage(2)		V_{CCO} = 3.3V or 2.5V	V_{CCO}-2.0		V_{CCO}-1.7	V

Note:

1. Outputs terminated with 50Ω to V_{CCO} -2.0V

AC Characteristics (TA = -40°C to +85°C, VCC = 3.3V ±10%, VCCO = 2.5V ±5% to 3.3V ±10%)

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
fmax	Output Frequency				500	MHz
tpd	Propagation Delay(1)				4	ns
Tsk	Output-to-output Skew(2)				100	ps
Tskpp	Part-to-part Skew(3)				500	ps
tr/tf	Output Rise/Fall time	20% - 80%	150		700	ps
odc	Output duty cycle		45		55	%
T_j	Buffer additive jitter RMS			0.05		ps

Note:

1.Measured from the differential input to the differential output crossing point

2 Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point.

3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal loads. Measured at the outputs differential crossing point.

Applications Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = VCC/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be placed as close as possible to the input pin. The ratio of R1 and R2 should be adjusted to postion the V_REF at the center of the input voltage swing. For example, if the input clock swing is 2.5V and VCC = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

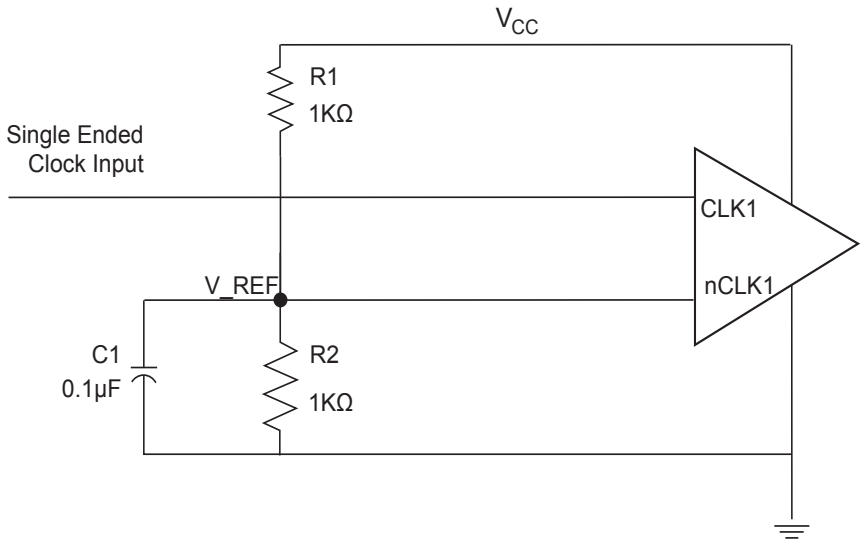
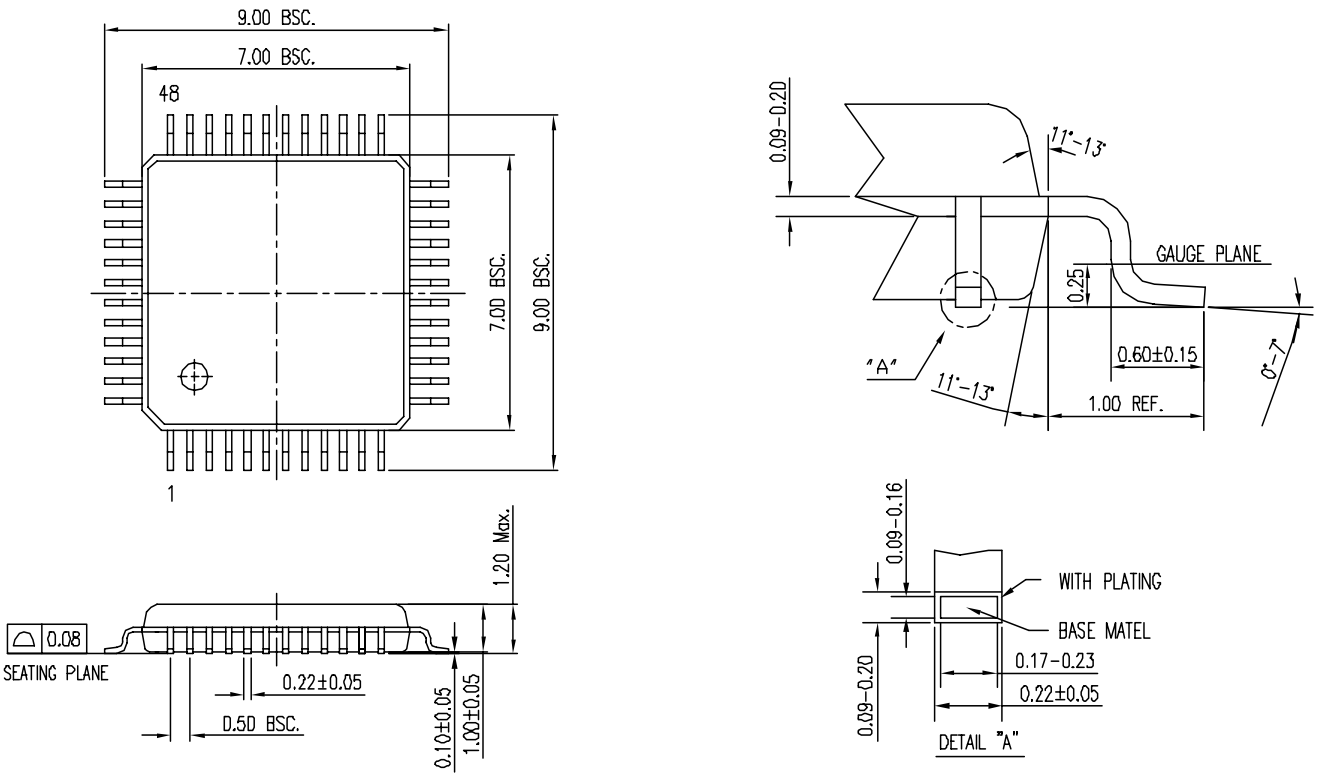


Figure 1: Single-ended Signal Driving Differential Input

Packaging Mechanical: 48-Pin TQFP (FA)



Notes:
1) All dimensions are in millimeters, Angles in Degrees
2) Ref JEDEC: MO-026D, variation ABC
3) Dimensions do not include mold protrusion

PERICOM Semiconductor Corporation — DATE: 02/16/06

DESCRIPTION: 48-pin Thin Quad Flat Package (TQFP)

PACKAGE CODE: FA48

DOCUMENT CONTROL #: PD-2056 — REVISION: - -

06-0182

Ordering Information

Ordering Number	Package Code	Package Description
PI6C485352FAE	FA	Pb-free & Green, 48-pin, 276-mil wide TQFP

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**