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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PCIe® Gen 2 Networking Clock Generator

Features

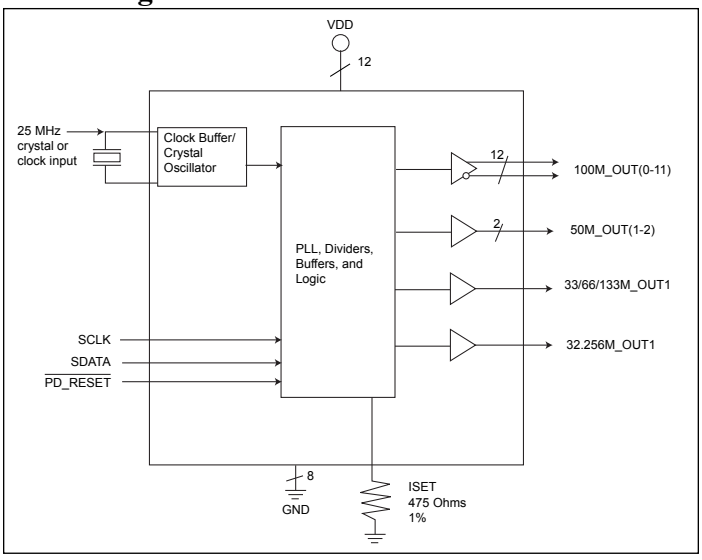
- 3.3V +/-10% Supply Voltage
- Uses 25MHz xtal such as Saronix-eCera™ SRX7278
- Twelve PCIe® Gen. 2 100MHz HCSL outputs with optional -0.5% spread spectrum support
- Two LVCMOS 50MHz outputs that support +/- 10% frequency margining
- One frequency selectable 33/66/133MHz LVCMOS output
- One 32.256MHz LVCMOS output
- Industrial temperature -40°C to 85°C
- Package: 56-pin TSSOP package

Description

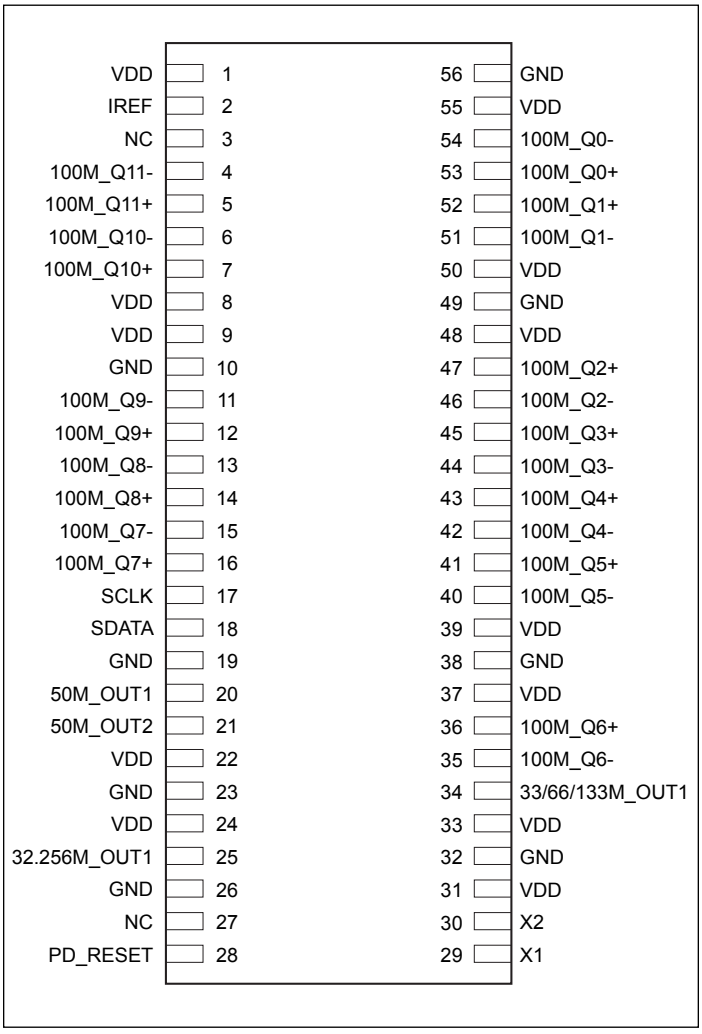
The PI6C49004A is a clock generator device intended for PCIe® Gen2 networking applications. The device includes twelve 100MHz differential Host Clock Signal Level (HCSL) outputs for PCIe Gen 2, two single-ended 50MHz outputs, one single-ended 32.256MHz output, and one selectable single-ended 33/66/133MHz output.

Using a serially programmable SMBUS interface, the PI6C49004A incorporates spread spectrum modulation on the twelve 100MHz HCSL PCIe Gen 2 outputs, and independent frequency margining on the 50MHz output, 33.3333MHz and 66.6666MHz clock outputs.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	V_{DD}	Power	3.3V Supply Pin
2	IREF	Output	Connect to 475-Ohm resistor to set HCSL output drive current
3	NC		No connect. Leave open
4	100M_Q11-	Output	100MHz HCSL output
5	100M_Q11+	Output	100MHz HCSL output
6	100M_Q10-	Output	100MHz HCSL output
7	100M_Q10+	Output	100MHz HCSL output
8	V_{DD}	Power	3.3V Supply Pin
9	V_{DD}	Power	3.3V Supply Pin
10	GND	Power	Ground
11	100M_Q9-	Output	100MHz HCSL output
12	100M_Q9+	Output	100MHz HCSL output
13	100M_Q8-	Output	100MHz HCSL output
14	100M_Q8+	Output	100MHz HCSL output
15	100M_Q7-	Output	100MHz HCSL output
16	100M_Q7+	Output	100MHz HCSL output
17	SCLK	Input	SMBus compatible input clock. Supports fast mode 400kHz input clock.
18	SDATA	I/O	SMBus compatible data line
19	GND	Power	Ground
20	50M_Out1	Output	50MHz LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
21	50M_Out2	Output	50MHz LVCMOS output. When disabled, output is trisated and has a nominal 110kOhm pull-down.
22	V_{DD}	Power	3.3V Supply Pin
23	GND	Power	Ground
24	V_{DD}	Power	3.3V Supply Pin
25	32.256M_Out1	Output	32.256MHz LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
26	GND	Power	GND
27	NC		No connect. Leave open
28	$\overline{\text{PD\_RESET}}$	Input	Power down reset - when low all PLL's are powered down and outputs tristated. SMBus registers are reset to default values. When Byte0-Bit 6 = 0 (Hardware Control Mode) $\overline{\text{PD RESET}}$ = high, all outputs are enabled
29	X1	Input	Crystal input. Integrated 6pF capacitance
30	X2	Output	Crystal output. Integrated 6pF capacitance
31	V_{DD}	Power	3.3V Supply Pin
32	GND	Power	GND

(Continued)

Pin Description (Cont..)

Pin #	Pin Name	Pin Type	Pin Description
33	V_{DD}	Power	Connect to 3.3V
34	33/66/133M_Out1	Output	33/66/133MHz selectable LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
35	100M_Q6-	Output	100MHz HCSL output
36	100M_Q6+	Output	100MHz HCSL output
37	V_{DD}	Power	3.3V Supply Pin
38	GND	Power	Ground
39	V_{DD}	Power	3.3V Supply Pin
40	100M_Q5-	Output	100MHz HCSL output
41	100M_Q5+	Output	100MHz HCSL output
42	100M_Q4-	Output	100MHz HCSL output
43	100M_Q4+	Output	100MHz HCSL output
44	100M_Q3-	Output	100MHz HCSL output
45	100M_Q3+	Output	100MHz HCSL output
46	100M_Q2-	Output	100MHz HCSL output
47	100M_Q2+	Output	100MHz HCSL output
48	V_{DD}	Power	3.3V Supply Pin
49	GND	Power	Ground
50	V_{DD}	Power	3.3V Supply Pin
51	100M_Q1-	Output	100MHz HCSL output
52	100M_Q1+	Output	100MHz HCSL output
53	100M_Q0-	Output	100MHz HCSL output
54	100M_Q0+	Output	100MHz HCSL output
55	V_{DD}	Power	3.3V Supply Pin
56	GND	Power	Ground

50MHz Frequency Margining Table

FS3	FS2	FS1	FS0	50M_OUT1, 50M_OUT2
0	0	0	0	nominal
0	0	0	1	nominal + 1%
0	0	1	0	nominal + 2%
0	0	1	1	nominal + 3%
0	1	0	0	nominal + 4%
0	1	0	1	nominal + 5%
0	1	1	0	nominal + 6%
0	1	1	1	nominal + 8%
1	0	0	0	nominal + 10%
1	0	0	1	nominal - 1%
1	0	1	0	nominal - 2%
1	0	1	1	nominal - 3%
1	1	0	0	nominal - 4%
1	1	0	1	nominal - 6%
1	1	1	0	nominal - 8%
1	1	1	1	nominal - 10%

33/66/133 MHz Frequency Margining Table

FS6	**FS5**	**FS4**	**33M/66M/133M_OUT1**
0	0	0	33.3333MHz
0	0	1	66.6666MHz +2%
0	1	0	66.6666MHz +1%
0	1	1	66.6666MHz +0%
1	0	0	66.6666MHz -2%
1	0	1	66.6666MHz -4%
1	1	0	66.6666MHz -6%
1	1	1	133.3333MHz

Serial Data Interface (SMBus)

PI6C49004A is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	D2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:
1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting databyte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Spectrum Selection for 100MHz HCSL PCI-Express clocks	RW	0	All 100MHz HCSL PCI Express outputs	0=spread off 1 = -0.5% down spread
6	Enables hardware or software control of OE bits (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{\text{PD\_RESET}}$ pin, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{\text{PD\_RESET}}$ bit. Enables or disables all outputs (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4	Frequency margining select bit FS3	RW	1	50M_Out1 and 50M_ Out2	See 50MHz Frequency Margining Table on Page 3
3	Frequency margining select bit FS2	RW	0		
2	Frequency margining select bit FS1	RW	1		
1	Frequency margining select bit FS0	RW	0		
0	OE for single-ended 50MHz output 50M_Out2	RW	1	Single-ended 50MHz output 50M_Out2	0 = disabled 1 = enabled

Byte 0 - Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	($\overline{\text{PD\_RESET}}$ = "H" will enable all outputs; SMBus cannot control each output.)
1	0	Disables all outputs and tri-states the outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE
1	1	Enable outputs according to the SMBus default values; SMBus can control each output. $\overline{\text{PD\_RESET}}$ HW pin/signal = DON'T CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 32.256M_Out1	RW	1	32.256M_Out1	0 = disabled 1 = enabled
6	OE for 50M_Out1	RW	1	50M_Out1	0 = disabled 1 = enabled
5	OE for 33/66/133M_Out1	RW	1	33/66/133M_Out1	0 = disabled 1 = enabled
4	OE for 100M_Q11 HCSL output	RW	1	100M_Q11	0 = disabled 1 = enabled
3	OE for 100M_Q10 HCSL output	RW	0	100M_Q10	0 = disabled 1 = enabled
2	OE for 100M_Q09 HCSL output	RW	0	100M_Q9	0 = disabled 1 = enabled
1	OE for 100M_Q08 HCSL output	RW	0	100M_Q8	0 = disabled 1 = enabled
0	OE for 100M_Q07 HCSL output	RW	0	100M_Q7	0 = disabled 1 = enabled

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Frequency margining select bit FS6	RW	1	33/66/133M_Out1	See 33/66/133MHz Frequency Margining Table on Page 3
6	Frequency margining select bit FS5	RW	0		
5	Frequency margining select bit FS4	RW	0		
4 to 0	Reserved	R	Undefined	Not Applicable	

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 100M_Q6 HCSL Output	RW	0	100M_Q6	0 = disabled 1 = enabled
6	OE for 100M_Q5 HCSL Output	RW	0	100M_Q5	0 = disabled 1 = enabled
5	OE for 100M_Q4 HCSL Output	RW	0	100M_Q4	0 = disabled 1 = enabled
4	OE for 100M_Q3 HCSL Output	RW	0	100M_Q3	0 = disabled 1 = enabled
3	OE for 100M_Q2 HCSL Output	RW	0	100M_Q2	0 = disabled 1 = enabled
2	OE for 100M_Q1 HCSL Output	RW	1	100M_Q1	0 = disabled 1 = enabled
1	OE for 100M_Q0 HCSL Output	RW	1	100M_Q0	0 = disabled 1 = enabled
0	Reserved	R	Undefined	Not Applicable	

Byte 4 & 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revivsion ID bit 3	R	0	Not Applicable	
6	Revivsion ID bit 2	R	0	Not Applicable	
5	Revivsion ID bit 1	R	0	Not Applicable	
4	Revivsion ID bit 0	R	0	Not Applicable	
3	Vendor ID bit 3	R	0	Not Applicable	
2	Vendor ID bit 2	R	0	Not Applicable	
1	Vendor ID bit 1	R	1	Not Applicable	
0	Vendor ID bit 0	R	1	Not Applicable	

Absolute Maximum Ratings[1] (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	V
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Note:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, V_{DD} 7V
All Inputs and Outputs .....–0.5V to V_{DD} +0.5V
Ambient Operating Temperature.....–40°C to +85°C
Storage Temperature.....–65°C to +150°C
Junction Temperature .....125°C
Peak Soldering Temperature.....260°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Supply Voltage	V_{DD}		3.0		3.6	V
Input High Voltage	V_{IH}		2		V_{DD}	
Input Low Voltage	V_{IL}		–0.3		0.8	
Input High Voltage	V_{IH}	SDATA, SCLK	$0.7V_{DD}$		V_{DD}	
Input Low Voltage	V_{IL}	SDATA, SCLK			$0.3V_{DD}$	
Operating Supply Current	I_{DD}			320		mA
IDD at Output Disable Condition		$\overline{\text{PD\_RESET}}$ = 0		3.0		
Internal Pull-Up/Pull-Down Resistor	R_{PU}/R_{PD}	$\overline{\text{PD\_RESET}}$		216		k–Ohm
		All single-ended outputs		75		
Input Capacitance	C_{IN}	All input pins		6		pF

Electrical Characteristics - Single-Ended

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Frequency	F_{IN}			25		MHz
SCLK Frequency				100	400	kHz
Minimum Pulse Width of $\overline{\text{PD\_RESET}}$ Input			100			ns
Output Frequency Error		FS0, FS6 = 0		0		ppm
Output Frequency Error		32.256MHz			7	
Output Rise/Fall Time	t_r, t_f	V_{DD}=3.3V, 0.8V to 2.4V		0.5	1	ns
Output Clock Duty Cycle		Measured at $V_{DD}/2$	45	50	55	%
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DD}-0.4			V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	2.4			
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	
Peak-to-Peak Jitter		50MHz clock output		140	200	ps
		33/66/133MHz clock output		125	175	
		32.256MHz clock output		115	150	
Cycle-to-Cycle Jitter		50MHz clock output		120	175	
		33/66/133 MHz clock output		120	160	
Clock Stabilization Time from Power Up			3		10	ms

Electrical Characteristics - 100MHz Differential HCSL Outputs

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency					100	MHz
Cycle-to-Cycle Jitter	$T_{CC/Jitter}$				150	ps
Peak-to-Peak Phase Jitter		Using PCIe jitter measurement method			86	
PCIe 2.0 RMS Phase Jitter	$J_{RMS2.0}$	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
Spread Modulation Percentage				-0.5	0	%
Spread Modulation Frequency				32		kHz
Duty Cycle	T_{DC}		45	50	55	%
Rising/Falling Edge Rate		Note 3, 4	0.6		4.5	V/ns
Output Skew	T_{OSKEW}	V_T = 50%(measurement threshold)			200	ps
Clock Source DC Impedance, single ended	Z_{C-DC}			50		Ohm
High-Level Output Voltage	V_{OH}	Note 2, (R_S=33-Ohm, R_T=50-Ohm)	0.65	0.71	0.95	V
Low-Level Output Voltage	V_{OL}		–0.20	0	0.05	
I_{OH} @ 6*I_{REF}	I_{OH}		–13	–14.2	-18.5	mA
Absolute Crossing Point Voltage	V_{CROSS}	Note 2, 5, 6	0.25		0.55	V
Variation of VCROSS over all rising clock edges	$V_{CROSS\ Delta}$	Note 2, 5, 8			140	mV
Average Clock Period Accuracy	$T_{PERIOD\ AVG}$	Note 3, 9, 10	–300		2800	ppm
Absolute Period (including jitter and spread spectrum)	$T_{PERIOD\ ABS}$	Note 3, 7	9.847		10.203	ns

(Continued)

Notes:

1. Measured at the end of an 8-inch trace with a 5pF load.
2. Measurement taken from a single-ended waveform.
3. Measurement taken from a differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
5. Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M–.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
7. Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
8. Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M–.
9. Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.
10. 10) PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 PPM there is an error budget of 100Hz/PPM * 300 PPM = 30 kHz. The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than ±300 ppm. With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.

Crystal Load Capacitors

If an input crystal is used, crystal should be connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L = Crystal's load capacitance in pF

Crystal Capacitors (pF) = (C_L - 8) *2

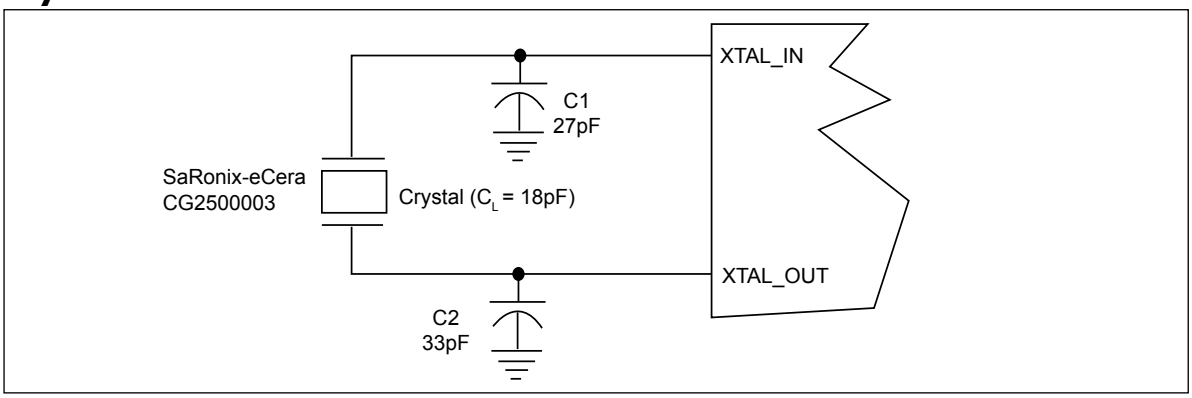
For example, for a crystal with a 18pF load cap, each external crystal cap would be 18pF. (18 - 8) *2 =18.

Application Notes

Crystal circuit connection

The following diagram shows PI6LC4830-01 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 33pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



Recommended Crystal Specification

Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Configuration test load board termination for HCSL Outputs

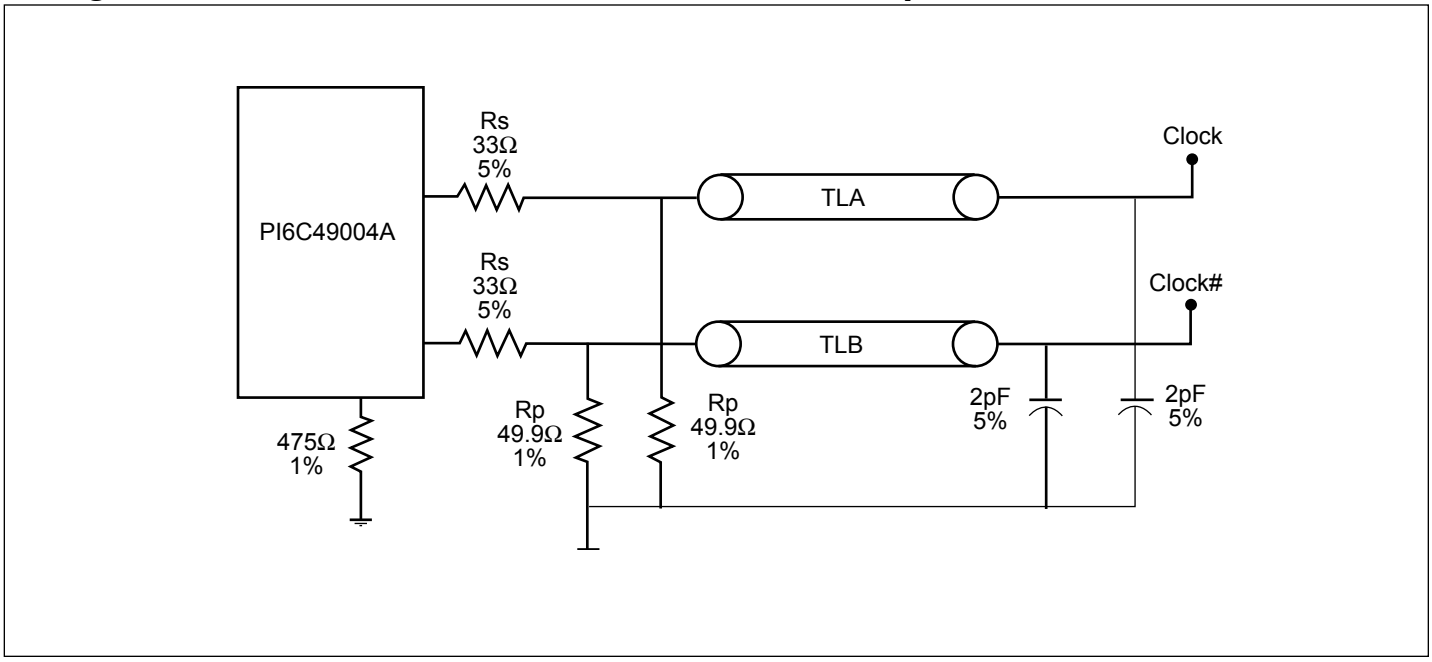
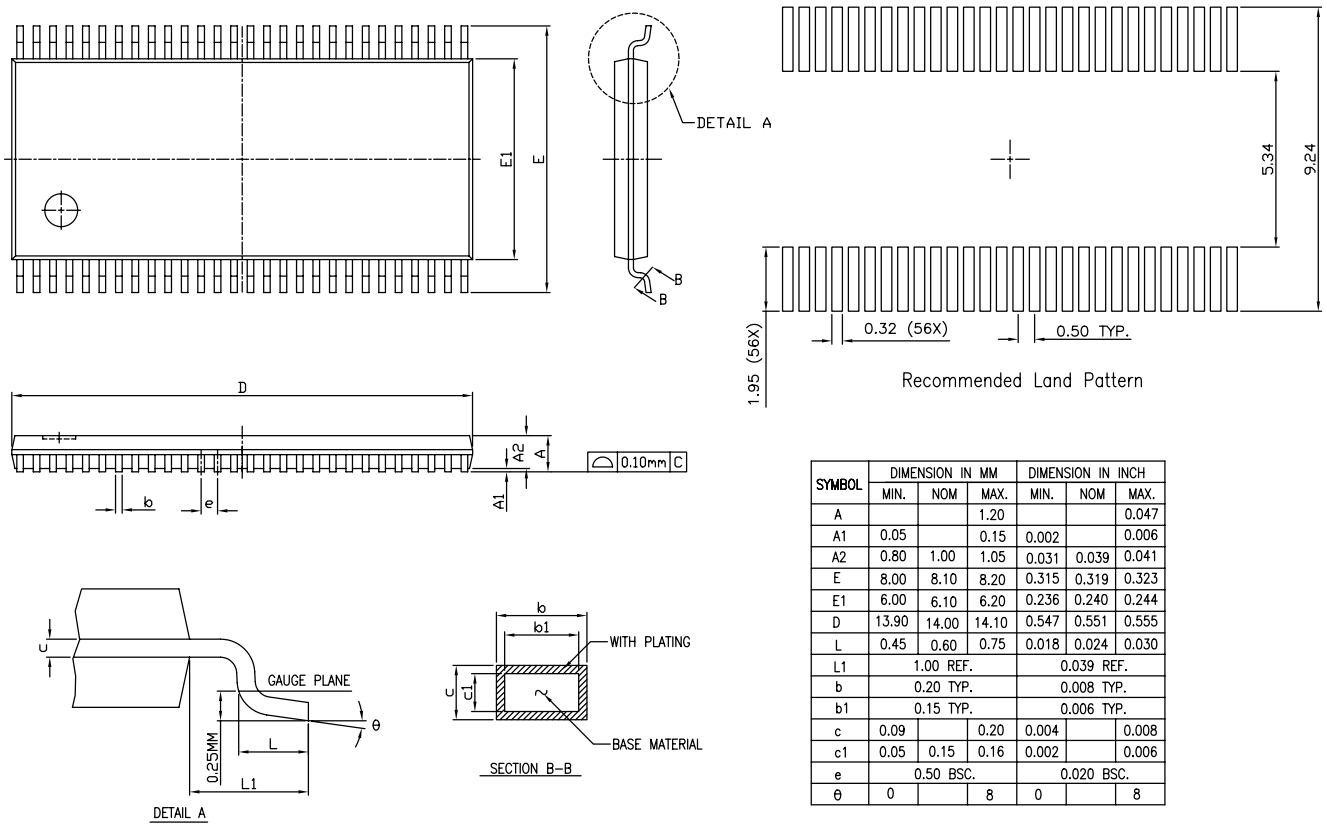


Figure 4. Configuration Test Load Board Termination



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
D	13.90	14.00	14.10	0.547	0.551	0.555
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	0.20 TYP.			0.008 TYP.		
b1	0.15 TYP.			0.006 TYP.		
c	0.09		0.20	0.004		0.008
c1	0.05	0.15	0.16	0.002		0.006
e	0.50 BSC.			0.020 BSC.		
θ	0		8	0		8

PERICOM Semiconductor Corporation

DATE: 09/11/06

DESCRIPTION: 56-pin, 240-mil wide TSSOP

PACKAGE CODE: A56

DOCUMENT CONTROL #: PD-1502 REVISION: M

Notes:
1. Controlling dimensions in millimeters.
2. Ref: JEDEC MO-153F/EE
3. Package Outline Exclusive of Mold Flash and Metal Burr

06-0736

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C49004AAE	A	56-pin, Pb-free & Green, TSSOP, (A56)

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel