Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PI6C49006

Embedded Clock Generator

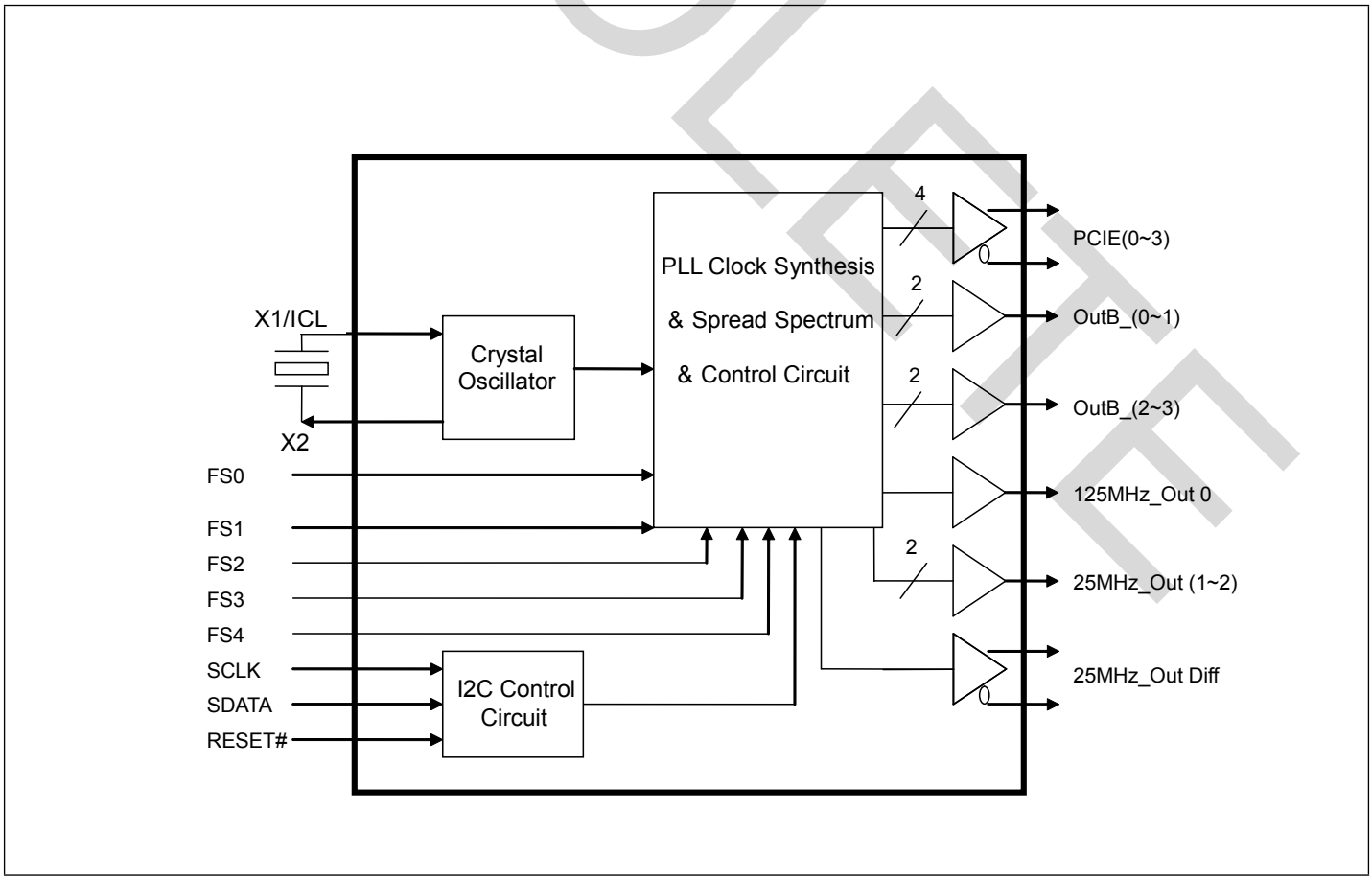
Features

- 3.3V supply voltage
- 25MHz XTAL or reference clock input
- Output
  - 4 x PCIe 2.0 100MHz/125MHz clock with spread spectrum support
  - (2+2) x selectable 33/50/66/100/133MHz LVCMOS clock with ±10% frequency margin
  - 1 x 125MHz LVCMOS clock
  - 2 x 25MHz LVCMOS clock
  - 1 x 25MHz Differential clock (HCSL type)
- Packaging (Pb free and Green)
  - 48-pin TSSOP (A)

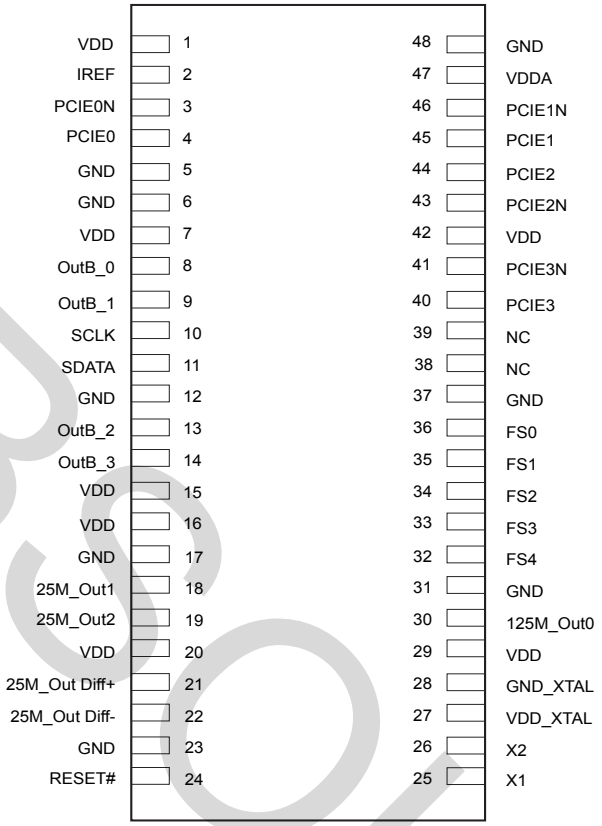
Description

The new PI6C49006 is a high performance clock generator intended for all kinds of embedded applications, which include Wireless AP & Femtocell BTS, Multi Function Printer, and other PCIe/Networking applications. It is the most cost effective way to generate a high quality, high frequency clock output from a crystal and reference clock. The device can generate 100/125MHz HCSL outputs for PCIe, selectable 33/50/66/100/133 LVMOS clock for network processor and DSP and 25MHz Ethernet clock combination.

Block Diagram



Pin Description



Pin List

Pin#	Pin Name	Pin Type	Pin Description
1	VDD	Power	3.3V Supply Pin
2	IREF	Output	Connect to 475 ohm resistor to set HCSL output drive current
3	PCIE0N	Output	100/125MHz HCSL output
4	PCIE0	Output	100/125MHz HCSL output
5	GND	Power	Ground
6	GND	Power	Ground
7	VDD	Power	3.3V Supply Pin
8	OutB_0	Output	33/50/66 MHz selectable LVCMOS output
9	OutB_1	Output	33/50/66MHz selectable LVCMOS output
10	SCLK	Input	I2C compatible clock
11	SDATA	Input	I2C compatible data
12	GND	Power	Ground
13	OutB_2	Output	50/66/100/133 MHz selectable LVCMOS output
14	OutB_3	Output	50/66/100/133 MHz selectable LVCMOS output
15	VDD	Power	3.3V Supply Pin

Pin List

Pin#	Pin Name	Pin Type	Pin Description
16	VDD	Power	3.3V Supply Pin
17	GND	Power	Ground
18	25M_Out1	Output	25.MHz LVCMOS output
19	25M_Out2	Output	25MHz LVCMOS output
20	VDD	Power	3.3V Supply Pin
21	25M_Out Diff+	Output	25MHz HCSL output, follow matching circuit in Figure 4
22	25M_Out Diff-	Output	25MHz HCSL output, follow matching circuit in Figure 4
23	GND	Power	Ground
24	RESET#	Input	Power down reset - When low all PLLs are powered down and outputs tristated. SMBus registers are reset to default values
25	X1	Input	Crystal input. Integrated 6pF capacitance
26	X2	Output	Crystal output. Integrated 6pF capacitance
27	VDD_XTAL	Power	3.3V Supply Pin for XTAL
28	GND_XTAL	Power	Ground for XTAL
29	VDD	Power	3.3V Supply Pin
30	125M_Out0	Output	125MHz LVCMOS output
31	GND	Power	Ground
32	FS4	Input	Frequency select pin for Bank C 25/125MHz LVCMOS output
33	FS3	Input	Frequency select pin for Bank B 33/50/66/100/133MHz LVCMOS output
34	FS2	Input	Frequency select pin for Bank B 33/50/66/100/133MHz LVCMOS output
35	FS1	Input	Frequency select pin for Bank B 33/50/66/100/133MHz LVCMOS output
36	FS0	Input	Frequency select pin for Bank A 100/125MHz HCSL output
37	GND	Power	Ground
38	NC	-	Do Not Connect
39	NC	-	Do Not Connect
40	PCIE3	Output	100/125MHz HCSL output
41	PCIE3N	Output	100/125MHz HCSL output
42	VDD	Power	3.3V Supply Pin
43	PCIE2N	Output	100/125MHz HCSL output
44	PCIE2	Output	100/125MHz HCSL output
45	PCIE1	Output	100/125MHz HCSL output
46	PCIE1N	Output	100/125MHz HCSL output
47	VDDA	Power	Analog Power Supply Pin. See Application Circuit in Figure 5
48	GND	Power	Ground

Selection Table 1 – 100MHz/125MHz PCIe clock in bank A

FS0	PCIE(0~3)
0	100MHz
1	125MHz

Selection Table 2 – Spread Spectrum

SS1	SS0	SSC
0	0	No spread
0	1	Down -0.75%
1	0	Down -0.5%
1	1	No spread

Selection Table 3 – 33/50/66/100/133MHz LVCMOS clock in bank B

FS1	FS2	FS3	OutB_0/1	OutB_2/3
0	0	0	1. Output disable in hardware control mode, internal pull-down 2. Output = 50MHz in software control mode	1. Output disable in hardware control mode, internal pull-down 2. Output = 133MHz in software control mode
0	0	1	33M	66M
0	1	0	50M	100M
0	1	1	66M	133M
1	0	0	33M	50M
1	0	1	33M	100M
1	1	0	66M	50M
1	1	1	66M	100M

Selection Table 4 – 25/125MHz LVCMOS/25MHz Diff clock in bank C

FS4	125M_Out0	25M_Out1	25M_Out2	25M_Out Diff
0	Output disable, internal pull-down	25MHz	25MHz	Output disable, internal pull-down
1	125MHz	25MHz	25MHz	Output disable, internal pull-down
NC	Output disable, internal pull-down	Output disable, internal pull-down	Output disable, internal pull-down	25MHz Diff

OutB_1 Frequency Margining Table

FM3	FM2	FM1	FM0	OutB_(2~3)
0	0	0	0	nominal
0	0	0	1	nominal + 1%
0	0	1	0	nominal + 2%
0	0	1	1	nominal + 3%
0	1	0	0	nominal + 4%
0	1	0	1	nominal + 5%
0	1	1	0	nominal + 6%
0	1	1	1	nominal + 8%
1	0	0	0	nominal + 10%
1	0	0	1	nominal - 1%
1	0	1	0	nominal - 2%
1	0	1	1	nominal - 3%
1	1	0	0	nominal - 4%
1	1	0	1	nominal - 6%
1	1	1	0	nominal - 8%
1	1	1	1	nominal - 10%

Serial Data Interface (SMBus)

PI6C49006 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	D2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting databyte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for OutB_2	RW	1	50/66/100/133 MHz selectable LVCMOS output	0 = disabled 1 = enabled
6	Enables hardware or software control of OE bits (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	0	RESET# pin, bit 5	0 = hardware cntl 1 = software ctrl
5	Software RESET# bit. Enables or disables all outputs (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4	Frequency margining select bit FM3	RW	1	OutB_2,3	See OutB_2,3 Frequency Margining Table on Page 5
3	Frequency margining select bit FM2	RW	0		
2	Frequency margining select bit FM1	RW	1		
1	Frequency margining select bit FM0	RW	0		
0	OE for OutB_3	RW	1	50/66/100/133 MHz selectable LVCMOS output	0 = disabled 1 = enabled

Byte 0 - Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	(RESET# = "H" will enable all outputs; SMBus cannot control each output.)
1	0	Disables all outputs and tri-states the outputs, RESET# HW pin/signal = DO NOT CARE
1	1	Enable outputs according to the SMBus default values; SMBus can control each output. RESET# HW pin/signal, FS1, FS2, FS3 and FS4 = DON'T CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 25M_Out Diff	RW	1	25M_Out Diff	0 = disabled 1 = enabled
6	OE for 25M_Out2	RW	1	25M_Out2	0 = disabled 1 = enabled
5	OE for 25M_Out1	RW	1	25M_Out1	0 = disabled 1 = enabled
4	OE for 125_Out0	RW	1	125_Out0	0 = disabled 1 = enabled
3	OE for OutB_1	RW	1	OutB_1	0 = disabled 1 = enabled
2	OE for OutB_0	RW	1	OutB_0	0 = disabled 1 = enabled
1	Spread Spectrum Selection for 100MHz HCSL PCI Express clocks Bit 1: SS1, Bit 0:SS0	RW	0	All 100MHz HCSL PCI Express outputs	See Selection Table 2 - Spread Spectrum
0		RW	0		

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved	RW	Undefined	Not Applicable	
6	Reserved	RW	1	Not Applicable	
5	Reserved	RW	1	Not Applicable	
4	OE for 100M_Out3 HCSL Output	RW	1	100M_Out3	0 = disabled 1 = enabled
3	OE for 100M_Out2 HCSL Output	RW	1	100M_Out2	0 = disabled 1 = enabled
2	OE for 100M_Out1 HCSL Output	RW	1	100M_Out1	0 = disabled 1 = enabled
1	OE for 100M_Out0 HCSL Output	RW	1	100M_Out0	0 = disabled 1 = enabled
0	Reserved	R	Undefined	Not Applicable	

Byte 4 & 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revivsion ID bit 3	R	0	Not Applicable	
6	Revivsion ID bit 2	R	0	Not Applicable	
5	Revivsion ID bit 1	R	0	Not Applicable	
4	Revivsion ID bit 0	R	0	Not Applicable	
3	Vendor ID bit 3	R	0	Not Applicable	
2	Vendor ID bit 2	R	0	Not Applicable	
1	Vendor ID bit 1	R	1	Not Applicable	
0	Vendor ID bit 0	R	1	Not Applicable	

Recommended Operation Conditions[1] (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	V
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, V_{DD} 7V
All Inputs and Outputs ..... –0.5V to V_{DD} +0.5V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... 125°C
Peak Soldering Temperature ..... 260°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±5%, Ambient Temperature 0°C to +70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Supply Voltage	V_{DD}		3.135		3.465	V
Analog Supply Voltage	V_{DDA}		3.135		3.465	
Input High Voltage	V_{IH}		2		V_{DD}	
Input Low Voltage	V_{IL}		–0.3		0.8	
Input High Voltage	V_{IH}	SDATA, SCLK, FS4	$0.7V_{DD}$		V_{DD}	
Input Low Voltage	V_{IL}	SDATA, SCLK, FS4			$0.3V_{DD}$	
Operating Supply Current	I_{DD}			197	230	mA
IDD at Output Disable Condition		RESET# = 0		4.3		
Internal Pull-Up/Pull-Down Resistor	R_{PU}/R_{PD}	RESET#		216		k–Ohm
		All single-ended outputs		75		
Input Capacitance	C_{IN}	All input pins		6		pF
Pin FS4 External Pull-Up/Pull-Down Resistor	R_{FS4Ext}				470	Ohm

Electrical Characteristics - Single-Ended

Unless otherwise specified, V_{DD}=3.3V±5%, Ambient Temperature 0°C to +70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Frequency	F_{IN}			25		MHz
SCLK Frequency				100	400	kHz
Minimum Pulse Width of RESET# Input			100			ns
Output Frequency Error		FM0, FM3 = 0		0		ppm
Output Rise/Fall Time	t_r, t_f	20% to 80%		1	2	ns
Output Clock Duty Cycle		Measured at $V_{DD}/2$	45	50	57	%
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	VDD-0.4			
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	
Peak-to-Peak Jitter		125MHz clock output		140	200	ps
		33/50/66/100/133MHz clock output		125	175	
		25MHz clock output		115	150	
Cycle-to-Cycle Jitter		125MHz clock output		120	175	
		33/50/66/100/133MHz clock output		120	160	
		25MHz clock output		120	160	
Clock Stabilization Time from Power Up			3		10	ms

Electrical Characteristics - 100MHz Differential HCSL Outputs

Unless otherwise specified, V_{DD}=3.3V±5%, Ambient Temperature 0°C to +70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency					100	MHz
Cycle-to-Cycle Jitter	$T_{CC/Jitter}$				150	ps
Peak-to-Peak Phase Jitter		Using PCIe jitter measurement method			86	
PCIe 2.0 RMS Phase Jitter	$J_{RMS2.0}$	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
Spread Modulation Percentage				-0.5	0	%
Spread Modulation Frequency				32		kHz
Duty Cycle	T_{DC}		45	50	55	%
SE Rise/Fall Time Measured from 0.175V to 0.525V	T_{or}, T_{of}	1. R_L=50-Ohm with C_L = 2pF 2. Single-ended waveform	175		700	ps
Output Skew	T_{OSKEW}	V_T = 50%(measurement threshold)			200	ps
High-Level Output Voltage	V_{OH}	Note 2, (R_S=33-Ohm, R_T=50-Ohm)	0.65	0.71	0.95	V
Low-Level Output Voltage	V_{OL}		–0.20	0	0.05	
I_{OH} @ 6*I_{REF}	I_{OH}		–13	–14.2	–19	mA
Absolute Crossing Point Voltage	V_{CROSS}	Note 2, 5, 6	0.25		0.55	V
Variation of VCROSS over all rising clock edges	$V_{CROSS\ Delta}$	Note 2, 5, 8			140	mV
Average Clock Period Accuracy	$T_{PERIOD\ AVG}$	Note 3, 9, 10	–300		2800	ppm
Absolute Period (including jitter and spread spectrum)	$T_{PERIOD\ ABS}$	Note 3, 7	9.847		10.203	ns

Notes:

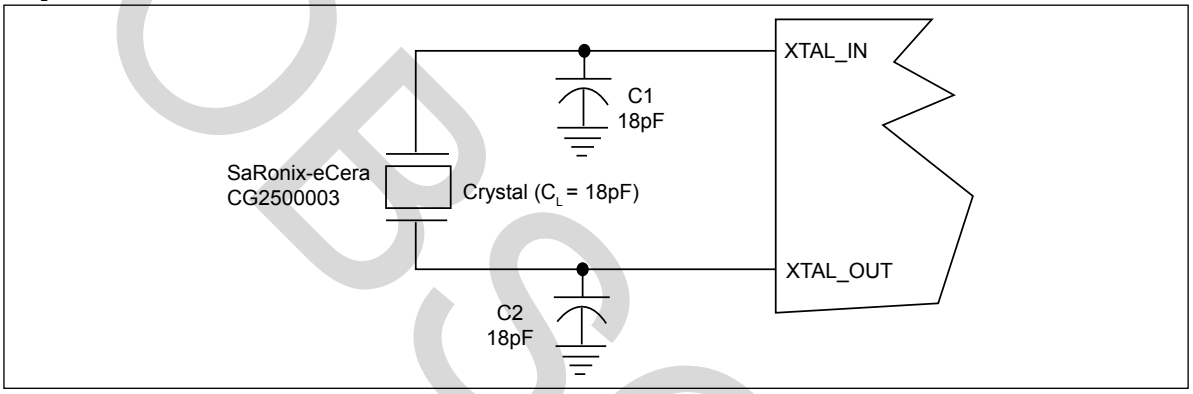
1. Measured at the end of an 8-inch trace with a 5pF load.
2. Measurement taken from a single-ended waveform.
3. Measurement taken from a differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
5. Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M–.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
7. Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
8. Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M–.
9. Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.
10. 10) PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 PPM there is an error budget of 100Hz/PPM * 300 PPM = 30 kHz. The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than ±300 ppm. With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.

Application Notes

Crystal circuit connection

The following diagram shows PI6C49006 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 18pF, C2= 18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



Recommended Crystal Specification

Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Configuration test load board termination for HCSL Outputs

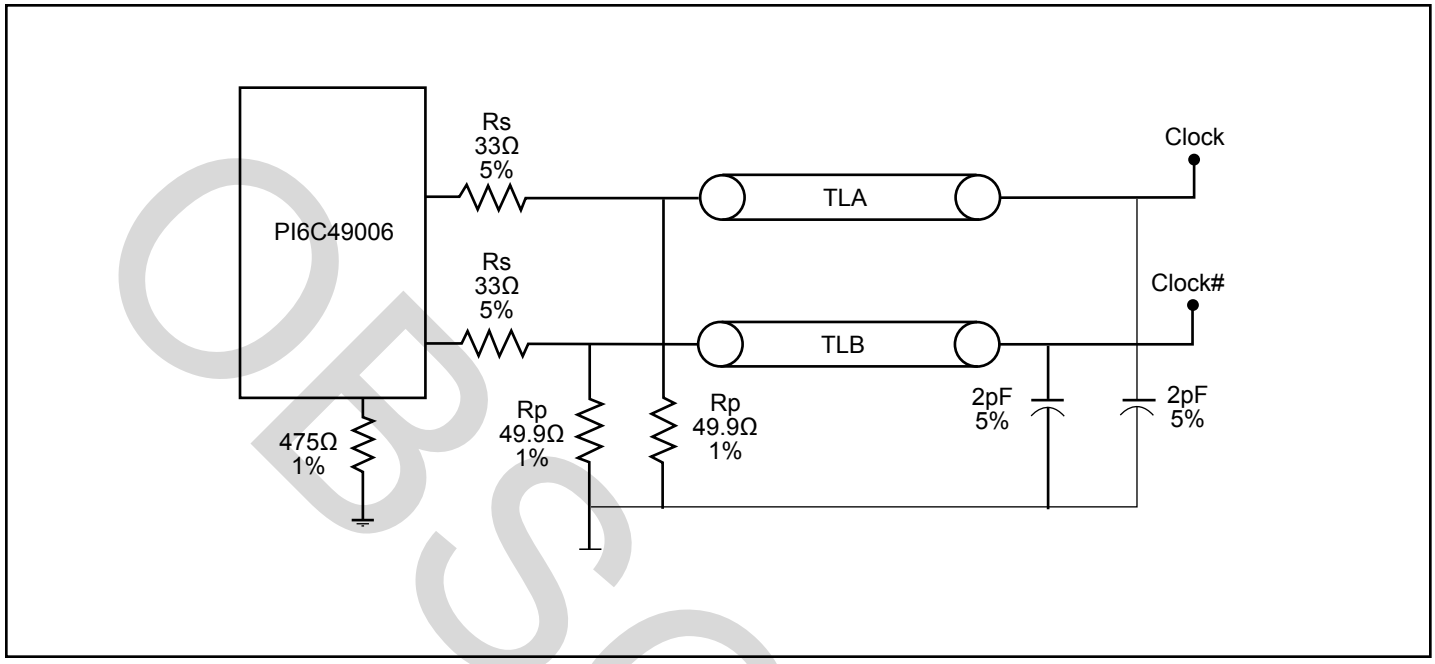


Figure 4. Configuration Test Load Board Termination

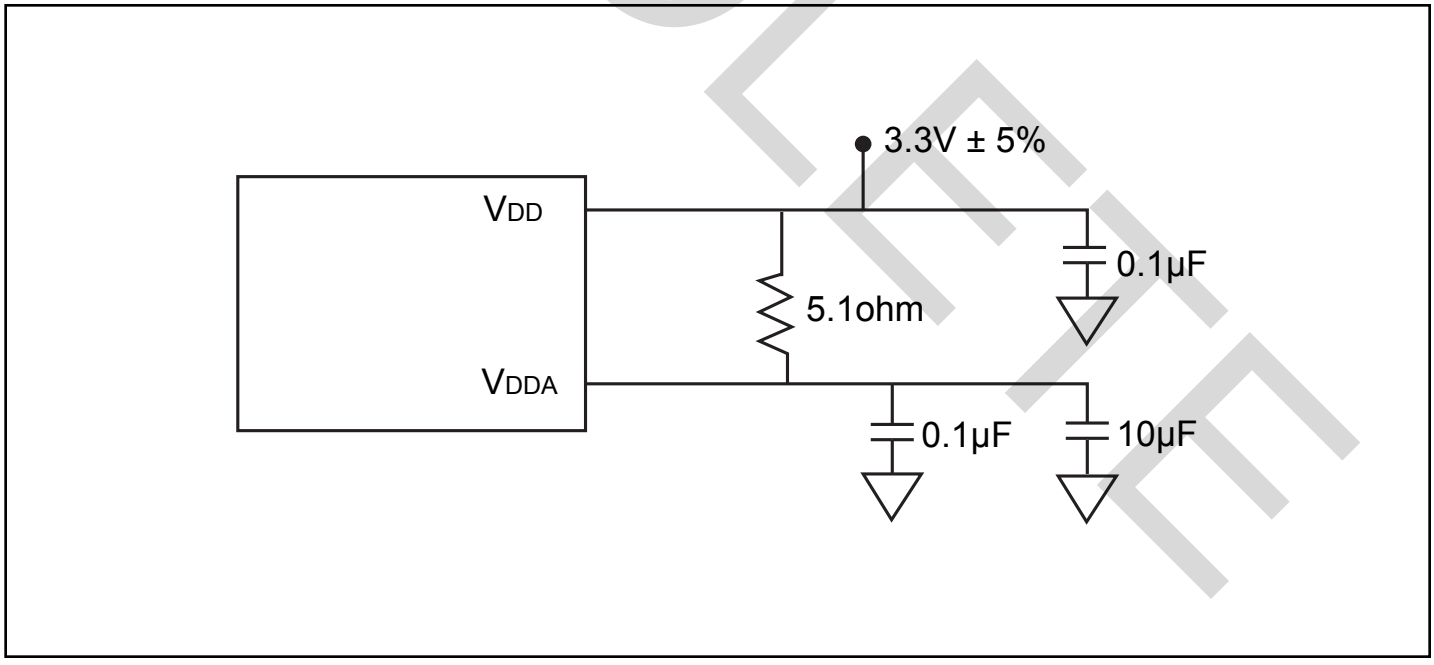
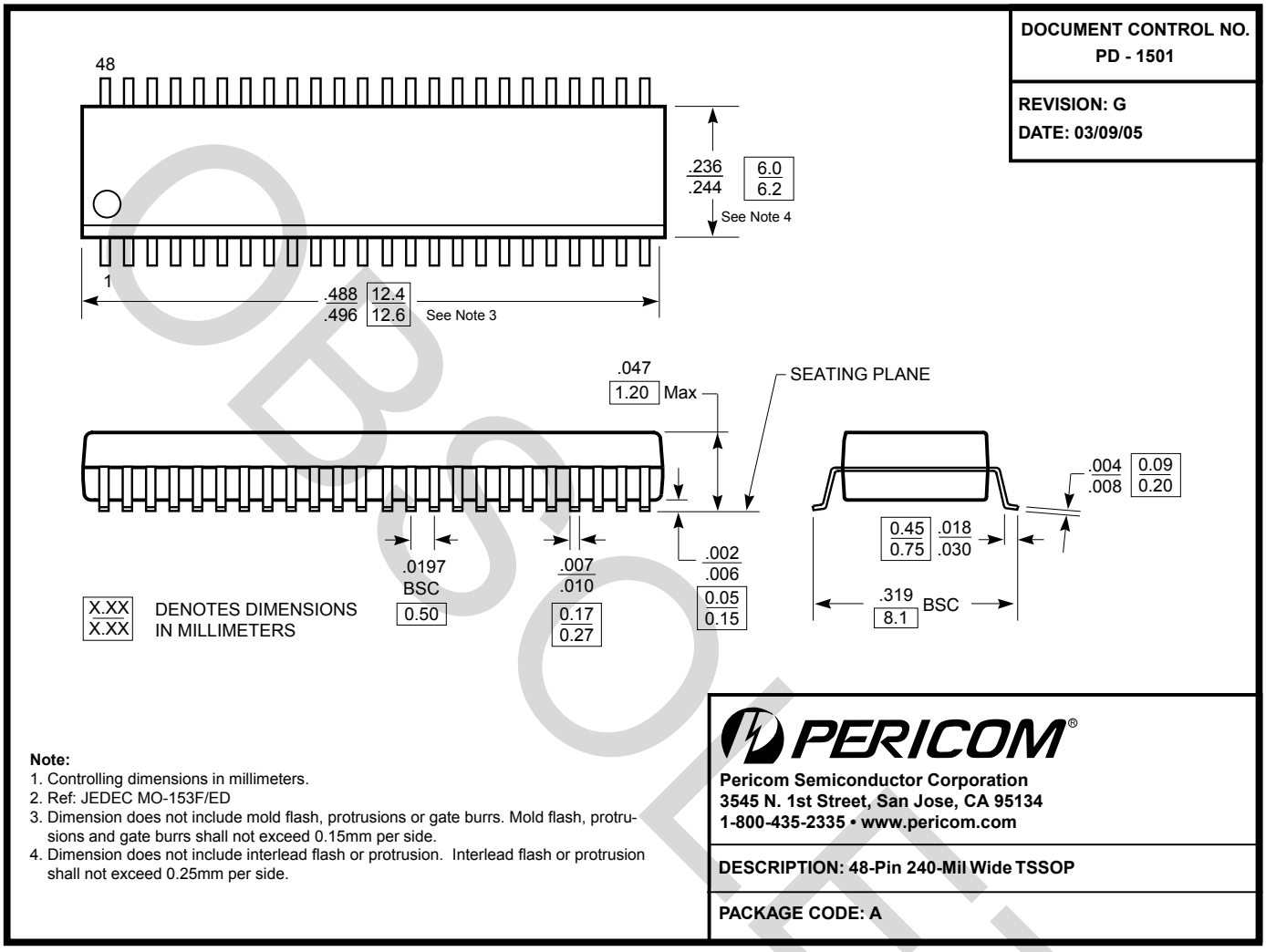


Figure 5. Power Supply Filter



Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information[1-3]

Ordering Code	Package Code	Package Description
PI6C49006AE	A	48-pin, Pb-free & Green, TSSOP, (A48)

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel