Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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PERICOM®

PI6C490086

PLL Clock Multiplier

Features

→ Support XTAL or Clock input at 25MHz

→ Three buffered outputs support V_{DD} operation

→ One 8.192 MHz output

→ Very low phase jitter(RMS), 25MHz : < 2ps

→ Very low additive jitter: <500fs (typ)

→ 3.3V supply voltage for Core

→ 1.8V ~ 3.3V supply voltage for two outputs

→ Packaging: 16-pin TSSOP

→ Commercial & Industrial Temperature support

Applications

→ Networking Systems

→ Femtocell BTS

→ Peripheral

Description

The PI6C490086 is a low jitter clock generator supporting either XTAL or reference input. Two of its buffered outputs can support wide operating voltage from 1.8V to 3.3V. It is a cost effective way to generate multiple outputs for all kinds of applications that need 25MHz with different power supplies and a 8.192 MHz clock signal.

Block Diagram
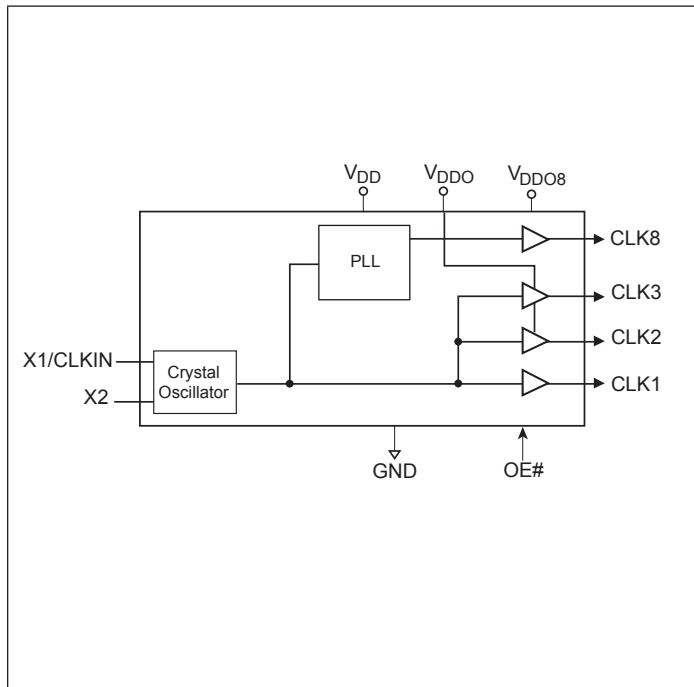
Pin Configuration (16-Pin TSSOP)

16-pin (173 mil) TSSOP
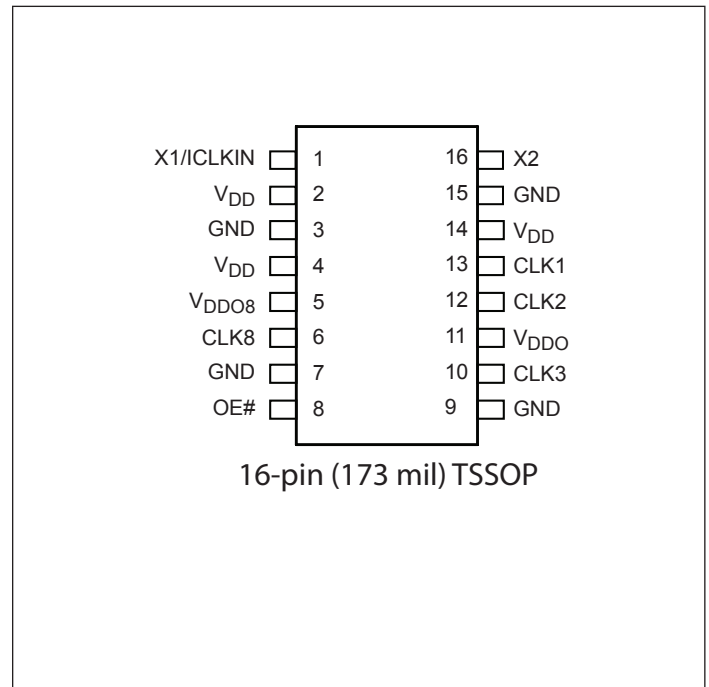
Pin number	Pin Name	Type	Description
1	X1/CLKIN	Input	Crystal connection or clock input
2, 4, 14	V_{DD}	Power	3.3V Core and CLK1 supply voltage
5	V_{DDO8}	Power	Supply voltage for CLK8
6	CLK8	Output	8.192 MHz output
7, 9, 15	GND	Power	Connect to Ground
8	OE#	Input	Global output enable when low. Internal pull-down resistor.
10	CLK3	Output	Clock Output 3
11	V_{DDO}	Power	Supply voltage from 1.8V to 3.3V for CLK2 and CLK3
12	CLK2	Output	Clock Output 2
13	CLK1	Output	Clock Output 1
16	X2	Output	Crystal connection

Function Table

OE#	CLK1/CLK2/CLK3/CLK8
0	Enabled
1	Hi-Z, weak pull down

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.. −65°C to +150°C

Supply Voltage to Ground Potential, V_{DD} ....−0.5V to +4.6V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Requirements (Over operating free-air temperature range)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
V_{DDO}, V_{DDO8}	Power Supply Voltage for outputs	1.71		3.465	V
I_{DD}	Power supply current, no load		20		mA
T_A	Ambient Operating Temperature	0		+70	°C
		-40		+85	
t_{UP}	Power Supply Ramp Time			4	ms

DC Electrical Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	CLKIN, OE#		$V_{DD}/2+1$			V
V_{IL}	Input Low Voltage	CLKIN, OE#				$V_{DD}/2-1$	V
V_{OH}	Output High Voltage	I_{OH} = -4mA and -8mA	8MHz output	$V_{DDo8} - 0.4$			V
			25MHz output	$V_{DDo} - 0.4$			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA and 8mA				0.4	V
Z_O	Nominal Output Impedance				20		Ω
R_{PD}	Internal Pull-down Resistor	OE#			200		kΩ
		CLKIN			230		
C_{IN}	Input Capacitance	Inputs			4		pF

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Input Frequency	Fundamental Crystal		25		MHz
		Input Clock		25		
t_R	Output Rise Time	20% to 80% 25MHz, Note 1		1		ns
t_F	Output Fall Time	80% to 20% 25MHz, Note 1		1		
t_R	Output Rise Time	20% to 80% 8.192MHz, Note 1		2		
t_F	Output Fall Time	80% to 20% 8.192MHz, Note 1		2		
t_{DC}	Duty Cycle	Note 2		50	53	%
F_{error}	Output Frequency Synthesis Error			0		ppm
J_{phase}	Clock Phase Jitter (RMS)	25MHz only, Note 2		0.5	1.5	ps
J_{add}	Additive Jitter	25MHz, Note 3		500		fs
J_{add}	Absolute Period Jitter (pk-pk)	8.192MHz		+/-100		ps

1. Note 1: Measured with 7 pF lump load.

2. Note 2: 12 kHz to 20 MHz offset frequency using a crystal input.

3. Note 3: CLKIN input with X2 floating.

4. Note 4: Do not drive this device without a crystal or valid clock input
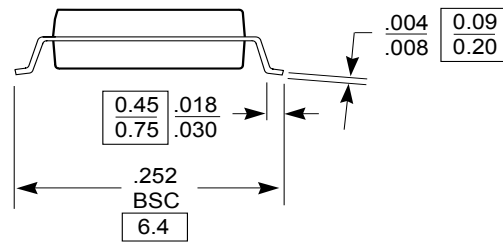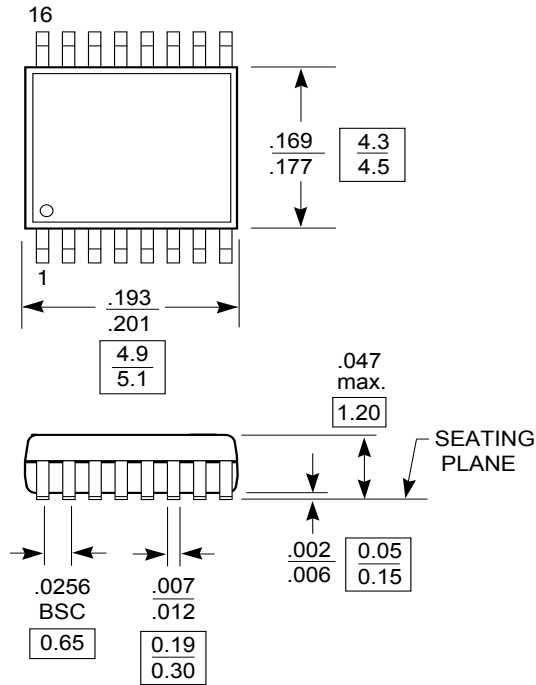
Crystal Oscillator Circuit
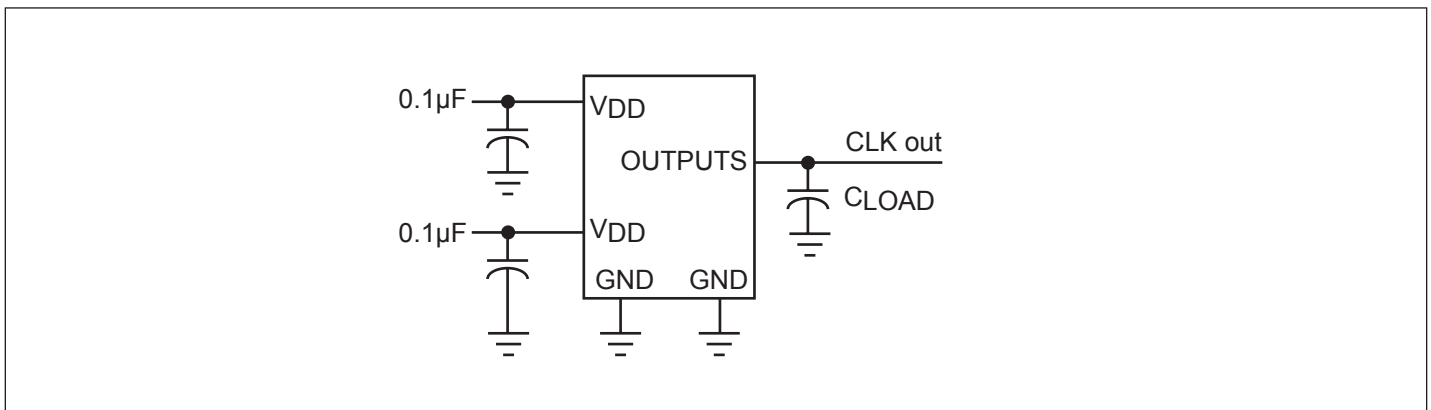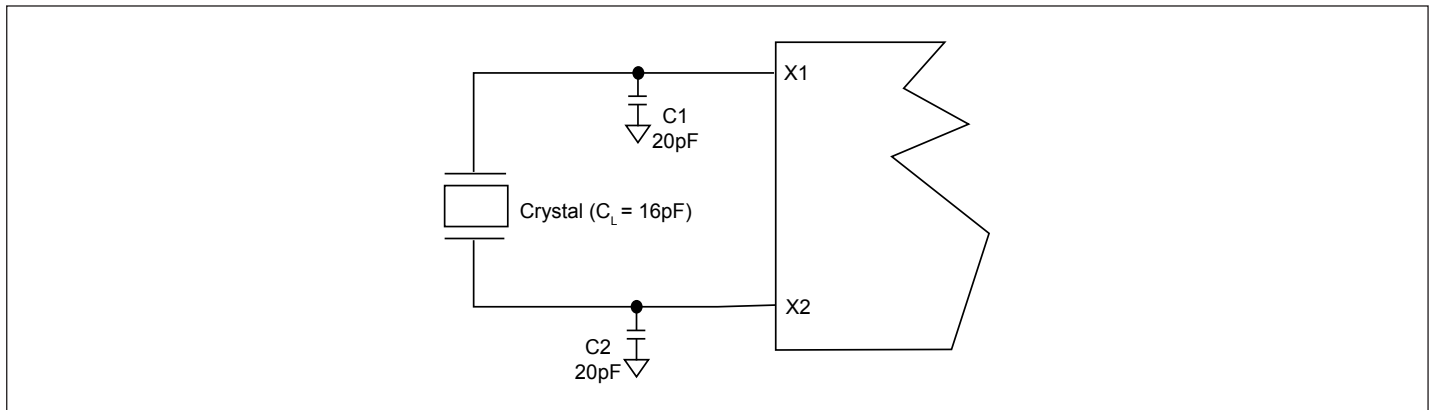
CMOS Test Configuration

Packaging Mechanical: 16-Pin TSSOP (L)

	DOCUMENT CONTROL NO. PD - 1310
	REVISION: E DATE: 03/09/05

.169 / .177 → 4.3 / 4.5

16

1

.193 / .201 → 4.9 / 5.1

.047 max. → 1.20

SEATING PLANE

.0256 BSC → 0.65

.007 / .012 → 0.19 / 0.30

.002 / .006 → 0.05 / 0.15

.004 / .008 → 0.09 / 0.20

0.45 / 0.75 ← .018 / .030

.252 BSC → 6.4

Note:
1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimentions in millimeters
3. Ref: JEDEC MO-153F/AB

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 16-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C490086LE	L	Pb-free & Green, 16-pin TSSOP	Commercial
PI6C490086LIE	L	Pb-free & Green, 16-pin TSSOP	Industrial

Notes:

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• E = Pb-free and Green

• X suffix = Tape/Reel