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Low Power Networking Clock Generator

Features

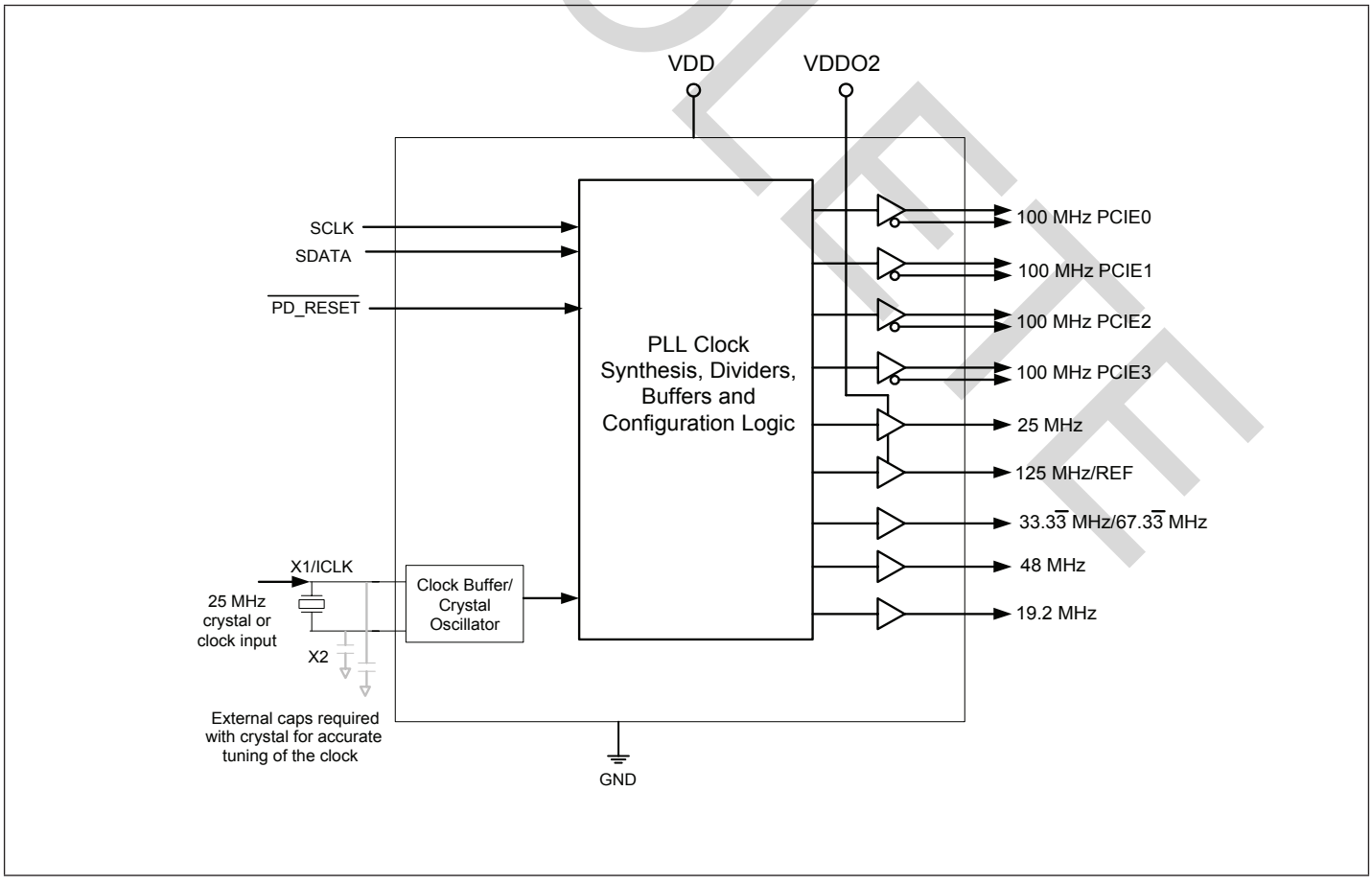
- 3.3V supply voltage
- 25MHz XTAL or reference clock input
- Output
  - 4x100MHz HCSL PCIe clock outputs with integrated series termination resistors, spread spectrum capability on all 100MHz PCIe clock outputs with -0.5% down spread.
  - 1x single-ended 33.33MHz or 67.33MHz output with spread spectrum capability
  - 1x single-ended 125MHz output for Gigabit Ethernet
  - 1x single-ended 25MHz
  - 1x single-ended 48MHz
  - 1x single-ended 19.2MHz
- Packaging (Pb free and Green) : 48-pin TSSOP (A)
- Industrial temperature support

Description

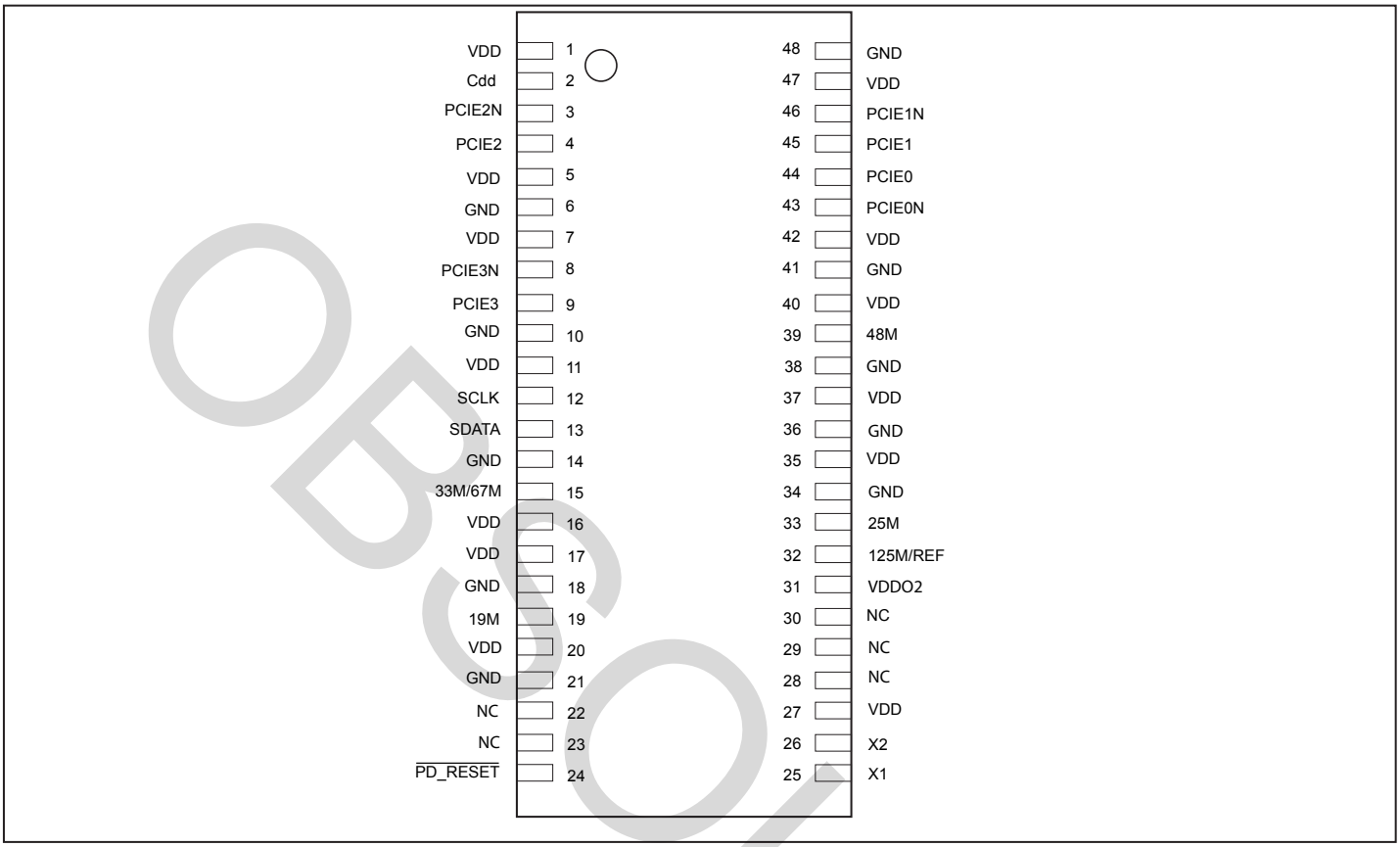
The new PI6C49019 is a high integration clock generator intended for all kinds of embedded applications and networking application with PCIe interface. The device is the most cost effective way to generate multi-frequencies and multi-outputs clocks from a 25MHz crystal and reference clock. The device can generate four pairs low power 100MHz HCSL outputs for PCIe, one single-ended 25MHz and 125 MHz output, one single-ended 48MHz and 19.2 MHz output, and one single-ended 33.33 MHz or 67.33MHz output with spread spectrum.

Using a serially programmable SMBus interface, the PI6C49019 incorporates spread spectrum modulation on the four 100 MHz PCI-Express outputs with -0.5% down spread and the 33.33 MHz/67.33 MHz output with down spread.

Block Diagram



Pin Description



Pin List

Pin#	Pin Name	Pin Type	Pin Description
1	VDD	Power	3.3V Supply Pin
2	Cdd	Input	Input pin for off chip bypass capacitor. Connect to 0.01 µF capacitor
3	PCIE2N	Output	Differential 100 MHz HCSL PCI Express Clock output
4	PCIE2	Output	Differential 100 MHz HCSL PCI Express Clock output
5	VDD	Power	3.3V Supply Pin
6	GND	Power	Ground
7	VDD	Power	3.3V Supply Pin
8	PCIE3N	Output	Differential 100 MHz HCSL PCI Express Clock output
9	PCIE3	Output	Differential 100 MHz HCSL PCI Express Clock output
10	GND	Power	Ground
11	VDD	Power	3.3V Supply Pin
12	SCLK	Input	SMBus clock input
13	SDATA	I/O	SMBus data input
14	GND	Power	Ground
15	33M/67M	Output	33.33 MHz or 67.33 MHz LVCMOS output. Tri-stated with a weak pull-down when disabled.

Pin List

Pin#	Pin Name	Pin Type	Pin Description
16	VDD	Power	3.3V Supply Pin
17	VDD	Power	3.3V Supply Pin
18	GND	Power	Ground
19	19M	Output	19.2 MHz LVCMOS output. Tri-state with weak pull-down when disabled
20	VDD	Power	3.3V Supply Pin
21	GND	Power	Ground
22	NC	-	-
23	NC	-	-
24	$\overline{\text{PD\_RESET}}$	Input	Global reset input powers down PLLs plus tri-states outputs and sets the I2C tables to their default state when pulled low. Controlled by external POR.
25	X1	XI	Crystal input. Connect to 25 MHz fundamental mode crystal or clock
26	X2	XO	Crystal output. Connect to 25 MHz fundamental mode crystal. Float for clock input
27	VDD	Power	3.3V Supply Pin
28	NC	-	-
29	NC	-	-
30	NC	-	-
31	VDDO2	Power	125 MHz output supply voltage. Connect to +2.5 V
32	125M/REF	Output	125 MHz or 25 MHz reference +2.5 V LVCMOS output. Tri-stated with a weak pull-down when disabled
33	25M	Output	25 MHz +2.5 LVCMOS output. Tri-stated with a weak pull-down when disabled
34	GND	Power	Ground
35	VDD	Power	3.3V Supply Pin
36	GND	Power	Ground
37	VDD	Power	3.3V Supply Pin
38	GND	Power	Ground
39	48M	Output	48 MHz LVCMOS output. Tri-state with weak pull-down when disabled
40	VDD	Power	3.3V Supply Pin
41	GND	Power	Ground
42	VDD	Power	3.3V Supply Pin
43	PCIE0N	Output	Differential 100 MHz HCSL PCI Express Clock output
44	PCIE0	Output	Differential 100 MHz HCSL PCI Express Clock output
45	PCIE1	Output	Differential 100 MHz HCSL PCI Express Clock output
46	PCIE1N	Output	Differential 100 MHz HCSL PCI Express Clock output
47	VDD	Power	3.3V Supply Pin
48	GND	Power	Ground

Notes: VDD and GND Pins Layout Guide

1. Small value decoupling caps. (0.1uF, 1uF, and 2.2uF) should be placed close each VDD pin or its via

2. Connect all GND pins to package thermal pad which must be connected to the GND plane for better thermal distribution and signal conducting with reasonable via count (>8)

Selection Table 1 – 33M/67M Spread Spectrum

SS1	SS0	SSC
0	0	No spread
0	1	Down -0.5%
1	0	Down -0.75%
1	1	Down -1.00%

Selection Table 2 – 125 MHz / 25 MHz Frequency Selection Table

SEL	Output
0	REF
1	125 MHz

Serial Data Interface (SMBus)

PI6C49019 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	D2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting databyte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Select for 100MHz HCSL PCI-Express clocks	RW	0	All 100MHz HCSL PCI-Express outputs	0=spread off 1=-0.5% down
6	Enables hardware or software control of OE bits (see Byte 0-Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{\text{PD\_RESET}}$, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{\text{PD\_RESET}}$ bit. Enables or disables all outputs. (see Byte 0-Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4	Spread Select for 33.33/67.33 MHz S1	RW	0	33MHz LVCMOS output pin 15	See Table1 on Page4
3	Spread Select for 33.33/67.33 MHz Page 4 S0	RW	0		
2	OE for single-ended 25 MHz	RW	1	25M	0 = disabled 1 = enabled
1	Frequency Select Bit	RW	1	125M/REF	0 = REF 1 = 125M
0	OE for single-ended 125 MHz/REF	RW	1	Single-ended 125MHz/REF pin 30	0 = disabled 1 = enabled

Byte 0: Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	($\overline{\text{PD\_RESET}}$= "H" will enable all outputs; SMBus cannot control each output.)
1	0	Disables all outputs and tri-states the outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE
1	1	Enable outputs according to the SMBus default values; SMBus can control each output. $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 33.33/67.33 MHz output	RW	1	33/67M	1 = enabled 0 = disabled
6	33.33/67.33 MHz Select	RW	0	33/67M	0 = 67.33 MHz 1 = 33.33 MHz
5 to 0	Reserved	R	-	-	-

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	-	-	-

Byte 3: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved	RW	0	-	-
6	OE for 48 MHz output	RW	0	48M	1 = enabled 0 = disabled
5	OE for 100 MHz PCI-Express output PCIE3	RW	1	100MHz HCSL PCI-Express output PCIE3	1 = enabled 0 = disabled
4	OE for 100 MHz PCI-Express output PCIE2	RW	1	100MHz HCSL PCI-Express output PCIE2	1 = enabled 0 = disabled
3	OE for 19.2 MHz output	RW	0	19M	1 = enabled 0 = disabled
2	OE for 100 MHz PCI-Express output PCIE1	RW	1	100MHz HCSL PCI-Express output PCIE1	1 = enabled 0 = disabled
1	OE for 100 MHz PCI-Express output PCIE0	RW	1	100 MHz PCI-Express output PCIE0	1 = enabled 0 = disabled
0	Reserved	R	-	-	-

Byte 4: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	-	-	-

Byte 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	0	-	-
6	Revision ID bit 2	R	0	-	
5	Revision ID bit 1	R	0	-	
4	Revision ID bit 0	R	0	-	
3	Vendor ID bit 3	R	0	-	
2	Vendor ID bit 2	R	0	-	
1	Vendor ID bit 1	R	0	-	
0	Vendor ID bit 0	R	0	-	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	-	-	-

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, V_{DD} 4.6V
All Inputs and Outputs ..... –0.5V to V_{DD} +0.5V
Ambient Operating Temperature ..... –40°C to +85°C
Storage Temperature ..... –65°C to +150°C
ESD Protection (HBM) 2000V

Note:
Stresses above the ratings listed below can cause permanent damage to the PI6C49019. These ratings, which are standard values for Pericom commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Recommended Operation Conditions

Parameters	Min.	Typ.	Max.	Units
Ambient Operating Temperatur	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0	3.3	+3.6	V
Output Supply Voltage, V_{DDO2}	+2.25		+3.6	V
Minimum Pulse Width of $\overline{PD\_RESET}$ Input	100			ns

DC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, V_{DDO2}=2.5V,Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Output Supply Voltage	V_{DDO2}		2.25	2.5	3.6	
Input High Voltage	V_{IH}	X1/SCLK, SDATA, $\overline{PD\_RESET}$	2		V_{DD}	
Input Low Voltage	V_{IL}	X1/SCLK, SDATA, $\overline{PD\_RESET}$	–0.3		0.8	
Operating Supply Current	I_{DD}	No load, all supply pins, $\overline{PD\_RESET}$ = 1		90	115	mA
IDD at Output Disable Condition		$\overline{PD\_RESET}$ = 0		6		
Short Circuit Current	I_{OS}	Single-ended clocks		±35		
Internal Pull-Up/Pull-Down Resistor	R_{PU}/R_{PD}	$\overline{PD\_RESET}$		240		kΩ
		All single-ended clocks		110		
Input Capacitance	C_{IN}	All input pins		6		pF

Electrical Characteristics - Single-Ended

Unless otherwise specified, V_{DD}=3.3V±10%, V_{DDO2}=2.5V, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Frequency	F_{IN}			25		MHz
Output Frequency Error				0		ppm
Output Rise Time	t_{OR}	20% to 80% [1]		0.5	1	ns
		0.7 V to 1.7V 125 MHz[4]			0.4	
Output Fall Time	t_{OF}	80% to 20% [1]		0.5	1.35	
		1.7 V to 0.7V 125 MHz[4]			0.4	
Output Clock Duty Cycle		Measured at $V_{DD/2}$	45	50	55	%
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	VDD-0.4			
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	2.1			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Peak-to-Peak Jitter		33MHz clock output		±150		ps
		125MHz clock output		±100		
Cycle-to-Cycle Jitter		125MHz clock output [1]			±100	
		33/67MHz clock output [1,2]			±100	
Clock Stabilization Time from Power Up		PD_RESET goes high to 1% of final frequency	3		10	ms

Note 1: CL = 15 pF
Note 2: Cycle-to-cycle jitter is measured at 25°C.
Note 3: Spread OFF.
Note 4: CL = 5 pF

Electrical Characteristics - 100 MHz Differential Push-Pull Outputs

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency					100	MHz
Cycle-to-Cycle Jitter	$T_{CC/Jitter}$				150	ps
Peak-to-Peak Phase Jitter		Using fixed-filter clock recovery function			86	
PCIe 2.0 RMS Phase Jitter	$J_{RM52.0}$	PCIe 2.0 Test Method @ 100 MHz Output			3.1	ps
Spread Range				-0.5	0	%
Spread Rate				32		kHz
Duty Cycle	T_{DC}		45	50	55	%
Clock Stabilization from Power Up				3.5		ms
Rising Edge Rate		Note3, 4	0.6		4.0	V/ns
Falling Edge Rate		Note3, 4	0.6		4.0	V/ns
Rise-Fall Matching		Note3, 11		20		%
Output Skew	T_{OSKEW}	V_T = 50%(measurement threshold), Intra-pair skew			50	ps
		V_T = 50%(measurement threshold), Inter-pair skew			200	ps
Clock Source DC Impedance(Zo)	Z_{C-DC}			17		Ω
High-Level Output Voltage	V_{OL}	V_{DD} = 3.3V Note2 (Rs = 33ohm)	0.65	0.71	0.90	V
Low-Level Output Voltage	V_{OH}		-0.20	0	0.05	
Absolute Crossing Point Voltage	V_{CROSS}	Note2, 5, 6	0.25		0.55	V
Variation of V_{CROSS} over all rising clock edges	V_{CROSS} Delta	Note2, 5, 8			140	mV
Average Clock Period Accuracy	T_{PERIOD} AVG	Note3, 9, 10	-300		2800	ppm
Absolute Period (including jitter and spread spectrum)	T_{PERIOD} ABS	Note3, 7	9.847		10.203	ns

Notes:

2. Measurement taken from a single-ended waveform.

3. Measurement taken from a differential waveform.

4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

5. Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M–.

6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

Notes (Continued)

7. Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.

8. Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M–.

9. Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.

10. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 PPM there is an error budget of 100Hz/PPM * 300 PPM = 30 kHz. The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than ±300 ppm. With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.

11. Matching applies to rising edge rate for PCIe and falling edge rate for PCIeN. It is measured using a ±75 mV window centered on the median cross point where PCIe rising meets PCIeN falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rising edge rate of PCIe should be compared to the falling edge rate of PCIeN. The maximum allowed difference should not exceed 20% of the slowest edge rate.

Thermal Characteristics

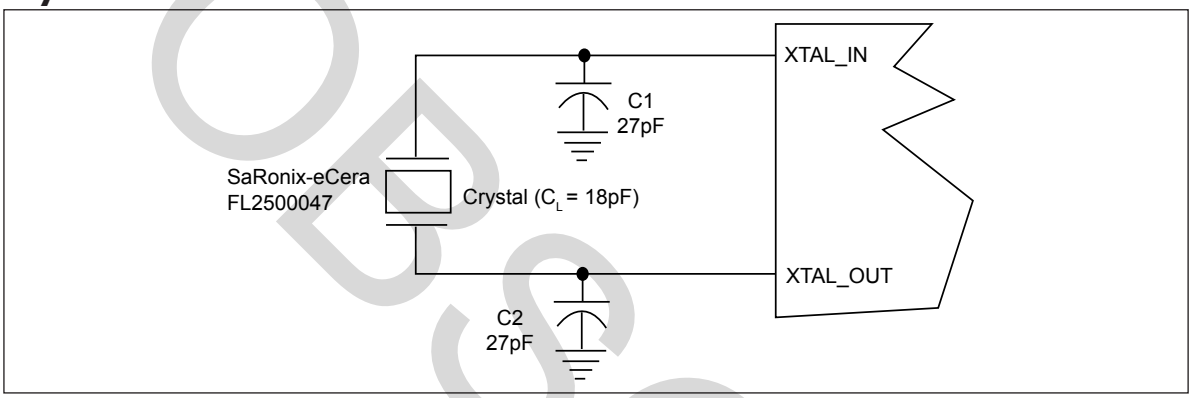
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		60.3		°C/W
	θ_{JA}	1 m/s air flow		53		°C/W
	θ_{JA}	3 m/s air flow		50		°C/W
Thermal Resistance Junction to Case	θ_{JC}			27.7		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still air		1.2		°C/W
	Ψ_{JT}	1 m/s air flow		1.5		°C/W
	Ψ_{JT}	3 m/s air flow		2.0		°C/W

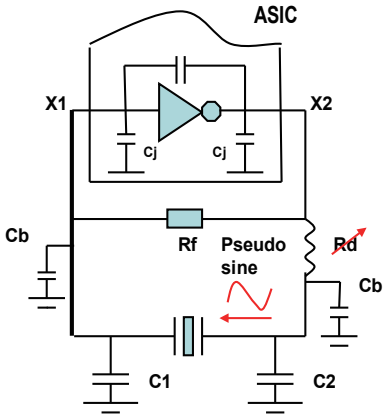
Application Notes

Crystal circuit connection

The following diagram shows PI6C49019 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 27pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit





CL= crystal spec. loading cap.

Cj = chip in/output cap. (3~5pF)

Cb = PCB trace/via cap. (2~4pF)

C1,2 = load cap. components

Rd = drive level res. (100Ω)

Final choose/trim C1=C2=2 *CL - (Cb +Cj) for the target +/-ppm
Example: C1=C2=2*(18pF) – (4pF+5pF)=27pF

Recommended Crystal Specification

Pericom recommends:

a) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

Decoupling Capacitors

Decoupling capacitors of 0.01 ìF should be connected between VDD and GND as close to the device as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into PI6C49019 pin.

Output Termination

The PCI-Express differential clock outputs of the PI6C49019 are push-pull and require an external series resistor. These resistor values and their allowable locations are shown in detail in the PCI-Express Layout Guidelines section.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from PI6C49019.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

PCI-Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure	Notes
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	1,2	
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1,2	
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1,2	
R_S	33	ohm	1,2	

Down Device Differential Routing	Dimension or Value	Unit	Figure	Notes
L4 length, Route as coupled microstrip 100 ohm differential trace.	2 min to 16 max	inch	1	
L4 length, Route as coupled stripline 100 ohm differential trace.	1.8 min to 14.4 max	inch	1	

Figure 1: Down Device Routing

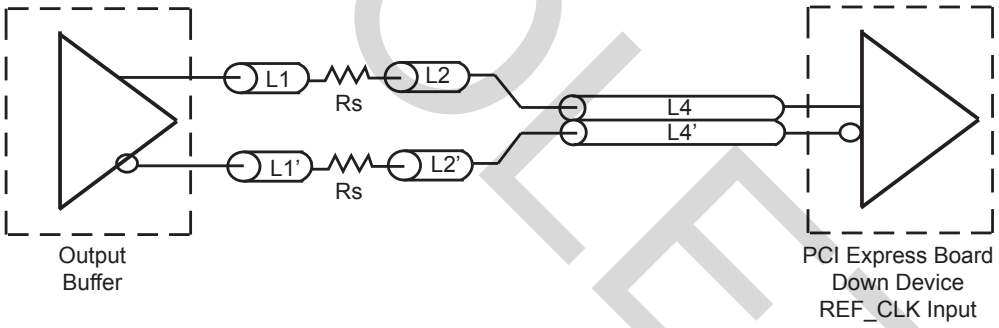
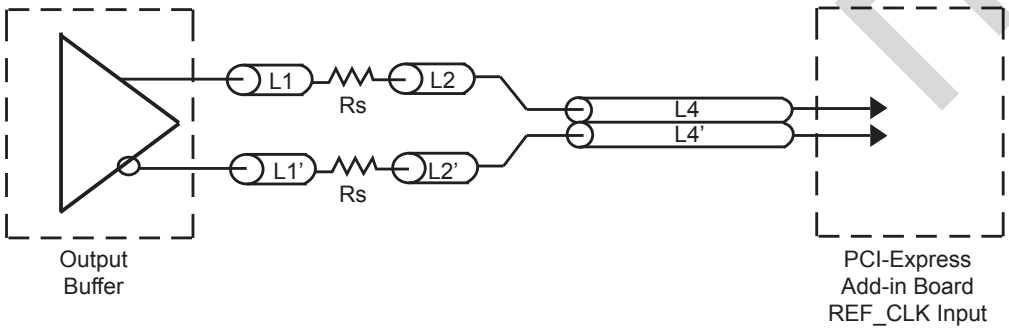


Figure 2: PCI-Express Connector Routing



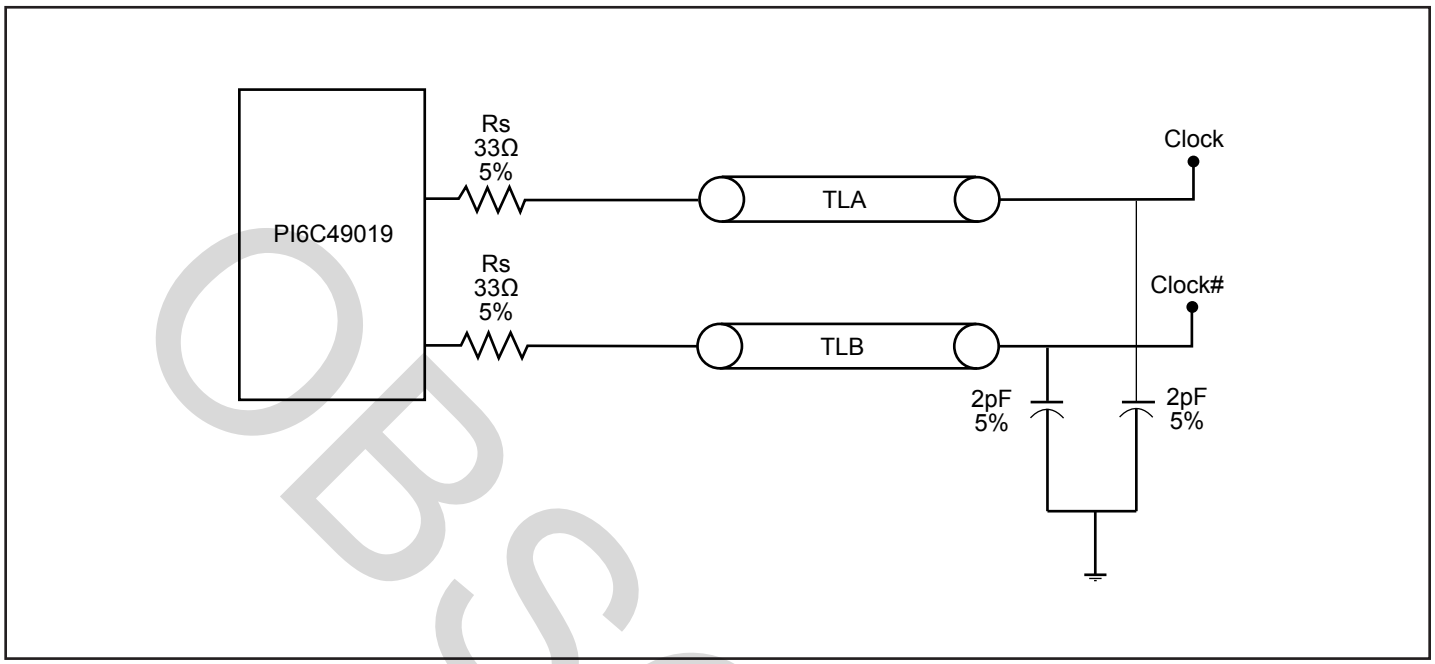
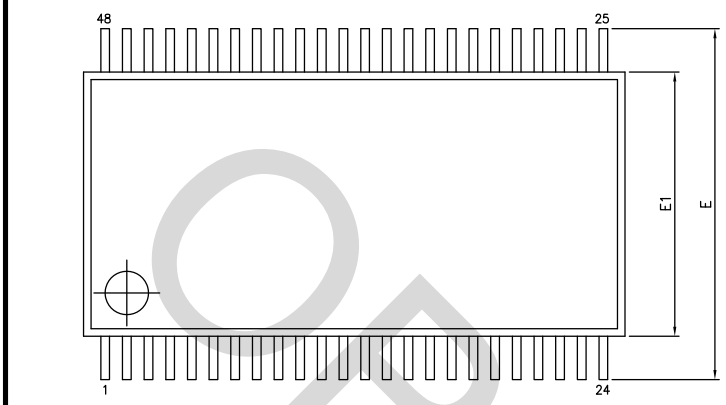
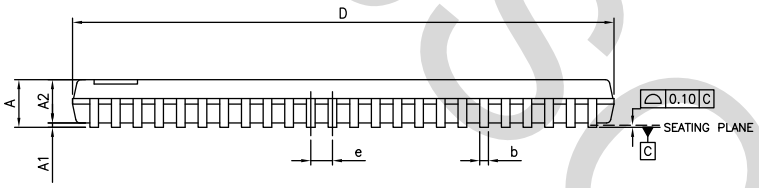


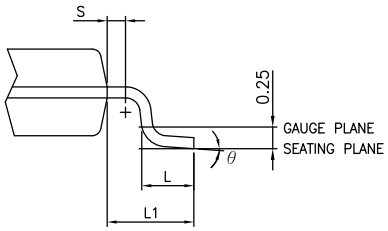
Figure 4. Configuration Test Load Board Termination

Packaging Mechanical: 48-Pin TSSOP (A48)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.17	–	0.27
c	0.09	–	0.20
D	12.40	12.50	12.60
E1	6.00	6.10	6.20
E	7.90	8.10	8.30
e	0.50 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





DETAIL F

Notes:
1. Controlling Dimension in Millimeters. Angle in Degrees.
2. Refer JEDEC MO–153F
3. Package Outline Exclusive of Mold Flash and Metal Burr.

PERICOM Enabling Serial Connectivity

DATE: 03/30/16

DESCRIPTION: 48-Pin, 240mil Wide TSSOP

PACKAGE CODE: A (A48)

DOCUMENT CONTROL #: PD-1501 REVISION: H

16-0065

Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C49019AIE	A	48-pin, Pb-free & Green, TSSOP, (A48)
PI6C49019AIEX	A	48-pin, Pb-free & Green, TSSOP, (A48), Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel