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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PI6C49X0204B-A

Low Skew, 1-TO-4 LVCMOS/LVTTL Fanout Buffer

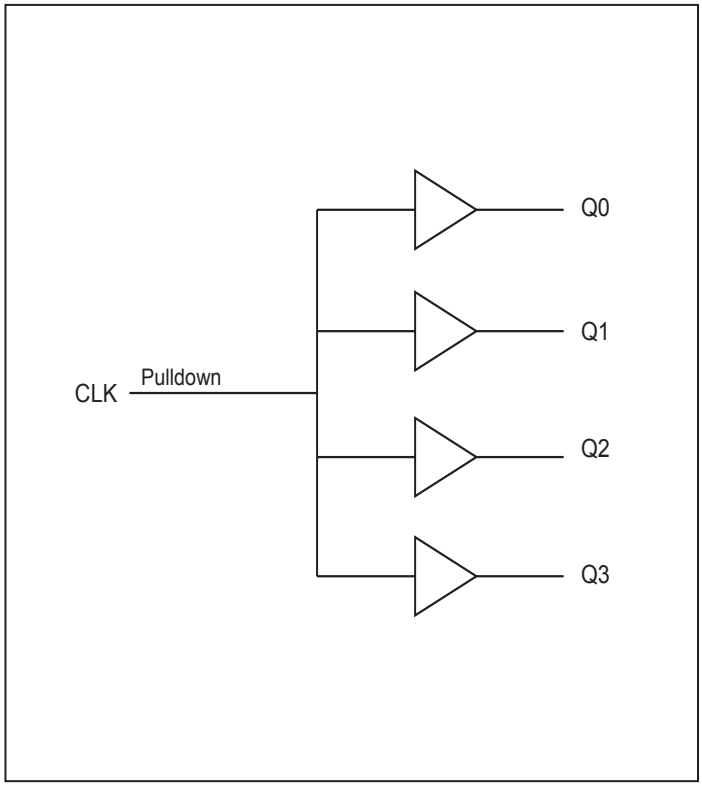
Features

- Four LVCMOS / LVTTL outputs
- LVCMOS / LVTTL clock input
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 200MHz
- Additive phase jitter, RMS: 0.06ps (typical) @ 3.3V
- Output skew: 45ps (maximum) @ 3.3V
- Part-to-part skew: 500ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V core supply, 3.3V or 2.5V output supply
- 0°C to 70°C ambient operating temperature

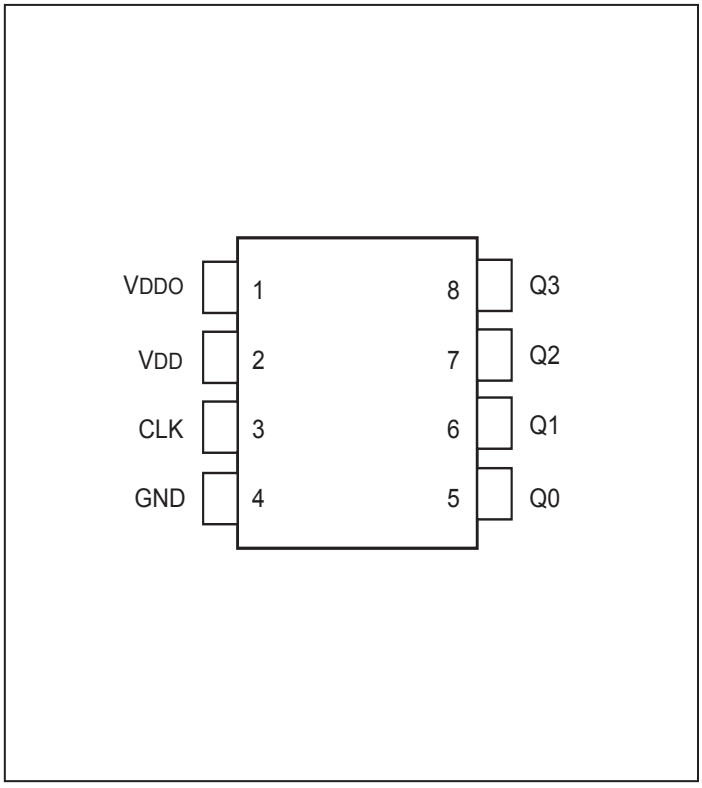
Description

The PI6C49X0204B-A is a low skew, 1-to-4 Fanout Buffer. Guaranteed output and part-to-part skew characteristics make the PI6C49X0204B-A ideal for those clock distribution applications demanding well defined performance and repeatability.

Block Diagram



Pin Assignment



Pin Descriptions

Pin#	Pin Name	Pin Type		Pin Description
1	V_{DDO}	Power		Output supply pin.
2	V_{DD}	Power		Positive supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTL interface levels.

Note: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Pin Characteristics

Symbol	Parameter	Test Conditions	Min.	Typical	Max.	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} , V_{DDO} = 3.465V			15	pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DD} , V_{DDO} >2.5V	5	7	12	Ω

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage, V_{DD} 4.6V
Inputs, V_I . . . . . –0.5V to V_{DD} +0.5V
Output, V_O . . . . . –0.5V to V_{DDO} +0.5V
Package Thermal Impedance, θ_{JA} . . . . . 112.7°C/W (0 lfpm)
Storage Temperature, T_{STG} . . . . . -65°C to 150°C

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, T_A = 0°C TO 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Core Supply Voltage	3.3V Operation	3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage	3.3V Supply	3.135	3.3	3.465	V
		2.5V Supply	2.375	2.5	2.625	
I_{DD}	Power Supply Current				22	mA
I_{DDO}	Output Supply Current	25MHz			7	mA
		200MHz			45	mA

LVCMOS / LVTTL DC CHARACTERISTICS, T_A = 0°C to 70°C

AC CHARACTERISTICS, VDD = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency	VDDO = 3.3V			200	MHz
		VDDO = 2.5V			200	
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	VDDO = 3.3V, $f \leq$ 200MHz	1.9	2.35	2.8	ns
		VDDO = 2.5V, $f \leq$ 200MHz	2.3		3.3	
tsk(o)	Output Skew; NOTE 2			25	100	ps
tsk(pp)	Part-to-Part Skew; NOTE 3			250	500	ps
t_R	Output Rise Time NOTE 4	VDDO = 3.3V	280		800	ps
		VDDO = 2.5V	280		850	
t_F	Output Fall Time NOTE 4	VDDO = 3.3V	280		800	ps
		VDDO = 2.5V	280		850	
odc	Output Duty Cycle	VDDO = 3.3V, $f \leq$ 133MHz	45		55	%
		VDDO = 3.3V, 133MHz < $f \leq$ 200MHz	40		60	%
		VDDO = 2.5V, $f \leq$ 133MHz	45		55	%
		VDDO = 2.5V, 133MHz < $f \leq$ 200MHz	40		60	%
t_{jit}	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.06		ps
		125MHz (@12kHz to 20MHz)		0.04		ps

Parameters measured at f_{MAX} unless otherwise noted.

NOTE 1: Measured from VDD /2 of the input to VDDO /2 of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO /2.

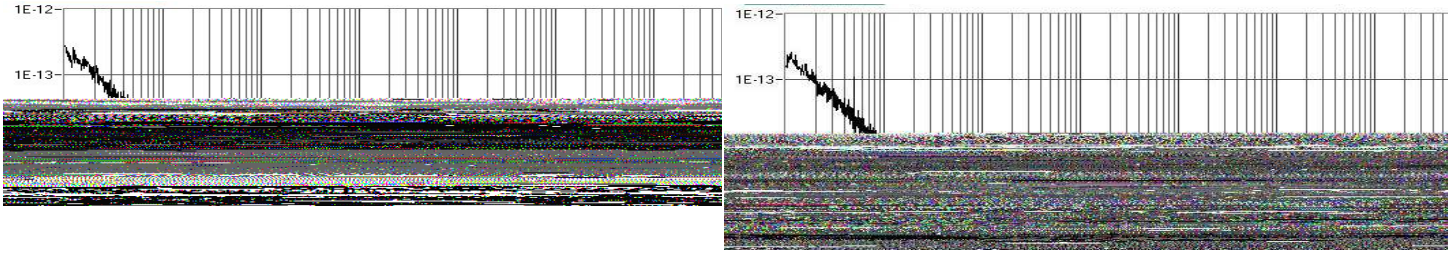
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO /2.

NOTE 4: Defined from 20% to 80%

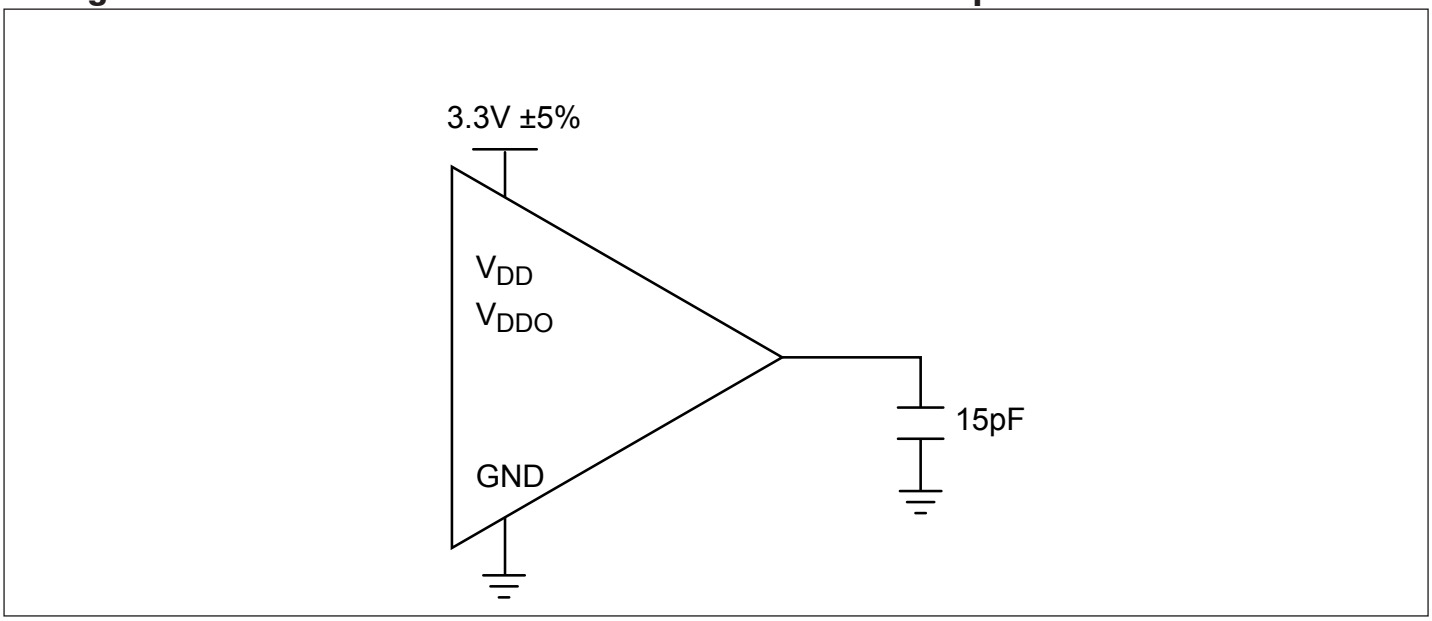
Phase Noise and Additive Jitter

Output phase noise (Right plot) vs Input Phase noise (Left plot)

Additive jitter is calculated at ~60.2fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$

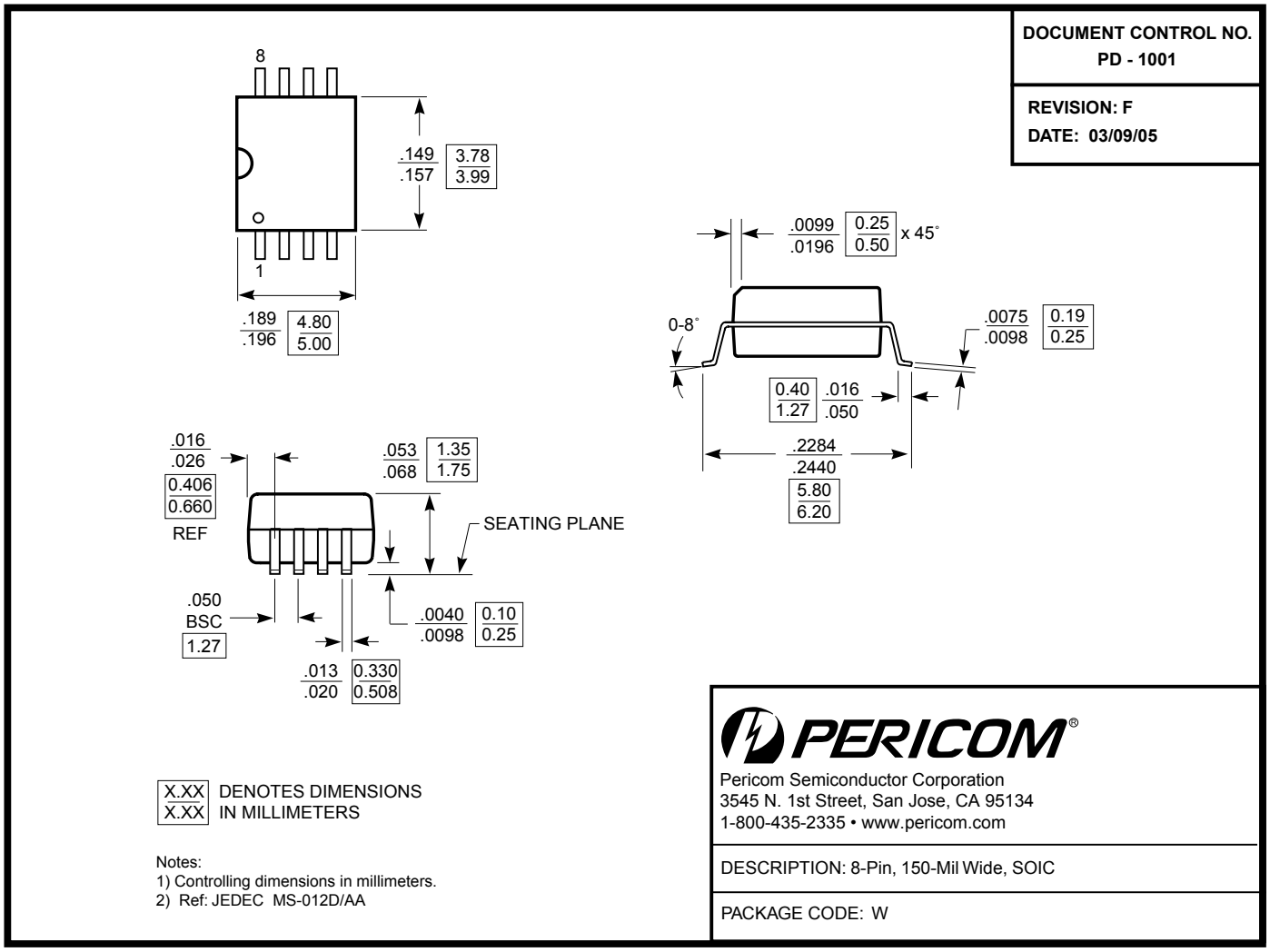


Configuration Test Load Board Termination for LVCMOS Outputs



Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	157 °C/W
Θ_{JC}	Junction-to-case thermal resistance		42 °C/W



Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C49X0204B-AWE	W	8-pin, Pb-free & Green, SOIC

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel