



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



4 -Output Low Power PCIE GEN 1-2-3 Buffer

Features

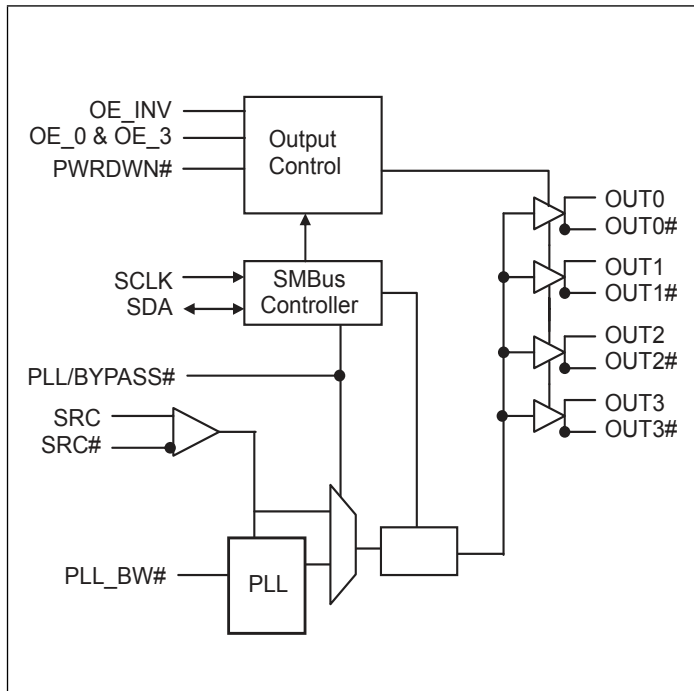
- Phase jitter filter for PCIe 3.0/ 2.0/ 1.0 application
- Low power consumption with independent output power supply 1.8V~3.3V
- Low skew < 60ps
- Low cycle-to-cycle jitter - 45ps (typ.) @100MHz
- < 1 ps additive RMS phase jitter
- Output Enable for all outputs
- Programmable PLL Bandwidth
- 100 MHz PLL Mode operation
- 1 - 400 MHz Bypass Mode operation
- 3.3V Operation
- Packaging (Pb-free and Green):
-28-Pin TSSOP (L28)

Description

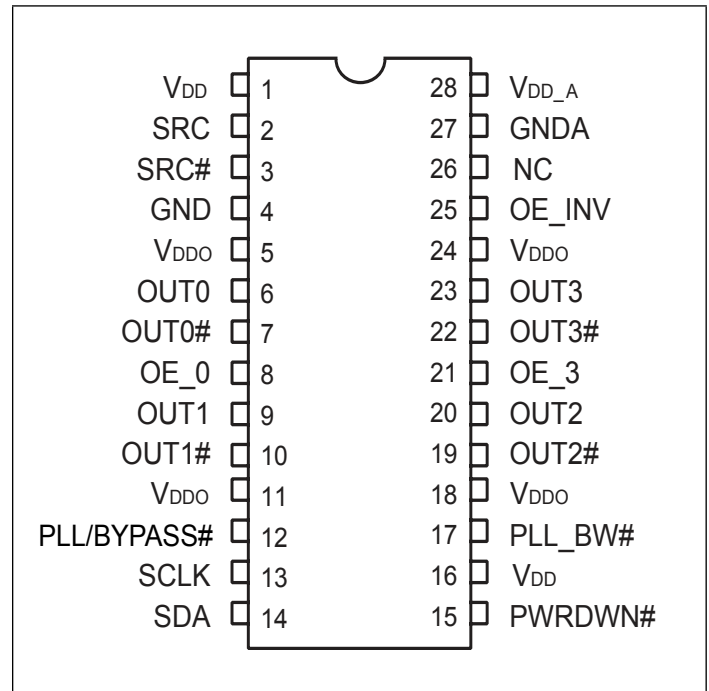
Pericom Semiconductor's PI6CDBL402B is a PCIe 3.0 compliant high-speed, low-noise differential clock buffer designed to be companion to PCIe 3.0 clock generator. It is backward compatible with PCIe 1.0 and 2.0 specification.

The device distributes the differential SRC clock from PCIe 3.0 clock generator to four differential pairs of clock outputs either with or without PLL. The clock outputs are controlled by input selection of PWRDWN# and SMBus, SCLK and SDA.

Block Diagram



Pin Configuration



Pin Description

| Pin # | Pin Name | Type | Description |
|-----------------------------|----------------------|--------|--|
| 2, 3 | SRC & SRC# | Input | 0.7V Differential SRC input from PI6C410 clock synthesizer |
| 8, 21 | OE_0 & OE_3 | Input | 3.3V LVTTL input for enabling outputs, active high. OE_0 for OUT0 / OUT0# OE_3 for OUT3 / OUT3# |
| 25 | OE_INV | Input | 3.3V LVTTL input for inverting the OE and PWRDWN# pins. When 0 = same stage When 1 = OE_0, OE_3, PWRDWN# inverted. |
| 6, 7, 9, 10, 19, 20, 22, 23 | OUT[0:3] & OUT[0:3]# | Output | 0.7V Differential outputs, refer Power Management Table for detail output status |
| 12 | PLL/BYPASS# | Input | 3.3V LVTTL input for selecting fan-out of PLL operation. |
| 13 | SCLK | Input | SMBus compatible SCLOCK input |
| 14 | SDA | I/O | SMBus compatible SDATA |
| 26 | NC | | No Connect |
| 17 | PLL_BW# | Input | 3.3V LVTTL input for selecting the PLL bandwidth |
| 15 | PWRDWN# | Input | 3.3V LVTTL input for Power Down operation, active low |
| 5, 11, 18, 24 | V _{DDO} | Power | Power supply for outputs, range from 1.8V~3.3V |
| 4 | GND | Ground | Ground for Outputs |
| 27 | GND _A | Ground | Ground for PLL |
| 28 | V _{DD_A} | Power | 3.3V Power Supply for PLL |
| 1, 16 | V _{DD} | Power | 3.3V Power Supply for PLL |

Power Management Table

Output[0]/ Output[3] state choose

| OE_INV | PWRDWN# | Byte0/Bit7 | OE_0/OE_3(Pin) | OE(SMBus bit) | OUT0/ OUT3 | OUT0#/ OUT3# |
|--------|---------|------------|----------------|---------------|--------------|--------------|
| 0 | X | X | 0 | X | LOW | LOW |
| 0 | X | X | X | 0 | LOW | LOW |
| 0 | 0 | 0 | 1 | 1 | HIGH | LOW |
| 0 | 0 | 1 | X | X | LOW | LOW |
| 0 | 1 | X | 1 | 1 | Clock output | Clock output |
| 1 | X | X | 1 | X | LOW | LOW |
| 1 | X | X | X | 0 | LOW | LOW |
| 1 | 1 | 0 | 0 | 1 | HIGH | LOW |
| 1 | 1 | 1 | X | X | LOW | LOW |
| 1 | 0 | X | 0 | 1 | Clock output | Clock output |

Output[1]/ Output[2] state choose

| OE_INV | PWRDWN# | Byte0/Bit7 | OE(Pin) | OE(SMBus bit) | OUT1/ OUT2 | OUT1#/ OUT2# |
|--------|---------|------------|---------|---------------|--------------|--------------|
| 0 | X | X | NA | 0 | LOW | LOW |
| 0 | 0 | 0 | NA | 1 | HIGH | LOW |
| 0 | 0 | 1 | NA | X | LOW | LOW |
| 0 | 1 | X | NA | 1 | Clock output | Clock output |
| 1 | X | X | NA | 0 | LOW | LOW |
| 1 | 1 | 0 | NA | 1 | HIGH | LOW |
| 1 | 1 | 1 | NA | X | LOW | LOW |
| 1 | 0 | X | NA | 1 | Clock output | Clock output |

Notes:

- all registers can't be written/read during PWRDWN# active

Serial Data Interface (SMBus)

This part is a slave only device that supports blocks read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer by issuing STOP.

Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|----|----|----|----|----|----|----|-----|
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0/1 |

Data Protocol

| | | | | | | | | | | | | | |
|-----------|------------|-----|-----|-----------------|-----|----------------|-----|-------------|-----|-----|-----------------|-----|----------|
| 1 bit | 7 bits | 1 | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | | 8 bits | 1 | 1 bit |
| Start bit | Slave Addr | R/W | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte 0 | Ack | ... | Data Byte N - 1 | Ack | Stop bit |

Notes:

- Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|---|------|--------------------|---------------------|------------|
| 0 | Reserved | | | | NA |
| 1 | PLL/BYPASS# 0 = Fanout 1 = PLL | RW | 1 = PLL | OUT[0:3], OUT[0:3]# | NA |
| 2 | PLL Bandwidth 0 = High Bandwidth, 1 = Low Bandwidth | RW | 1 = Low | OUT[0:3], OUT[0:3]# | NA |
| 3 | Reserved | | | | NA |
| 4 | Reserved | | | | NA |
| 5 | Reserved | | | | NA |
| 6 | Reserved | | | | NA |
| 7 | PD_Mode Refer Power Management Table | RW | 0 | OUT[0:3], OUT[0:3]# | NA |

Data Byte 1: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|-----------------------------|------|--------------------|--------------------|------------|
| 0 | Reserved | | | | NA |
| 1 | OUTPUTS enable | RW | 1 = Enabled | OUT0, OUT0# | NA |
| 2 | 1 = Enabled 0 = Disabled | RW | 1 = Enabled | OUT1, OUT1# | NA |
| 3 | Reserved | | | | NA |
| 4 | Reserved | | | | NA |
| 5 | OUTPUTS enable | RW | 1 = Enabled | OUT2, OUT2# | NA |
| 6 | 1 = Enabled 0 = Disabled | RW | 1 = Enabled | OUT3, OUT3# | NA |
| 7 | Reserved | | | | NA |

Data Byte 2: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|--------------|------|--------------------|--------------------|------------|
| 0 | Reserved | | | | NA |
| 1 | Reserved | | | | NA |
| 2 | Reserved | | | | NA |
| 3 | Reserved | | | | NA |
| 4 | Reserved | | | | NA |
| 5 | Reserved | | | | NA |
| 6 | Reserved | | | | NA |
| 7 | Reserved | | | | NA |

Data Byte 3: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|--------------|------|--------------------|--------------------|------------|
| 0 | Reserved | RW | | | |
| 1 | | RW | | | |
| 2 | | RW | | | |
| 3 | | RW | | | |
| 4 | | RW | | | |
| 5 | | RW | | | |
| 6 | | RW | | | |
| 7 | | RW | | | |

Data Byte 4: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|--------------|------|--------------------|--------------------|------------|
| 0 | Pericom ID | R | 0 | NA | NA |
| 1 | | R | 0 | NA | NA |
| 2 | | R | 0 | NA | NA |
| 3 | | R | 0 | NA | NA |
| 4 | | R | 0 | NA | NA |
| 5 | | R | 1 | NA | NA |
| 6 | | R | 0 | NA | NA |
| 7 | | R | 0 | NA | NA |

Power Down (PWRDWN# assertion)

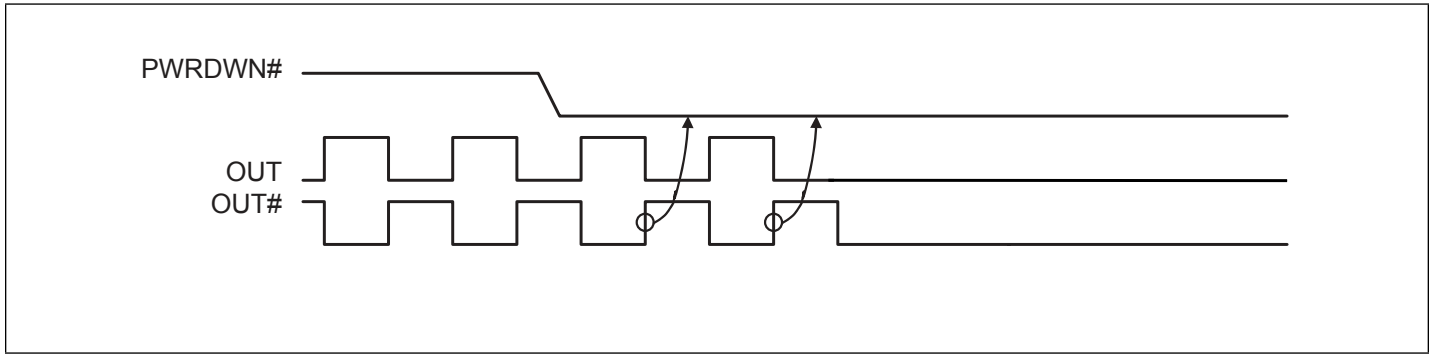


Figure 1. Power down sequence

Power Down (PWRDWN# De-assertion)

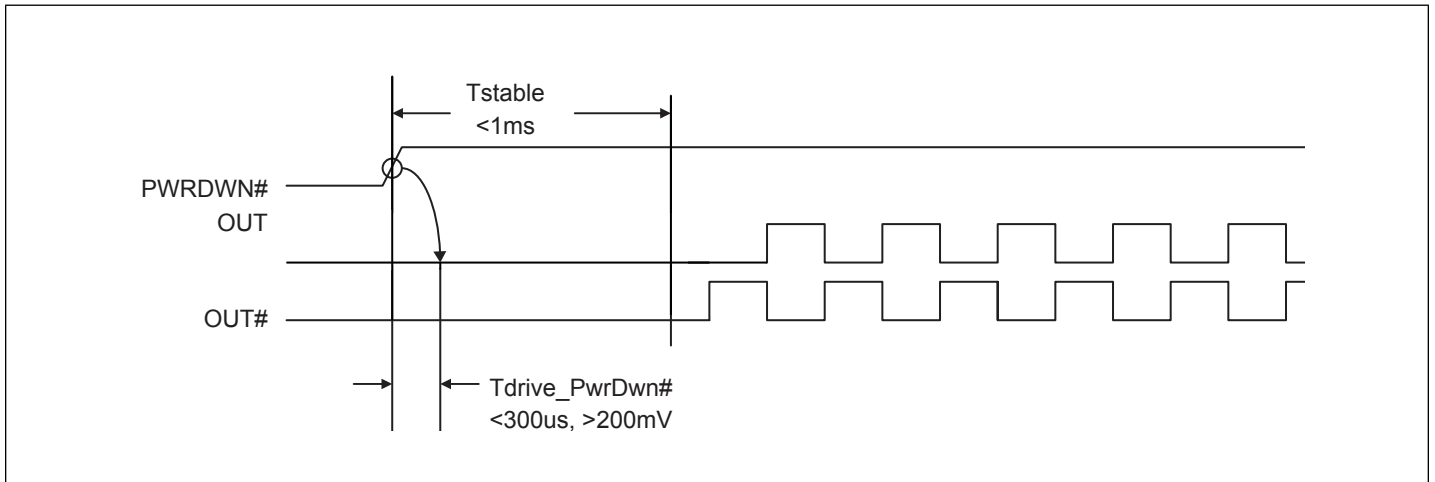
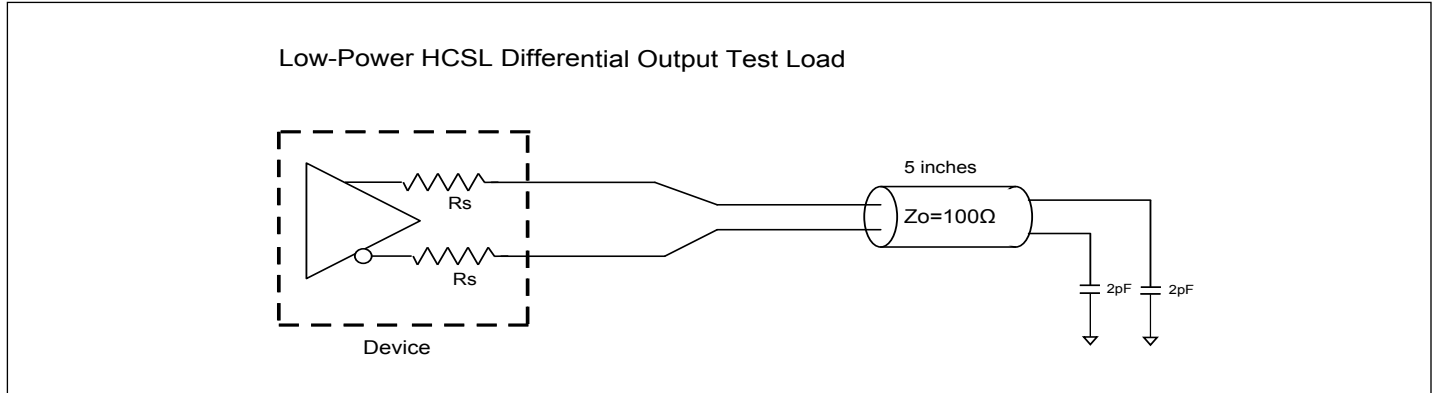
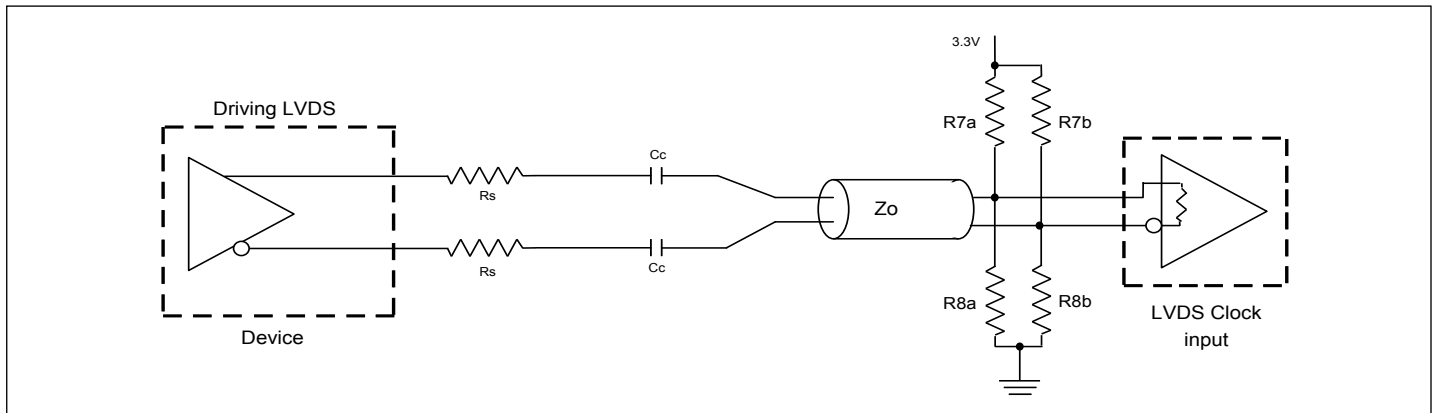


Figure 2. Power down de-assert sequence

Test Loads



Driving LVDS



Driving LVDS inputs with the PI6CDBL402B

| Component | Value | | Note |
|-----------|--------------------------|------------------------------------|------|
| | Receiver has termination | Receiver does not have termination | |
| R7a, R7b | 10K Ω | 140 Ω | |
| R8a, R8b | 5.6K Ω | 75 Ω | |
| Cc | 0.1 uF | 0.1 uF | |
| Vcm | 1.2 volts | 1.2 volts | |

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|---|-------------------------------|
| Supply Voltage to Ground Potential..... | 4.6V |
| All Inputs and Output..... | -0.5V toV _{DD} +0.5V |
| Ambient Operating Temperature..... | -40 to +85°C |
| Storage Temperature..... | -65°C to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature..... | 260°C |
| ESD Protection (Input) | 2000V(HBM) |

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics–Clock Input Parameters (T_A = -40~85°C; VDD = 3.3V+/-10%; VDDO = 3.3V+/-10%, VDDO = 2.5V+/-10%, VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

| Symbol | Parameters | Condition | Min. | Type | Max. | Units |
|--------------------|--|---|--------------------------|------|------|-------|
| V _{IHDIF} | Input High Voltage - DIF_IN ¹ | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV |
| V _{ILDOF} | Input Low Voltage - DIF_IN ^{1,3} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV |
| V _{COM} | Input Common Mode Voltage - DIF_IN ¹ | Common Mode Input Voltage | 300 | | 725 | mV |
| V _{SWING} | Input Amplitude - DIF_IN ¹ | Peak to Peak value (V _{IHDIF} - V _{ILDIF}) | 300 | | 1450 | mV |
| dv/dt | Input Slew Rate - DIF_IN ^{1,2} | Measured differentially | 0.4 | | | V/ns |
| I _{IN} | Input Leakage Current ¹ | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA |
| d _{tin} | Input Duty Cycle ¹ | Measurement from differential wave- from | 45 | | 55 | % |
| J _{DIFIn} | Input Jitter - Cycle to Cycle ¹ | Differential Measurement | 0 | | 150 | ps |

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven from a single ended clock by driving the true clock and biasing the complement clock input to the VBIAS, where VBIAS is (VIH-HIGH - VIHLOW)/2

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating

Conditions ($T_A = -40\sim 85^\circ\text{C}$; SVDD = 3.3V+/-10%; VDDO = 3.3V+/-10%, VDDO = 2.5V+/-10%, VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

| Symbol | Parameters | Condition | Min. | Type | Max. | Units |
|---------------------|--|--|--------------------|--------|------------------|--------|
| V_{DD_A}, V_{DD} | Supply Voltage ¹ | Supply voltage for core, analog | 3.0 | 3.3 | 3.6 | V |
| V_{DDO} | Supply Voltage ¹ | 3.3V Operation | 2.97 | 3.3 | 3.63 | V |
| | | 2.5V Operation | 2.25 | 2.5 | 2.75 | |
| | | 1.8V Operation | 1.62 | 1.8 | 1.98 | |
| V_{IH} | Input High Voltage ¹ | Single-ended inputs, except SMBus | 0.65 V_{DD} | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage ¹ | Single-ended inputs, except SMBus | -0.3 | | 0.35 V_{DD} | V |
| V_{IH} | Output High Voltage ¹ | Single-ended outputs, except SMBus. $I_{OH} = -2\text{mA}$ | V_{DD}^- 0.45 | | | V |
| V_{IL} | Output Low Voltage ¹ | Single-ended outputs, except SMBus. $I_{OL} = -2\text{mA}$ | | | 0.45 | V |
| I_{IN} | Input Current ¹ | Single-ended inputs, $V_{IN} = \text{GND}$, $V_{IN} = \text{VDD}$ | -5 | | 5 | uA |
| I_{INP} | | Single-ended inputs $V_{IN} = 0\text{V}$; Inputs with internal pull-up resistors $V_{IN} = \text{VDD}$; Inputs with internal pull-down resistors | -200 | | 200 | uA |
| F_{ibyp} | Input Frequency ² | Bypass mode | 1 | | 400 | MHz |
| $F_{ipll100}$ | | 100MHz PLL mode | 95 | 100.00 | 105 | MHz |
| L_{pin} | Pin Inductance ¹ | | | | 7 | nH |
| C_{IN} | Capacitance ^{1,4} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF |
| C_{INDIF_IN} | | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF |
| C_{OUT} | | Output pin capacitance | | | 6 | pF |
| T_{STAB} | Clk Stabilization ^{1,2} | From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.6 | 1 | ms |
| f_{MODIN} | Input SS Modulation Frequency ¹ | Allowable Frequency (Triangular Modulation) | 30 | 31.500 | 33 | kHz |
| $t_{LATO\#}$ | OE# Latency ^{1,3} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | clocks |
| $t_{DRV\#}$ | Tdrive_PD# ^{1,3} | DIF output enable after PD# de-assertion | | | 300 | us |
| t_F | Tfall ^{1,2} | Fall time of single-ended control inputs | | | 5 | ns |
| t_R | Trise ^{1,2} | Rise time of single-ended control inputs | | | 5 | ns |
| V_{ILSMB} | SMBus Input Low Voltage ¹ | | | | 0.8 | V |
| V_{IHSMB} | SMBus Input High Voltage ¹ | | 2.1 | | 3.6 | V |

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions Cont...

| Symbol | Parameters | Condition | Min. | Type | Max. | Units |
|--------------|--|--------------------------------------|------|------|------|-------|
| V_{OLSMB} | SMBus Output Low Voltage ¹ | @ I_{PULLUP} | | | 0.4 | V |
| I_{PULLUP} | SMBus Sink Current ¹ | @ V_{OL} | 4 | | | mA |
| V_{DDSMB} | Nominal Bus Voltage ¹ | 3.3V bus voltage | 2.7 | | 3.6 | V |
| t_{RSMB} | SCLK/SDATA Rise Time ¹ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns |
| t_{FSMB} | SCLK/SDATA Fall Time ¹ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns |
| f_{MAXSMB} | SMBus Operating Frequency ^{1,5} | Maximum SMBus operating frequency | | | 400 | kHz |

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing. Input Frequency Capacitance
3. Time from deassertion until outputs are >200 mV
4. DIF_IN input
5. The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Low Power HCSL Outputs ($T_A = -40\sim 85^\circ\text{C}$; $V_{DD} = 3.3\text{V}\pm 10\%$; $V_{DDO} = 3.3\text{V}\pm 10\%$, $V_{DDO} = 2.5\text{V}\pm 10\%$, $V_{DDO} = 1.8\text{V}\pm 10\%$, See Test Loads for Loading Conditions)

| Symbol | Parameters | Condition | Min. | Type | Max. | Units |
|------------------------|-----------------------------|---|------|------|------|-------|
| Trf | Slew rate ^{1,2,3} | | 1.1 | 2 | 4.5 | V/ns |
| V_{HIGH} | Voltage High ^{1,7} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | | 950 | mV |
| V_{LOW} | Voltage Low ^{1,7} | | -150 | | 200 | mV |
| Vmax | Max Voltage ¹ | Measurement on single ended signal using absolute value. (Scope averaging off) | | | 1150 | mV |
| Vmin | Min Voltage ¹ | | -300 | | | mV |
| Vswing | Vswing ^{1,2,7} | Scope averaging off | 300 | | | mV |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | | 550 | mV |
| Crossing Voltage (var) | Δ -Vcross | Scope averaging off | | | 140 | mV |

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
5. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
6. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ -Vcross to be smaller than Vcross absolute.
7. At default SMBus settings.

Electrical Characteristics–Current Consumption ($T_A = -40\sim 85^\circ\text{C}$; $V_{DD} = 3.3\text{V}\pm 10\%$; $V_{DDO} = 3.3\text{V}\pm 10\%$, $V_{DDO} = 2.5\text{V}\pm 10\%$, $V_{DDO} = 1.8\text{V}\pm 10\%$, See Test Loads for Loading Conditions)

| Symbol | Parameters | Condition | Min. | Type | Max. | Units |
|------------|---------------------------------------|--|------|------|------|-------|
| I_{DDOP} | Operating Supply Current ¹ | Total power consumption, All outputs active @100MHz, typical value under $V_{DDO} = 1.8\text{V}$ | | 50 | 60 | mA |
| | | Total power consumption, All outputs active @100MHz PLL bypass mode, typical value under $V_{DDO} = 1.8\text{V}$ | | 24 | 28 | mA |
| I_{DDPD} | Powerdown Current ^{1,2} | Total power consumption, Outputs Low | | | 1.3 | mA |

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics ($T_A = -40\sim 85^\circ\text{C}$; $V_{DD} = 3.3\text{V}\pm 10\%$; $V_{DDO} = 3.3\text{V}\pm 10\%$, $V_{DDO} = 2.5\text{V}\pm 10\%$, $V_{DDO} = 1.8\text{V}\pm 10\%$, See Test Loads for Loading Conditions)

| Symbol | Parameters | Condition | Min. | Type | Max. | Units |
|---------------|---------------------------------------|--|------|------|------|-------|
| t_{DC} | Duty Cycle ¹ | Measured differentially, PLL Mode | 45 | | 55 | % |
| t_{DCD} | Duty Cycle Distortion ^{1,3} | Measured differentially, Bypass Mode @100MHz | -1.3 | 0 | 1.3 | % |
| t_{pdBYP} | Skew, Input to Output ^{1,4} | Bypass Mode, $V_T = 50\%$ | 2500 | | 5000 | ps |
| t_{pdPLL} | | PLL Mode $V_T = 50\%$ | -260 | | 260 | ps |
| t_{skew} | Skew, Output to Output ^{1,2} | PLL Mode $V_T = 50\%$ | | | 60 | ps |
| $t_{jyc-cyc}$ | Jitter, Cycle to cycle ^{1,2} | PLL mode | | | 60 | ps |
| | | Additive Jitter in Bypass Mode | | | 25 | ps |

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
4. All outputs at default slew rate
5. The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

Electrical Characteristics–Phase Jitter Parameters ($T_A = -40\sim 85^\circ\text{C}$; $V_{DD} = 3.3\text{V}\pm 10\%$; $V_{DDO} = 3.3\text{V}\pm 10\%$, $V_{DDO} = 2.5\text{V}\pm 10\%$, $V_{DDO} = 1.8\text{V}\pm 10\%$, See Test Loads for Loading Conditions)

| Symbol | Parameters | Condition | Min. | Type | Industry Limit | Units |
|-----------------|--|--|------|------|----------------|-------------|
| $t_{jphPCIEG1}$ | Phase Jitter, PLL Mode | PCIe Gen 1 ^{1,2,3} | | 34 | 86 | ps (p-p) |
| $t_{jphPCIEG2}$ | | PCIe Gen 2 Lo Band $10\text{kHz} < f < 1.5\text{MHz}$ ^{1,2} | | 0.9 | 3 | ps (rms) |
| | | PCIe Gen 2 High Band $1.5\text{MHz} < f < \text{Nyquist} (50\text{MHz})$ ^{1,2} | | 2.2 | 3.1 | ps (rms) |
| $t_{jphPCIEG3}$ | | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) ^{1,2,3,4} | | 0.5 | 1 | ps (rms) |
| $t_{jphSGMII}$ | | 125MHz, 1.5MHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz ^{1,6} | | 1.9 | NA | ps (rms) |
| $t_{jphPCIEG1}$ | Additive Phase Jitter, Bypass Mode | PCIe Gen 1 ^{1,2,3} | | 0.6 | N/A | ps (p-p) |
| $t_{jphPCIEG2}$ | | PCIe Gen 2 Lo Band $10\text{kHz} < f < 1.5\text{MHz}$ ^{1,2,5} | | 0.1 | N/A | ps (rms) |
| | | PCIe Gen 2 High Band $1.5\text{MHz} < f < \text{Nyquist} (50\text{MHz})$ ^{1,2,5} | | 0.05 | N/A | ps (rms) |
| $t_{jphPCIEG3}$ | | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) ^{1,2,4,5} | | 0.05 | N/A | ps (rms) |
| $t_{jphSGMII}$ | | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz ^{1,6} | | 0.15 | N/A | ps (rms) |

Note:

1. Applies to all outputs, with device driven by 9FG432AKLF or equivalent.
2. See <http://www.pcisig.com> for complete specs
3. Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.
4. Subject to final ratification by PCI SIG.
5. For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = $\text{SQRT}[(\text{total jitter})^2 - (\text{input jitter})^2]$
6. Applies to all differential outputs

Packaging Mechanical: 28-Pin TSSOP (L)

DOCUMENT CONTROL NO.
PD - 1313

REVISION: D
DATE: 03/09/05

Note:

- Package Outline Exclusive of Mold Flash and Metal Burr
- Controlling dimensions in millimeters
- Ref: JEDEC MO-153F/AE

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 28-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Ordering Information⁽¹⁻³⁾

| Ordering Code | Package Code | Package Description |
|-----------------|--------------|---|
| PI6CDBL402BLIE | LE | 28-pin, 173-mil wide (TSSOP) |
| PI6CDBL402BLIEX | LE | 28-pin, 173-mil wide (TSSOP), Tape & Reel |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel