



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**PLL Clock Driver for
1.8V DDR2 Memory**
Features

- PLL clock distribution optimized for DDR2-667/533/400 SDRAM applications.
- Distributes one differential clock input pair to eleven differential clock output pairs.
- Differential Inputs (CLK, $\overline{\text{CLK}}$) and (FBIN, $\overline{\text{FBIN}}$)
- Input OE/OS: LVC MOS
- Differential Outputs (Y[0:9], $\overline{\text{Y}}[0:9]$) and (FBOU, $\overline{\text{FBOU}}$)
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input.
- Operates at $\text{AV}_{\text{DD}} = 1.8\text{V}$ for core circuit and internal PLL, and $\text{V}_{\text{DDQ}} = 1.8\text{V}$ for differential output drivers
- Packaging (Pb-free & Green):
 - 52-ball VFBGA (NF)
- PI6CU877 for DDR2-533/400 applications
- PI6CUA877 for DDR2-667/533/400 applications

Pin Configuration

	1	2	3	4	5	6
A	Y ₁	Y ₀	$\overline{\text{Y}}_0$	$\overline{\text{Y}}_5$	Y ₅	Y ₆
B	$\overline{\text{Y}}_1$	GND	GND	GND	GND	$\overline{\text{Y}}_6$
C	$\overline{\text{Y}}_2$	GND	NB	NB	GND	$\overline{\text{Y}}_7$
D	Y ₂	V _{DDQ}	V _{DDQ}	V _{DDQ}	OS	Y ₇
E	CK	V _{DDQ}	NB	NB	V _{DDQ}	FB _{IN}
F	$\overline{\text{CK}}$	V _{DDQ}	NB	NB	OE	$\overline{\text{FB}}_{\text{IN}}$
G	AGND	V _{DDQ}	V _{DDQ}	V _{DDQ}	V _{DDQ}	$\overline{\text{FB}}_{\text{OUT}}$
H	AV _{DD}	GND	NB	NB	GND	FB _{OUT}
J	Y ₃	GND	GND	GND	GND	Y ₈
k	$\overline{\text{Y}}_3$	$\overline{\text{Y}}_4$	Y ₄	Y ₉	$\overline{\text{Y}}_9$	$\overline{\text{Y}}_8$

Description

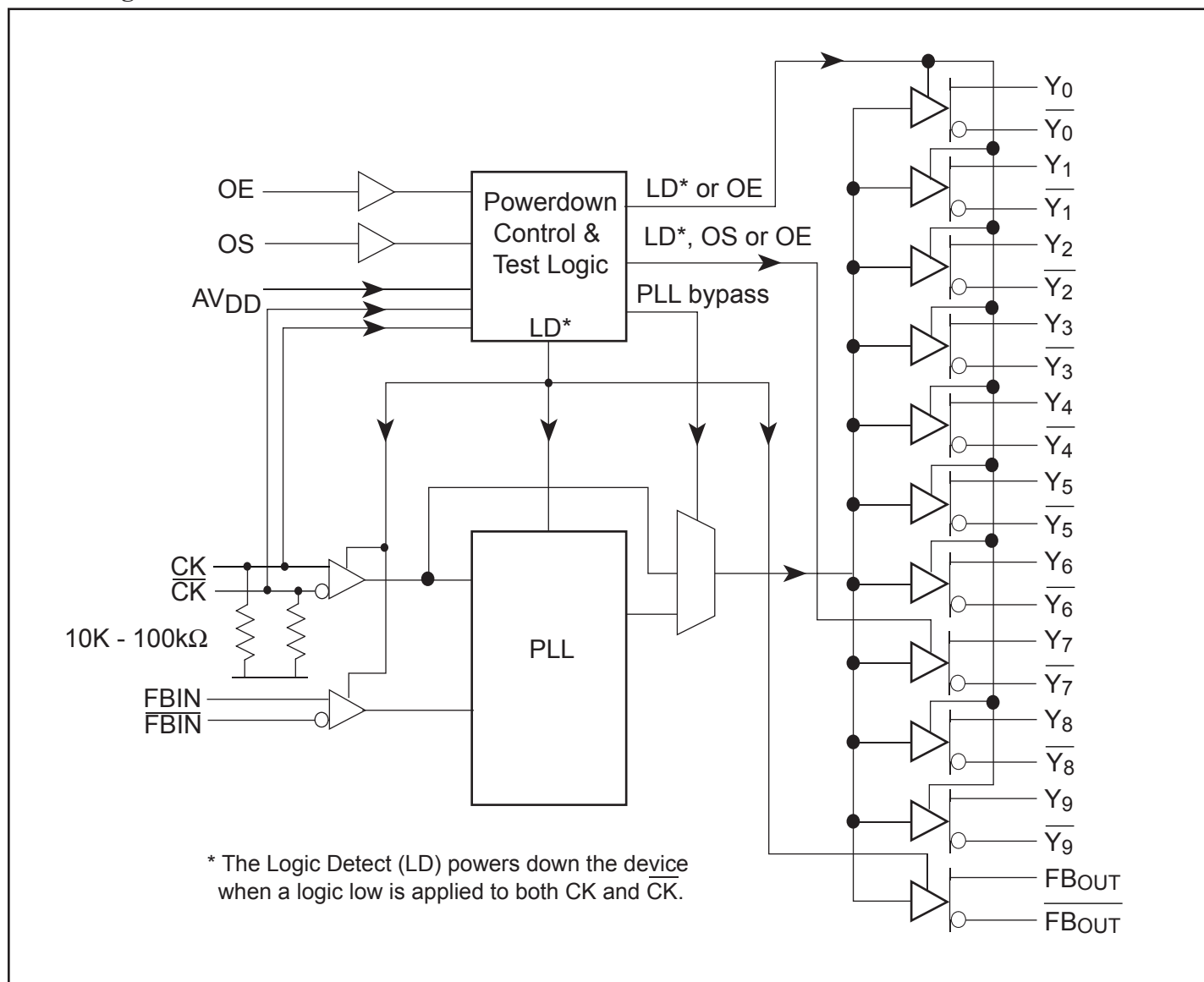
PI6CU877 is a PLL clock driver family, consisting of PI6CU877, and PI6CUA877, developed for Registered DDR2 DIMM applications with 1.8V operation and differential clock input and output levels.

The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to eleven differential pairs of clock outputs which includes feedback clock (Y[0:9], $\overline{\text{Y}}[0:9]$; FBOU, $\overline{\text{FBOU}}$).

The clock outputs are controlled by CLK/ $\overline{\text{CLK}}$, FBOU, $\overline{\text{FBOU}}$, the LVC MOS inputs (OE, OS) and the Analog Power input (AV_{DD}). When OE is LOW the outputs except $\overline{\text{FBOU}}$, $\overline{\text{FBOU}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS is a pin that must be tied to GND or V_{DD}. When OS is high, OE will function as described above. When OS is LOW, OE has no effect on Y7/Y7, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When CLK/ $\overline{\text{CLK}}$ are logic low, the device will enter a low power mode. An input logic detection circuit will detect the logic low level and perform a low power state where all Y[0:9], $\overline{\text{Y}}[0:9]$; FBOU, $\overline{\text{FBOU}}$, and PLL are OFF.

PI6CUx877 is a high-performance, low skew, and low jitter PLL clock driver, and it is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

Block Diagram


Pinout Table

Pin Name	Characteristics	Description
AGND	Ground	Analog ground
AV _{DD}	1.8V nominal	Analog power
CK	Differential Input	Clock input with a (10k - 100kΩ) pulldown resistor
$\overline{\text{CK}}$	Differential Input	Complementary clock input with a (10k - 100kΩ) pulldown resistor
FB _{IN}	Differential Input	Feedback clock input
$\overline{\text{FB}}_{\text{IN}}$	Differential Input	Complementary feedback clock input
FB _{OUT}	Differential Output	Feedback clock output
$\overline{\text{FB}}_{\text{OUT}}$	Differential Output	Complementary feedback clock output
OE	LVC MOS input	Output enable (async.)
OS	LVC MOS input	Output select (tied to GND or V _{DDQ})
GND	Ground	Ground
V _{DDQ}	1.8V nominal	Logic and output power
Y[0:9]	Differential Outputs	Clock outputs
$\overline{\text{Y}}[0:9]$	Differential Outputs	Complementary clock outputs
NB		No Ball

Function Table

Inputs					Outputs				PLL State
AV _{DD}	OE	OS	CK	$\overline{\text{CK}}$	Y	$\overline{\text{Y}}$	FB _{OUT}	$\overline{\text{FB}}_{\text{OUT}}$	
GND	H	X	L	H	L	H	L	H	Bypass/Off
GND	H	X	H	L	H	L	H	L	Bypass/Off
GND	L	H	L	H	L(Z) ⁽¹⁾	L(Z) ⁽¹⁾	L	H	Bypass/Off
GND	L	L	H	L	L(Z) ⁽¹⁾ , Y7 active	$\overline{\text{L}}(\text{Z})^{(1)}$, $\overline{\text{Y}}7$ active	H	L	Bypass/Off
Nom. V _{DD}	L	H	L	H	L(Z) ⁽¹⁾	L(Z) ⁽¹⁾	L	H	On
Nom. V _{DD}	L	L	H	L	L(Z) ⁽¹⁾ , Y7 active	$\overline{\text{L}}(\text{Z})^{(1)}$, $\overline{\text{Y}}7$ active	H	L	On
Nom. V _{DD}	H	X	L	H	L	H	L	H	On
Nom. V _{DD}	H	X	H	L	H	L	H	L	On
Nom. V _{DD}	X	X	L	L	L(Z) ⁽¹⁾	L(Z) ⁽¹⁾	L(Z) ⁽¹⁾	L(Z) ⁽¹⁾	Off
Nom. V _{DD}	X	X	H	H	Reserved				

Notes:

1. L(Z) means the outputs are disabled to a low state meeting the I_{ODL} limit on DC Specification

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{DD}	I/O supply voltage range and analog /core supply voltage range	-0.5	2.5	V
V_I	Input voltage range	-0.5	$V_{DDQ} + 0.5$	
V_O	Output voltage range	-0.5	$V_{DDQ} + 0.5$	
I_{IK}	Input clamp current	-50	50	mA
I_{OK}	Output clamp current	-50	50	
I_O	Continuous output current, $V_O = 0$ to V_{DDQ}	-50	50	
$I_{O(PWR)}$	Continuous current through each V_{DDQ} or GND	-100	100	
T_{STG}	Storage temperature	-65	150	°C

Note:

- Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Specifications Recommended Operating Conditions

Symbol	Parameter		Min.	Nom.	Max.	Units
V_{DDQ}	Output Supply Voltage		1.7	1.8	1.9	V
AV_{DD}	Supply voltage ⁽¹⁾			V_{DDQ}		
V_{IL}	Low-level input voltage ⁽²⁾	OE, OS, CK, \overline{CK}			$0.35 \times V_{DDQ}$	
V_{IH}	High-level input voltage ⁽²⁾	OE, OS, CK, \overline{CK}	$0.65 \times V_{DDQ}$			
I_{OH}	High-level output current, see Fig 2				-9	mA
I_{OL}	Low-level output current, see Fig. 2				9	
V_{IX}	Input differential-pair crossing voltage		$(V_{DDQ}/2) - 0.15$		$(V_{DDQ}/2) - 0.15$	
V_{IN}	Input voltage level		-0.3		$V_{DDQ} + 0.3$	V
V_{ID}	Input differential voltage, See Fig 9 ⁽²⁾	DC	0.3		$V_{DDQ} + 0.4$	
		AC	0.6		$V_{DDQ} + 0.4$	
T_A	Operating free air temperature		0		70	°C

Notes:

- The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are guaranteed.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} , see Figure 9 for definition. The CK and \overline{CK} , V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

FCK Clock Frequency Specifications ($V_{DD}, V_{DDQ} = 1.8 \pm 0.1V$)

PI6CUx877 Part Number	Operating Clock Frequency ^(1,2)		Application Clock Frequency ^(1,3)		Units
	Min	Max	Min	Max	
PI6CU877	125	300	160	270	MHz
PI6CUA877	125	410	160	360	MHz

Notes:

1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed debug or production testing of DIMM modules).
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.

Timing Requirements (Over recommended operating free-air temperature)

Symbol	Description	$V_{DD}, V_{DDQ} = 1.8V \pm 0.1V$		Units
		Min	Max	
t_{DC}	Input clock duty cycle	40	60	%
t_L	Stabilization time ⁽¹⁾		15	μs

1. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and CK go to a logic low state, enter the power-down mode and later return to active operation. CK and CK maybe left floating after they have been driven low for one complete clock cycle.

DC Specifications

Parameter	Description	Test Condition	V_{DD} , V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All Inputs	$I_I = -18\text{mA}$	1.7V			1.2	V
V_{OH}	HIGH output voltage	$I_{OH} = -100\mu\text{A}$	1.7 to 1.9V	$V_{DDQ} - 0.2$			
		$I_{OH} = -9\text{mA}$	1.7	1.1			
I_{ODL}	Output disabled low current	$OE = L, V_{ODL} = 100\text{mV}$	1.7V	100			μA
V_{OD}	Output differential voltage, the magnitude of the difference between the true and complimentary outputs, see fig. 9 for more details			0.6			V
I_I	CK, $\overline{\text{CK}}$	$V_I = V_{DDQ}$ or GND	1.9V			± 250	μA
	OE, OS, $\overline{\text{FB}}_{IN}, \overline{\text{FB}}_{IN}$	$V_I = V_{DDQ}$ or GND				± 10	
I_{DDLD}	Static Supply current, $I_{DDQ} + I_{ADD}$	CK and $\overline{\text{CK}} = L$				500	
I_{DD}	Dynamic supply current, $I_{DDQ} + I_{ADD}$, see note 6 for CPD calculation	CK and $\overline{\text{CK}} = 360\text{MHz}$, all outputs are open (not connected to a PCB)				300	mA
CI	CK, $\overline{\text{CK}}$	$V_I = V_{DDQ}$ or GND	1.8V	2		3	pF
	$\overline{\text{FB}}_{IN}, \overline{\text{FB}}_{IN}$	$V_I = V_{DDQ}$ or GND		2		3	
CI(Δ)	CK, $\overline{\text{CK}}$	$V_I = V_{DDQ}$ or GND				0.25	
	$\overline{\text{FB}}_{IN}, \overline{\text{FB}}_{IN}$	$V_I = V_{DDQ}$ or GND				0.25	

Notes:

6. Total $I_{DD} = I_{DDQ} + I_{ADD} = F_{CK} * C_{PD} * V_{DDQ}$, solving for $C_{PD} = (I_{DDQ} + I_{ADD}) / (F_{CK} * V_{DDQ})$ where F_{CK} is the input frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

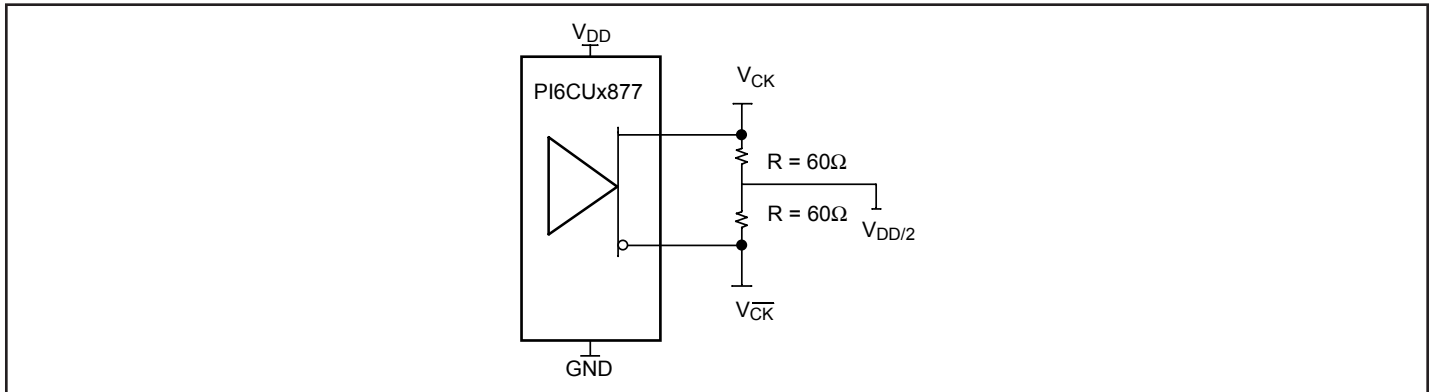
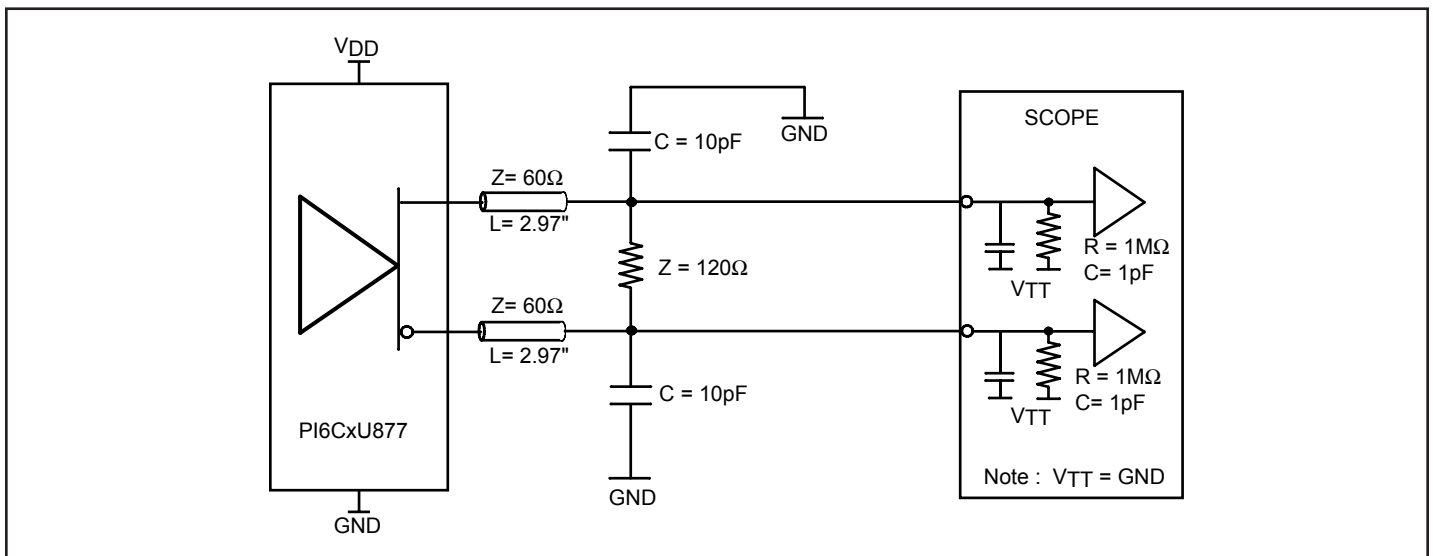
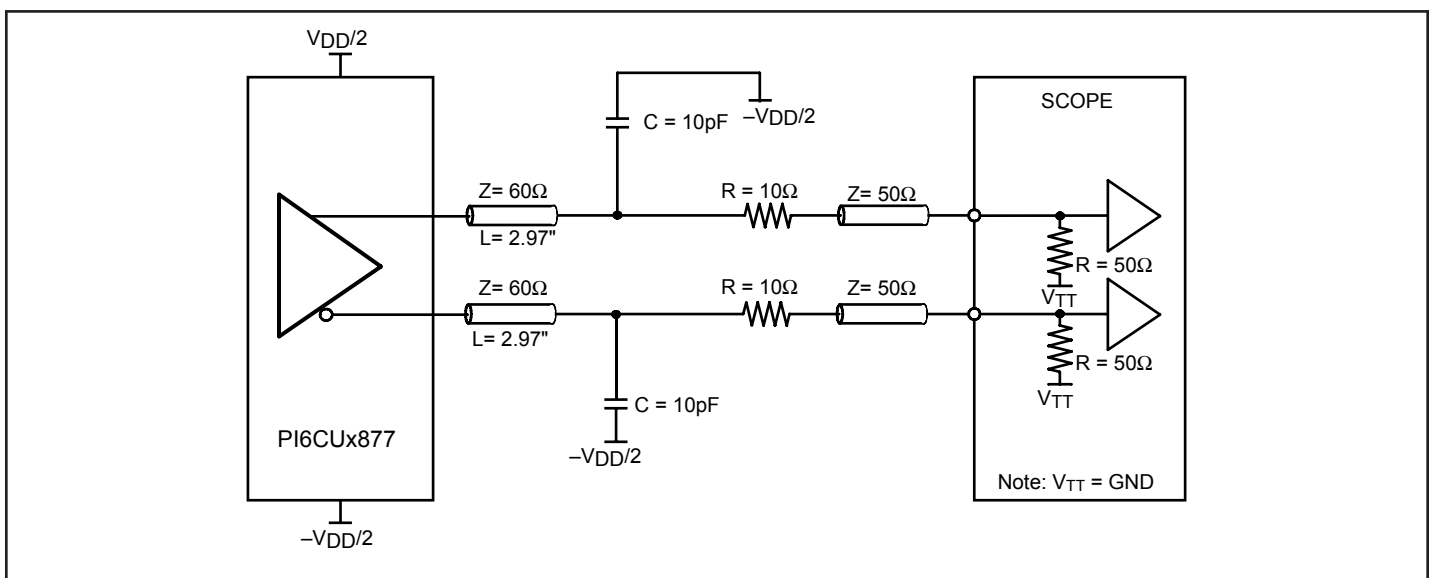
AC Specifications

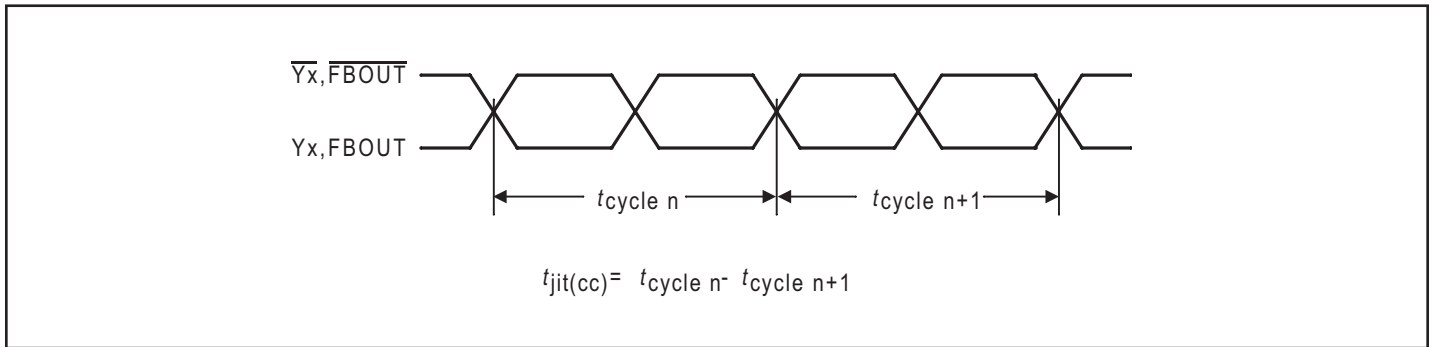
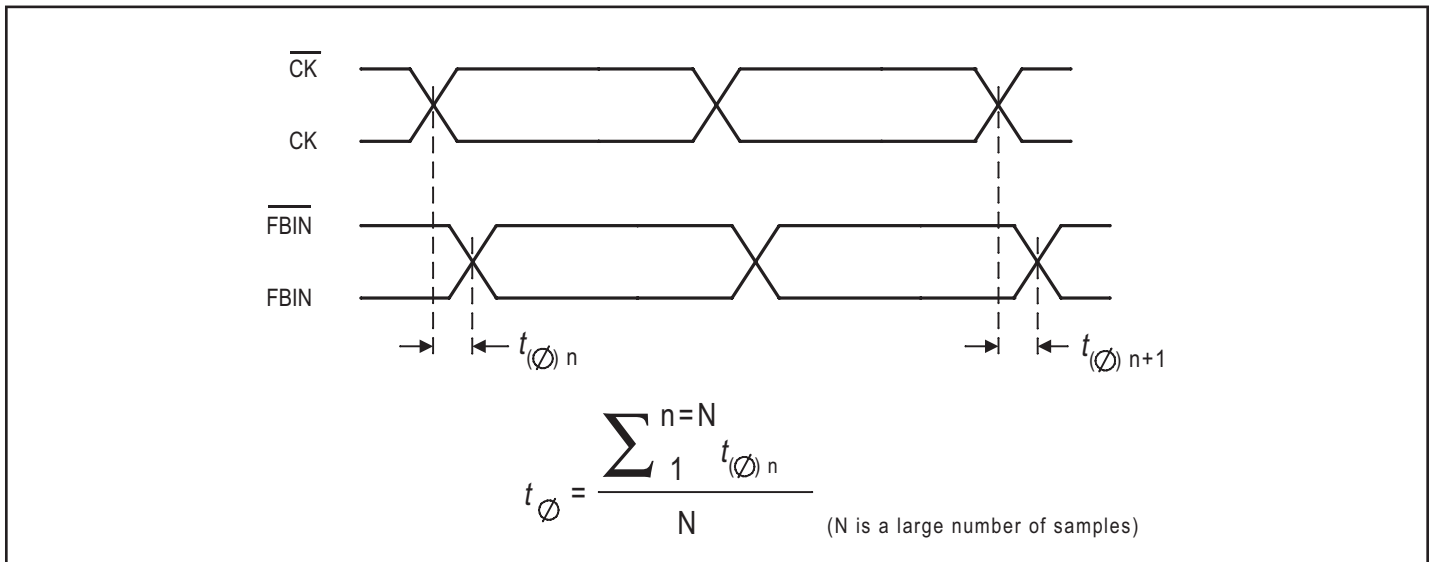
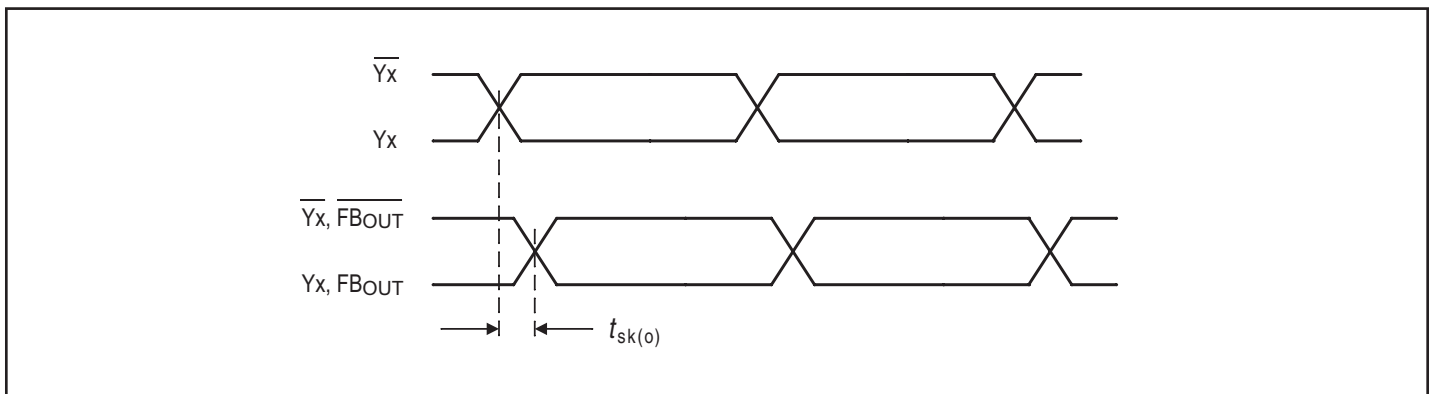
Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁵⁾

Parameter	Description	Diagram	AV _{DD} , V _{DDQ} = 1.8 ±0.1V			Units
			Min.	Nom.	Max.	
ten	OE to and Y/Y	see Fig 11			8	ns
t _{dis}	OE to and Y/Y	see Fig 11			8	
t _{jit(cc+)}	Cycle-to-cycle jitter	see Fig 4	0		40	ps
t _{jit(cc-)}			0		-40	
t(∅)	Static phase offset ⁽¹¹⁾	see Fig 5	-50		50	
t(∅) _{dyn}	Dynamic phase offset	see Fig 10	-50		50	
tsk(o)	Output clock skew	see Fig 6			40	
t _{jit(per)}	Period jitter ⁽¹²⁾	see Fig 7	-40		40	
t _{jit(hper)}	Half period jitter ⁽¹²⁾ 160 to 270 MHz	see Fig 8	-75		75	
	Half period jitter ⁽¹²⁾ 271 to 360 MHz	see Fig 8	-50		50	
slr(i)	Input clock slew rate	see Fig 9	1	2.5	4	V/ns
	Output enable (OE)	see Fig 9	0.5			
slr(o)	Output clock slew rate ^(14, 16)	see Fig 1, 9	1.5	2.5	3	
V _{OX}	Output differential-pair cross voltage ⁽¹³⁾	see Fig 2	(V _{DDQ} /2) -0.1		(V _{DDQ} /2) +0.1	V
The PLL on the PI6CUx877 is capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:						
	SSC modulation frequency		30.00		33	kHz
	SSC clock input frequency deviation		0.00		-0.50	%
PI6CUx877 PLL design should target the values below to minimize the SCC induced skew:						
	PLL Loop Bandwidth		2.0			MHz

Notes:

11. Static Phase Offset does not include Jitter
12. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
13. VOX specified at the DRAM clock input or the test load.
14. To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK, CK and Feedback Clock Input FBIN, FBIN are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these nominal values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
15. There are two terminations that are used with the above ac tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross-voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables should be used.
16. The Output slew rate is determined from IBIS model load shown in Figure 1. It is measured single-ended.


Figure 1. IBIS Model Output Load

Figure 2. Output Load Test Circuit 1

Figure 3. Output Load Test Circuit 2


Figure 4. Cycle-to-Cycle Jitter

Figure 5. Static Phase Offset

Figure 6. Output Skew

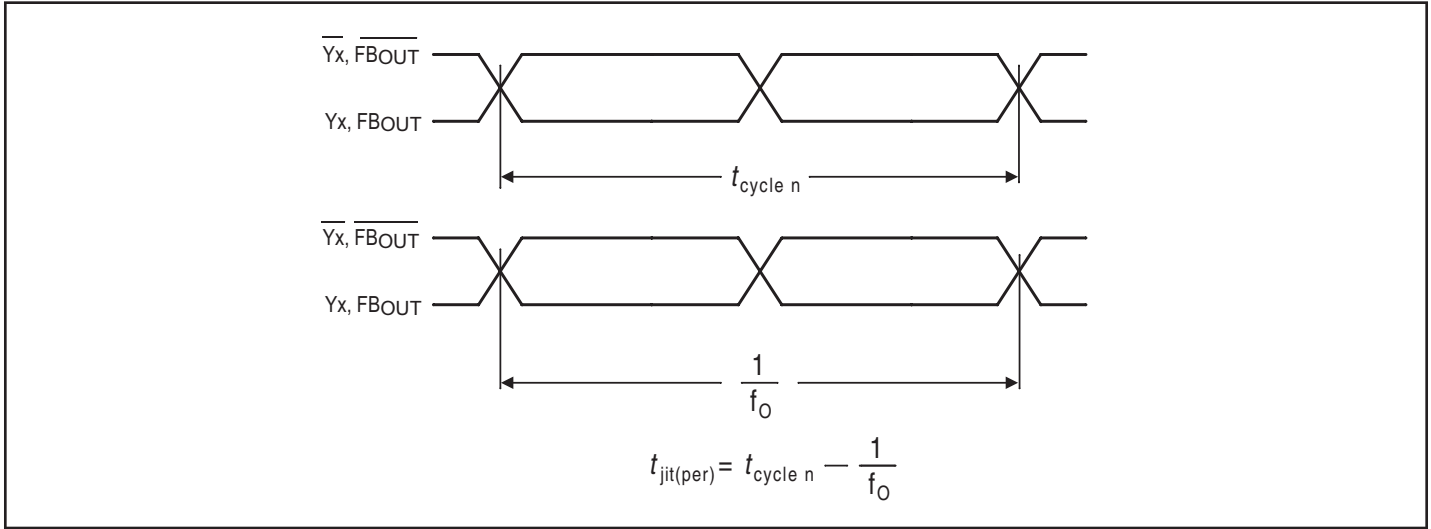


Figure 7. Period Jitter (fo = average input frequency measured at CK/CK)

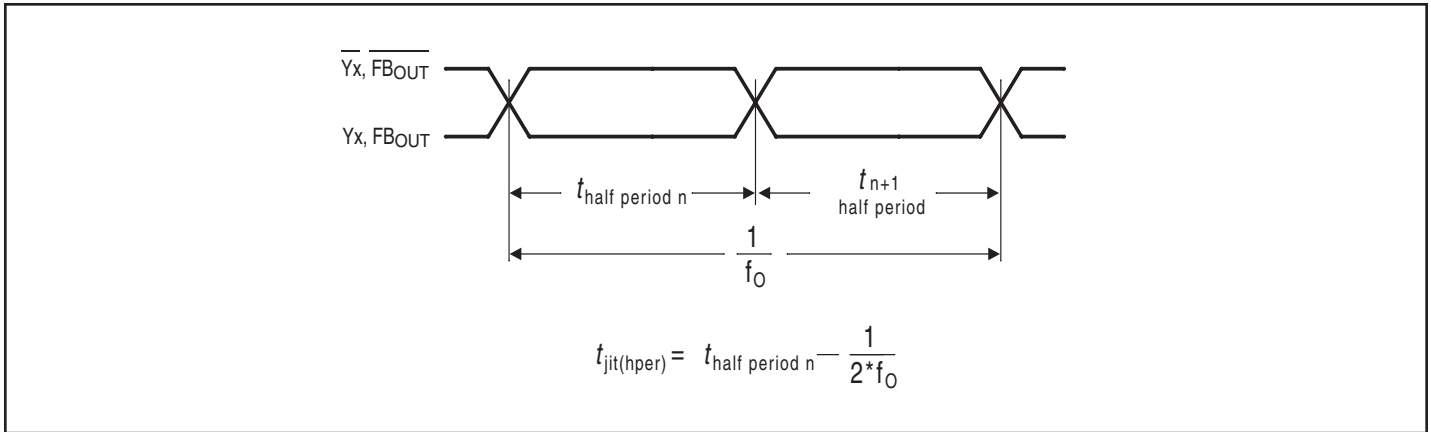


Figure 8. Half-Period Jitter

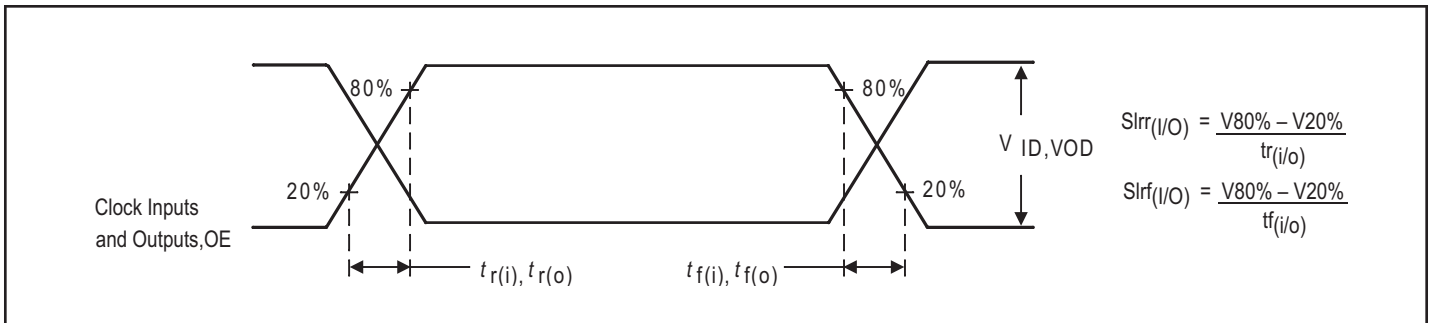


Figure 9. Input and Output Slew Rates

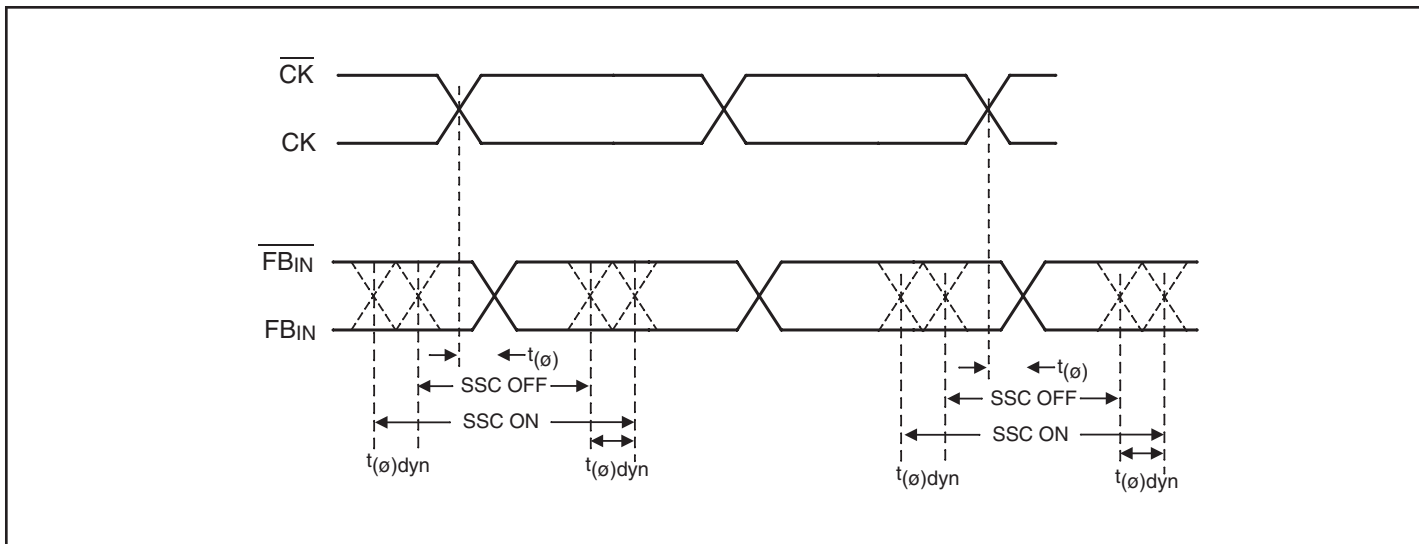


Figure 10. Dynamic Phase Offset

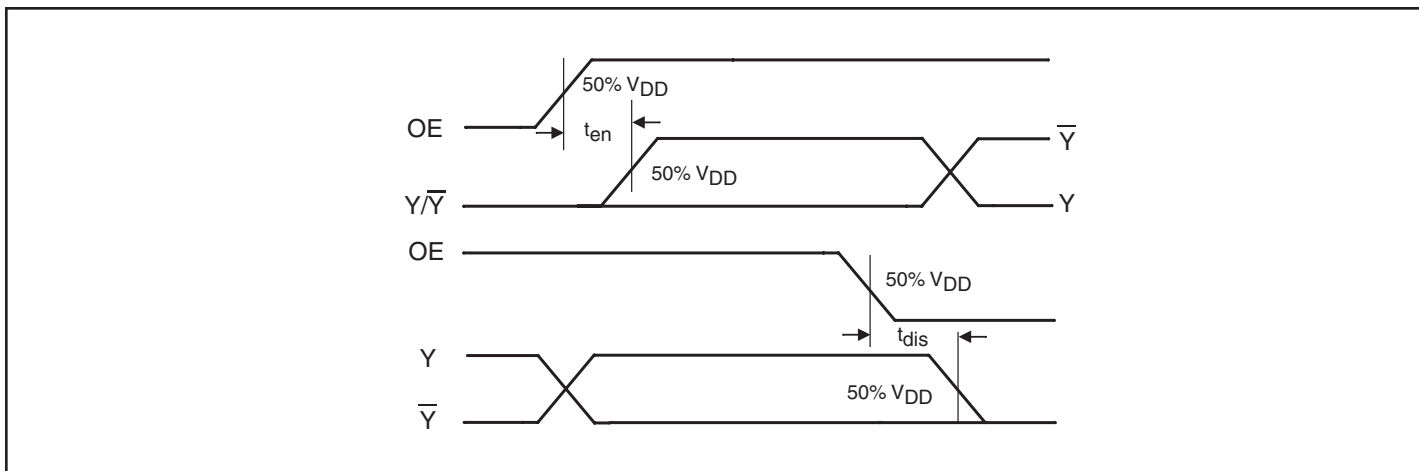
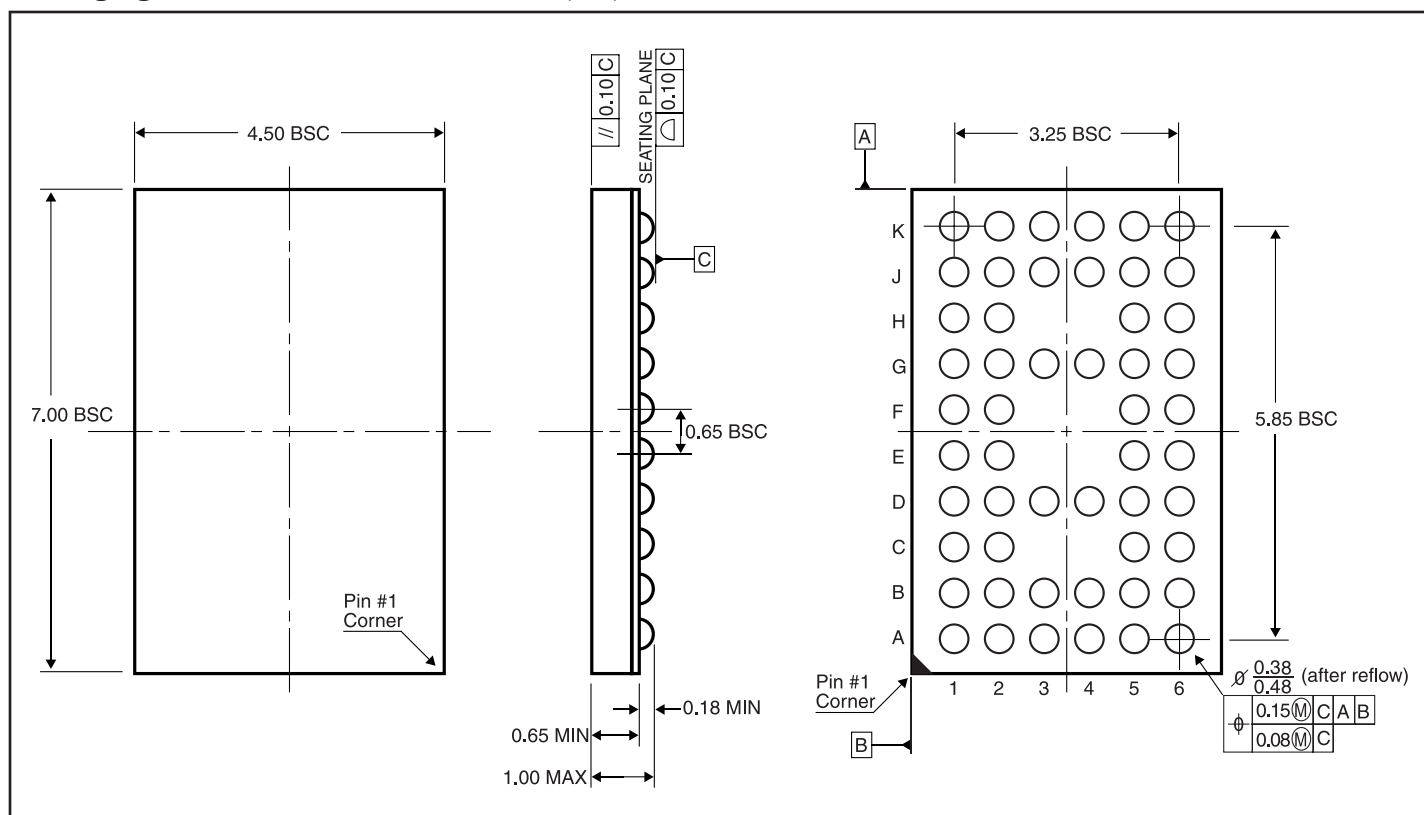


Figure 11. Time Delay Between Output Enable (OE) and Clock Output (\overline{Y} , Y)

Packaging Mechanical: 52-Ball VFBGA (NF)



Ordering Information(1,2)

Ordering Code	Package Code	Package Description
PI6CU877NFE	NF	Pb-free & Green, 52-ball VFBGA
PI6CUA877NFE	NF	Pb-free & Green, 52-ball VFBGA

Notes:

1. Thermal characteristics can be found on the company web site at <http://www.pericom.com/packaging/>
2. E = Pb-free and Green