



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



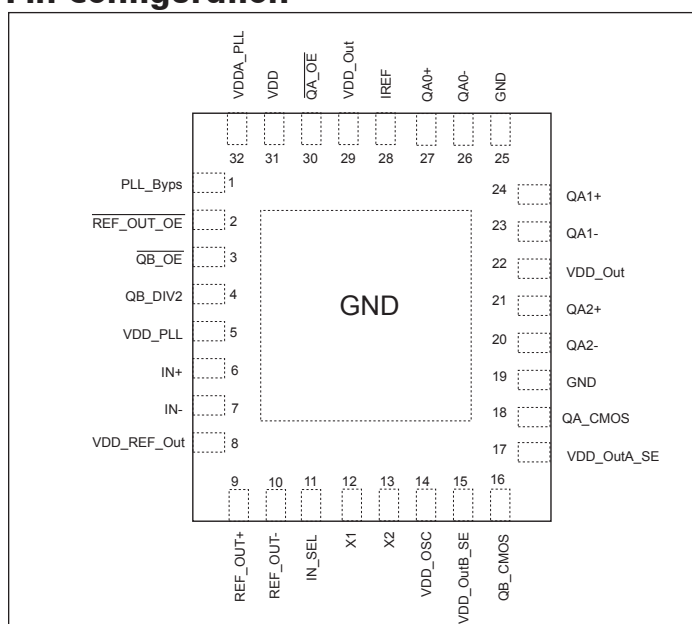
## Features

- 3.3V supply voltage
- 3 HCSL and 1 LVCMOS 100MHz outputs with OE/ function
- 1 LVCMOS 100/50MHz selectable
- 25MHz crystal or differential input
- Low 1ps RMS max integrated phase noise design
- PLL Bypass mode for test
- 32 lead 5x5mm TQFN package

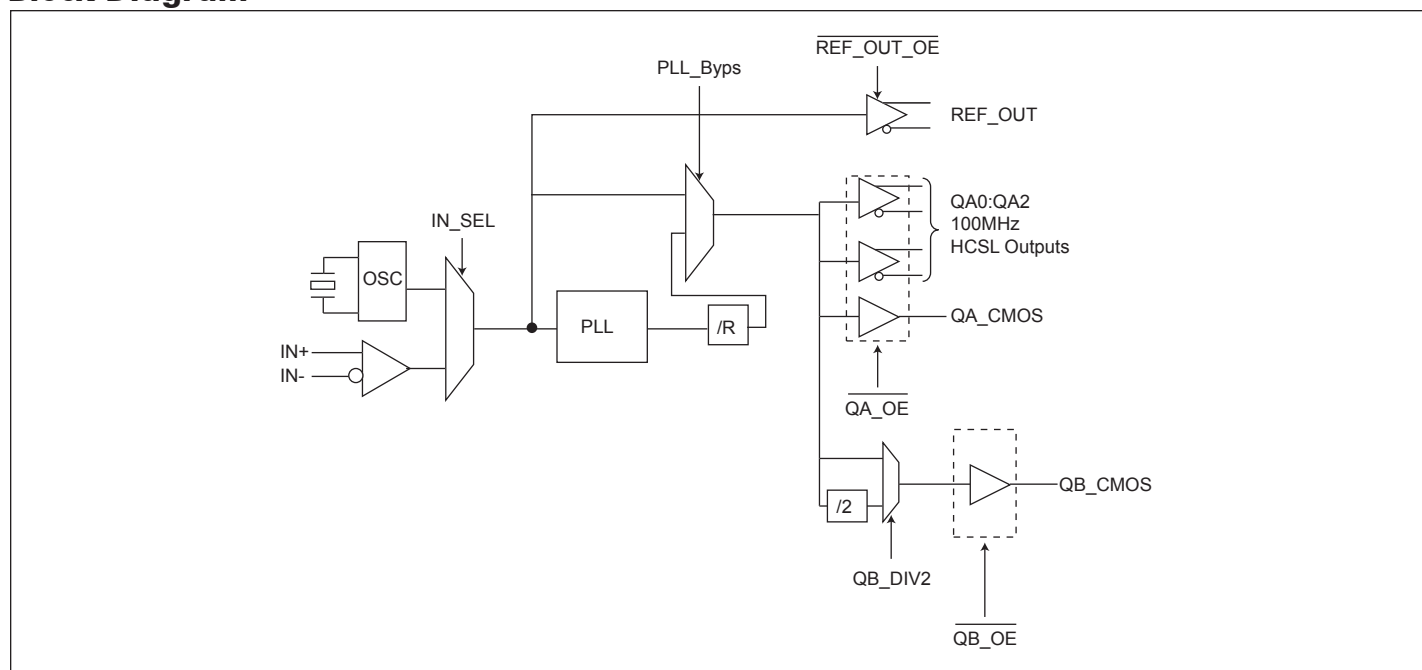
## Description

The PI6LC4830 is an LC VCO based low phase noise design intended for the most demanding PCIe® 2.0 applications. Use of the ultra-low noise LC VCO allows for much greater noise margins than traditional solutions. This is ideal for noisy environments.

## Pin Configuration



## Block Diagram



## Pin Description

| Pin Number             | Pin Name                                             | Type                 | Description                                                                                                                        |
|------------------------|------------------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 20, 21, 23, 24, 26, 27 | QA0+, QA0-, QA1+, QA1-, QA2+, QA2-                   | Output (HCSL)        | 100MHz HCSL Outputs                                                                                                                |
| 9, 10                  | REF_Out+, REF_Out-                                   | Output (LVPECL)      | 25MHz LVPECL output from fundamental oscillator core                                                                               |
| 12                     | X1                                                   | Input                | Crystal input pin                                                                                                                  |
| 13                     | X2                                                   | Output               | Oscillator output pin                                                                                                              |
| 6, 7                   | IN+, IN-                                             | Input (Differential) | HCSL/LVPECL/LVDS inputs                                                                                                            |
| 11                     | IN_SEL                                               | Input (LVCMOS)       | Low selects X1 and X2, High selects In+, In-. Internal pull up is 100k Ohms                                                        |
| 1                      | PLL_Byps                                             | Input (LVCMOS)       | If Low, output buffers are switched to the PLL. If High, output buffers are switched to the input mux. Internal 100K-Ohm pulldown. |
| 30, 3                  | $\overline{\text{QA\_OE}}, \overline{\text{QB\_OE}}$ | Input (LVCMOS)       | Low enables outputs, High selects high impedance mode. Internal 100K-Ohm pulldown                                                  |
| 14                     | V <sub>DD</sub> _OSC                                 | Power                | Power for xtal Osc core                                                                                                            |
| 5                      | V <sub>DD</sub> _PLL                                 | Power                | Power for digital portion of PLL circuitry                                                                                         |
| 22, 29                 | V <sub>DD</sub> _Out                                 | Power                | Power for output buffers                                                                                                           |
| 32                     | V <sub>DDA</sub> _PLL                                | Power                | Power for analog core of PLL                                                                                                       |
| 19, 25                 | GND                                                  | Power                | Ground                                                                                                                             |
| 18                     | QA_CMOS                                              | Output (LVCMOS)      | 100MHz LVCMOS Output                                                                                                               |
| 16                     | QB_CMOS                                              | Output (LVCMOS)      | 100/50MHz Selectable LVCMOS Output                                                                                                 |
| 17                     | V <sub>DD</sub> _OutA_SE                             | Power                | Bank A LVCMOS Power                                                                                                                |
| 15                     | V <sub>DD</sub> _OutB_SE                             | Power                | Bank B LVCMOS Power                                                                                                                |
| 4                      | QB_DIV2                                              | Input (LVCMOS)       | High selects 50MHz, Low selects 100MHz. Internal 100K-Ohm pull-up                                                                  |
| 28                     | I <sub>REF</sub>                                     | Output               | External resistor connection for internal current reference                                                                        |
| 8                      | V <sub>DD</sub> _REF_OUT                             | Power                | Power for reference output                                                                                                         |
| 2                      | $\overline{\text{REF\_OUT\_OE}}$                     | Input (LVCMOS)       | Low enables outputs, High selects high impedance mode. Internal 100K-Ohm pull-down.                                                |
| 31                     | V <sub>DD</sub>                                      | Power                | Power for Core                                                                                                                     |

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature..... -65°C to +155°C  
 3.3V Analog Supply Voltage..... -0.5 to +4.6V  
 ESD Protection (HBM) ..... 2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Operating Conditions** (Over Operating Conditions)

| Symbol                     | Parameters                                 | Conditions                                       | Min. | Max. | Units |
|----------------------------|--------------------------------------------|--------------------------------------------------|------|------|-------|
| V <sub>DD_PLL</sub>        | PLL Power Supply Voltage                   |                                                  | 2.8  | 3.6  | V     |
| V <sub>DD_REF_Out</sub>    | Power Supply for Reference Out             |                                                  | 2.9  | 3.6  |       |
| V <sub>DD_OSC</sub>        | Power Supply Voltage for oscillator core   |                                                  | 2.8  | 3.6  |       |
| V <sub>DD_OutA, OutB</sub> | Power Supply Voltage for Bank A and Bank B |                                                  | 2.9  | 3.6  |       |
| V <sub>DD_Out</sub>        | Power Supply Voltage for Output Buffer     |                                                  | 2.9  | 3.6  |       |
| V <sub>DD</sub>            | 3.3V General Power Supply Voltage          |                                                  | 2.9  | 3.6  |       |
| V <sub>DDA_PLL</sub>       | Analog PLL Power Supply Voltage            |                                                  | 2.8  | 3.6  |       |
| T <sub>A</sub>             | Ambient Temperature                        |                                                  | -40  | 85   | °C    |
| I <sub>DD_PLL</sub>        | PLL Power Supply Current                   | At 3.6V, loaded                                  |      | 10   | mA    |
| I <sub>DD_REF_OUT</sub>    | Current for Reference Out                  | At 3.6V, loaded                                  |      | 36   |       |
| I <sub>DD_OSC</sub>        | Current for Oscillator                     | At 3.6V, loaded                                  |      | 12   |       |
| I <sub>DD_OUTA, OUTB</sub> | Current for Bank A and Bank B              | At 3.6V, loaded                                  |      | 11   |       |
| I <sub>DD_OUT</sub>        | Current for Output Buffer                  | At 3.6V, loaded                                  |      | 76   |       |
| I <sub>DDA_PLL</sub>       | Analog PLL Current, V <sub>DDA_PLL</sub>   | At 3.6V, loaded                                  |      | 35   |       |
| I <sub>DD</sub>            | Total Power Supply Current                 | No load (Analog PLL Current Included)            |      | 85   |       |
|                            |                                            | All outputs loaded (Analog PLL Current Included) |      | 180  |       |
| P <sub>Diss</sub>          | Power Dissipation                          | All outputs loaded                               |      | 0.65 | W     |

**LVCMOS DC Electrical Characteristics** (Over Operating Conditions)

| Symbol          | Parameters                                                   | Conditions                        | Min.                  | Typ. | Max.                  | Units |
|-----------------|--------------------------------------------------------------|-----------------------------------|-----------------------|------|-----------------------|-------|
| V <sub>IH</sub> | Input High Voltage                                           |                                   | 2                     |      | V <sub>DD</sub> + 0.3 | V     |
| V <sub>IL</sub> | Input Low Voltage                                            |                                   | -0.3                  |      | 0.8                   |       |
| V <sub>OH</sub> | Output High Voltage                                          | I <sub>OH</sub> = -8mA            | V <sub>DD</sub> - 0.4 |      |                       |       |
| V <sub>OL</sub> | Output Low Voltage                                           | I <sub>OL</sub> = 8mA             |                       |      | 0.4                   |       |
| I <sub>IH</sub> | Input High Current for<br>QA_OE, QB_OE, REF_OUT_OE, PLL_Byps | V <sub>IN</sub> = V <sub>DD</sub> |                       |      | 45                    | μA    |
|                 | IN_SEL, QB_DIV2                                              |                                   |                       |      | 5                     |       |
| I <sub>IL</sub> | Input Low Current for<br>QA_OE, QB_OE, REF_OUT_OE, PLL_Byps  | V <sub>IN</sub> = 0V              | -5                    |      |                       |       |
|                 | IN_SEL, QB_DIV2                                              |                                   | -45                   |      |                       |       |
| R <sub>pu</sub> | Internal pull up resistance                                  |                                   |                       | 105  |                       | kOhm  |
| R <sub>dn</sub> | Internal pull down resistance                                |                                   |                       | 105  |                       | kOhm  |
| Z <sub>O</sub>  | Output Impedance                                             |                                   |                       | 30   |                       | Ohm   |
| C <sub>IN</sub> | Input Capacitance for X1, X2 inputs                          |                                   |                       | 4    |                       | pF    |

**LVCMOS AC Characteristics** (Over Operating Conditions)

| Symbol                         | Parameter                           | Conditions                                                                                                                                          | Min. | Typ. | Max. | Units |
|--------------------------------|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| f <sub>error</sub>             | Frequency Synthesis Error           |                                                                                                                                                     |      |      | 0    | ppm   |
| T <sub>r</sub> /T <sub>f</sub> | Output Rise/Fall time               | 20% to 80%, C <sub>L</sub> = 10pF                                                                                                                   |      | 1.2  | 2    | ns    |
| T <sub>DC</sub>                | Output Duty Cycle                   | t <sub>DC</sub> = t <sub>H</sub> /t <sub>CY</sub> , t <sub>H</sub> = High Pulse Width,<br>t <sub>CY</sub> = Output Cycle Time, @ V <sub>DD</sub> /2 | 45   | 50   | 55   | %     |
| J <sub>CC</sub>                | Jitter, Cycle-to-Cycle              |                                                                                                                                                     |      |      | 175  | ps    |
| J <sub>phase</sub>             | Rms Phase jitter from 12kHz - 20MHz |                                                                                                                                                     |      | 0.4  | 1    |       |
| T <sub>EN/DIS</sub>            | Output enable/disable time          |                                                                                                                                                     |      |      | 80   | ns    |
| T <sub>LOCK</sub>              | PLL Lock Time                       |                                                                                                                                                     |      |      | 5    | ms    |

**Differential DC Input Characteristics** (Over Operating Conditions)

| Symbol           | Parameters                       | Conditions | Min.                                       | Typ. | Max.                    | Units |
|------------------|----------------------------------|------------|--------------------------------------------|------|-------------------------|-------|
| I <sub>IH</sub>  | Input High Current               | IN-        | V <sub>IN</sub> = V <sub>DD</sub> = 3.465V |      | 5                       | uA    |
|                  |                                  | IN+        | V <sub>IN</sub> = V <sub>DD</sub> = 3.465V |      | 45                      |       |
| I <sub>IL</sub>  | Input Low Current                | IN-        | V <sub>IN</sub> = 0V                       | -45  |                         |       |
|                  |                                  | IN+        | V <sub>IN</sub> = 0V                       | -5   |                         |       |
| V <sub>CMR</sub> | Common Mode Voltage Range        |            | 0.5                                        |      | V <sub>DD</sub> - 0.85V | V     |
| V <sub>PP</sub>  | Peak-to-Peak Input Voltage Swing |            | 0.15                                       |      | 1.3                     |       |

**HCSL DC Electrical Characteristics** (Over Operating Conditions)

| Symbol               | Parameters                                                                  | Condition                                                    | Min. | Typ. | Max. | Units |
|----------------------|-----------------------------------------------------------------------------|--------------------------------------------------------------|------|------|------|-------|
| V <sub>OH</sub>      | Output High Voltage                                                         | V <sub>DD_OUT</sub> = V <sub>DD</sub> - 0.15V <sup>(1)</sup> | 660  |      | 900  | mV    |
| V <sub>OL</sub>      | Output Low Voltage                                                          |                                                              |      |      | 150  |       |
| V <sub>CROSS</sub>   | Absolute Crossing Point Voltages                                            |                                                              | 250  |      | 550  |       |
| D V <sub>CROSS</sub> | Total variation of V <sub>CROSS</sub> overall edges                         |                                                              |      |      | 140  |       |
| I <sub>OH</sub>      | Output High Current w/ 475-Ohm resistor. Connected between IREF pin and GND |                                                              |      | 14   |      | mA    |

**Note:**

1. This voltage drop is to account for the voltage across the series resistor in the layout guidelines.

**HCSL AC Output Switching Characteristics(1,2,3)** (Over Operating Conditions)

| Symbol                                  | Parameters                                                          | Min | Typ | Max. | Units | Notes |
|-----------------------------------------|---------------------------------------------------------------------|-----|-----|------|-------|-------|
| f <sub>error</sub>                      | Frequency Synthesis Error                                           |     |     | 0    | ppm   |       |
| T <sub>rise</sub> / T <sub>fall</sub>   | Rise and Fall Time (measured between 0.175V to 0.525V)              | 175 | 250 | 700  | ps    | 2     |
| ΔT <sub>rise</sub> / ΔT <sub>fall</sub> | Rise and Fall Time Variation                                        |     | 7   | 125  |       | 2     |
| T <sub>skew</sub>                       | Output-to-Output Skew                                               |     | 20  | 100  |       | 3     |
| T <sub>DC</sub>                         | Duty Cycle (Measured at 100 MHz)                                    | 47  | 50  | 53   | %     | 3     |
| J <sub>phase</sub>                      | RMS phase jitter from 12kHz - 20MHz                                 |     | 0.4 | 1    | ps    | 2     |
| T <sub>HF-RMS</sub>                     | >1.5MHz - 50MHz RMS jitter applying PCIE G2 jitter mask             |     | 2.2 | 3.1  |       | 3     |
| PSR                                     | Power Supply Rejection with -30dBm input sine wave 100kHz to 600kHz |     | -46 |      | dBc   | 2     |
| T <sub>EN/DIS</sub>                     | Output enable/disable time                                          |     |     | 80   | ns    |       |
| T <sub>LOCK</sub>                       | PLL Lock Time                                                       |     |     | 5    | ms    |       |

**Notes:**

1. Test configuration is RS = 33Ω, Rp = 49.9Ω with 2pF load.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.

**LVPECL DC Electrical Characteristics** (Over Operating Conditions)

| Symbol          | Parameters               | Condition                         | Min.                 | Typ. | Max.                 | Units |
|-----------------|--------------------------|-----------------------------------|----------------------|------|----------------------|-------|
| V <sub>PP</sub> | Output peak-peak Voltage | V <sub>DD_REF_Out</sub> = 3.3± 5% | 0.4                  | 0.7  | 1                    | V     |
| V <sub>OH</sub> | Output High Voltage      | V <sub>DD_REF_Out</sub> = 3.3± 5% | V <sub>DD</sub> -1.4 |      | V <sub>DD</sub> -0.9 |       |
| V <sub>OL</sub> | Output Low Voltage       | V <sub>DD_REF_Out</sub> = 3.3± 5% | V <sub>DD</sub> -2.0 |      | V <sub>DD</sub> -1.7 |       |

**AC LVPECL Switching Characteristics**

| Symbol                                | Parameters                 | Condition                | Min. | Typ. | Max. | Units |
|---------------------------------------|----------------------------|--------------------------|------|------|------|-------|
| T <sub>rise</sub> / T <sub>fall</sub> | Rise and Fall Time         | 20% to 80%, single-ended | 200  | 320  | 450  | ps    |
| T <sub>DC</sub>                       | Duty Cycle                 | Differential             | 47   | 50   | 53   | %     |
| T <sub>EN/DIS</sub>                   | Output enable/disable time |                          |      |      | 100  | ns    |

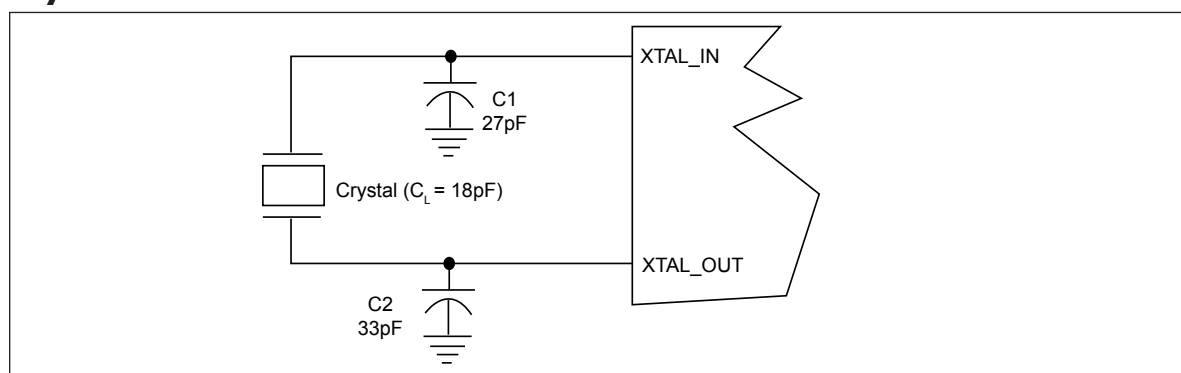
**Crystal Characteristic** (link to "<http://www.pericom.com/saronix>" for more detailed crystal specifications)

| Parameters         | Description                  | Min         | Typ | Max. | Units |
|--------------------|------------------------------|-------------|-----|------|-------|
| OSCmode            | Mode of Oscillation          | Fundamental |     |      |       |
| FREQ               | Frequency                    |             | 25  |      | MHz   |
| ESR <sup>(1)</sup> | Equivalent Series Resistance |             |     | 50   | Ohm   |
| Cload              | Load Capacitance             |             | 18  |      | pF    |
| Cshunt             | Shunt Capacitance            |             |     | 7    |       |
| DRIVE level        |                              |             |     | 1    | mW    |

Note: 1. ESR value is dependent upon frequency of oscillation

**Application Notes**
**Crystal circuit connection**

The following diagram shows PI6LC4830 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 33pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

**Crystal Oscillator Circuit**


## Recommended Crystal Specification

Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, [http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, [http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>

## HCSL output buffer characteristics

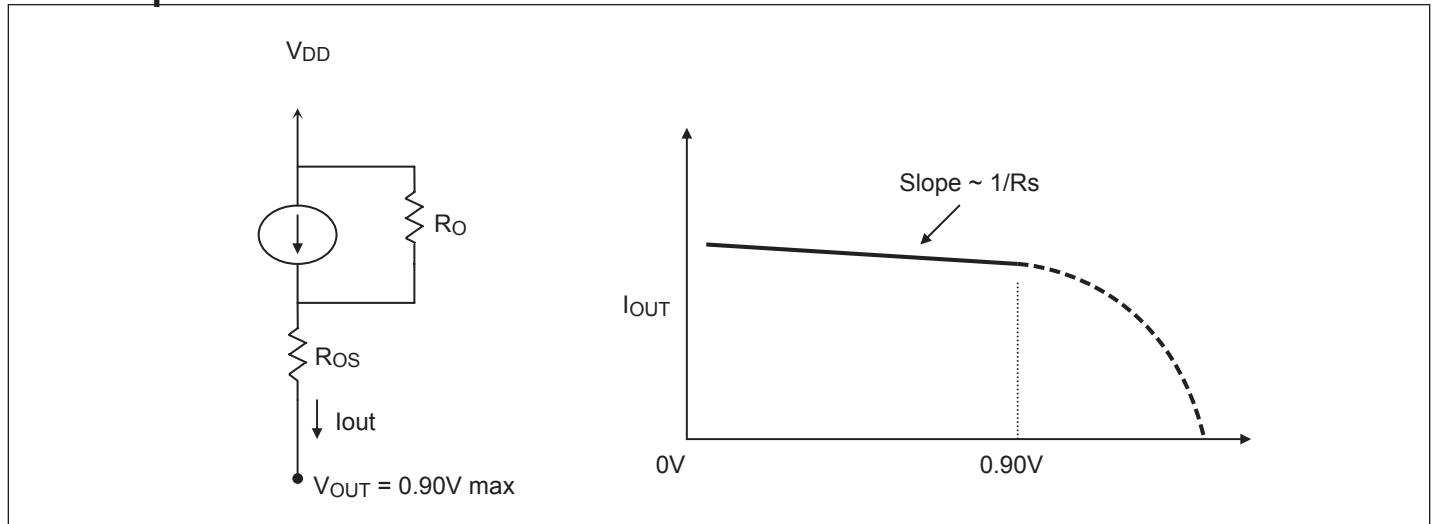


Figure 9. Simplified diagram of current-mode output buffer

## HCSL Buffer characteristics

| Symbol    | Minimum     | Maximum     |
|-----------|-------------|-------------|
| $R_O$     | 3000Ω       | N/A         |
| $R_{OS}$  | unspecified | unspecified |
| $V_{OUT}$ | N/A         | 900mV       |

## Current Accuracy (IREF pin)

| Symbol    | Conditions              | Configuration                                                   | Load                                      | Min.               | Max.               |
|-----------|-------------------------|-----------------------------------------------------------------|-------------------------------------------|--------------------|--------------------|
| $I_{OUT}$ | $V_{DD} = 3.30 \pm 5\%$ | $R_{REF} = 475\Omega \text{ } 1\%$<br>$I_{REF} = 2.32\text{mA}$ | Nominal test load for given configuration | -12% $I_{NOMINAL}$ | +12% $I_{NOMINAL}$ |

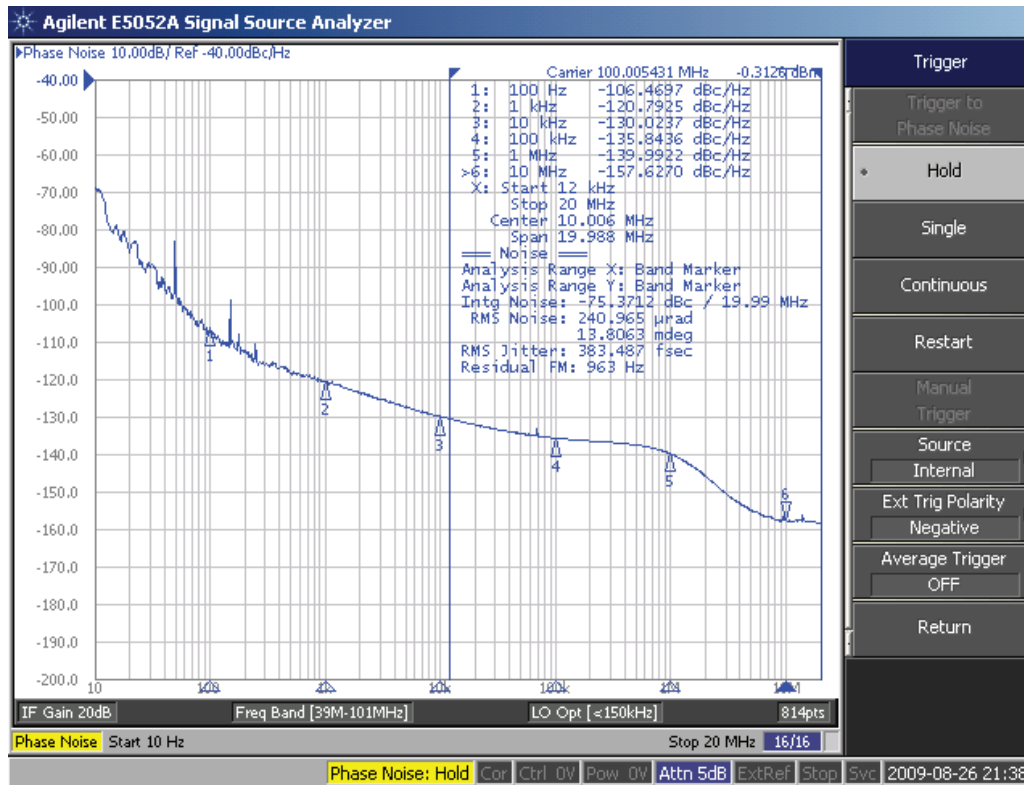
Note:

1.  $I_{NOMINAL}$  refers to the expected current based on the configuration of the device.

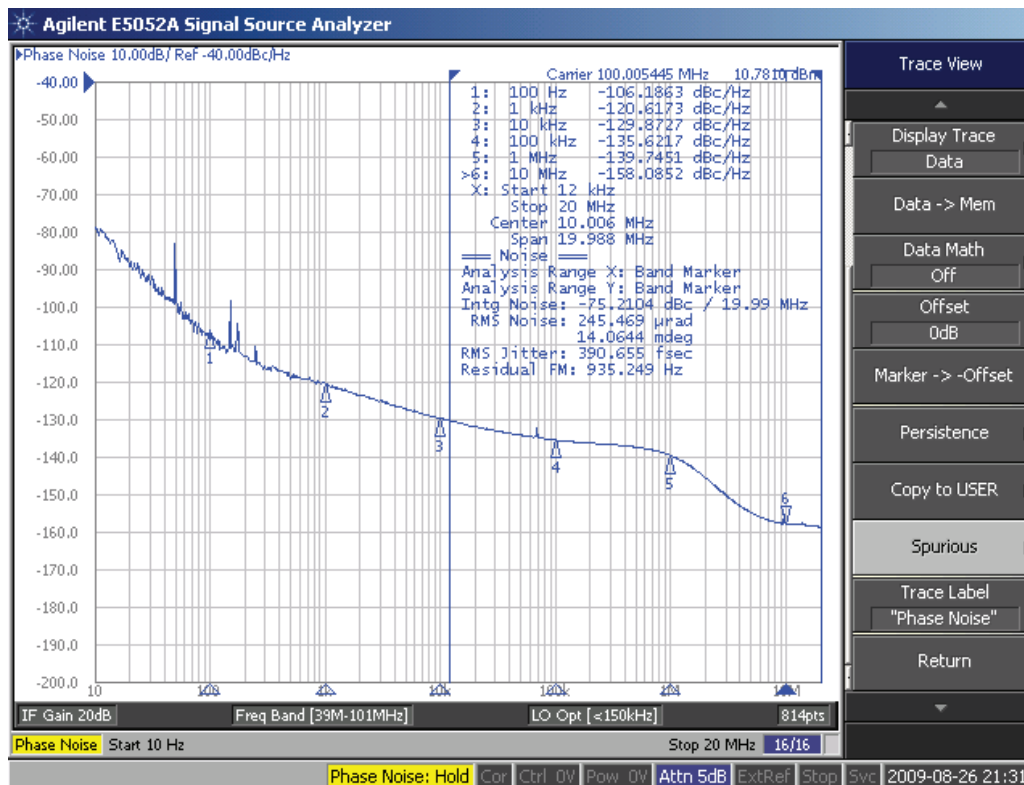
## Differential Clock Output Current

| Board Target Trace/Term Z                                | Reference R, $I_{ref} = V_{DD}/(3 \times R_r)$                    | Output Current              | $V_{OH} @ Z$ |
|----------------------------------------------------------|-------------------------------------------------------------------|-----------------------------|--------------|
| 100Ω<br>(100Ω differential $\approx$ 15% coupling ratio) | $R_{REF} = 475\Omega \text{ } 1\%$ ,<br>$I_{REF} = 2.32\text{mA}$ | $I_{OH} = 6 \times I_{REF}$ | 0.7V @ 50    |

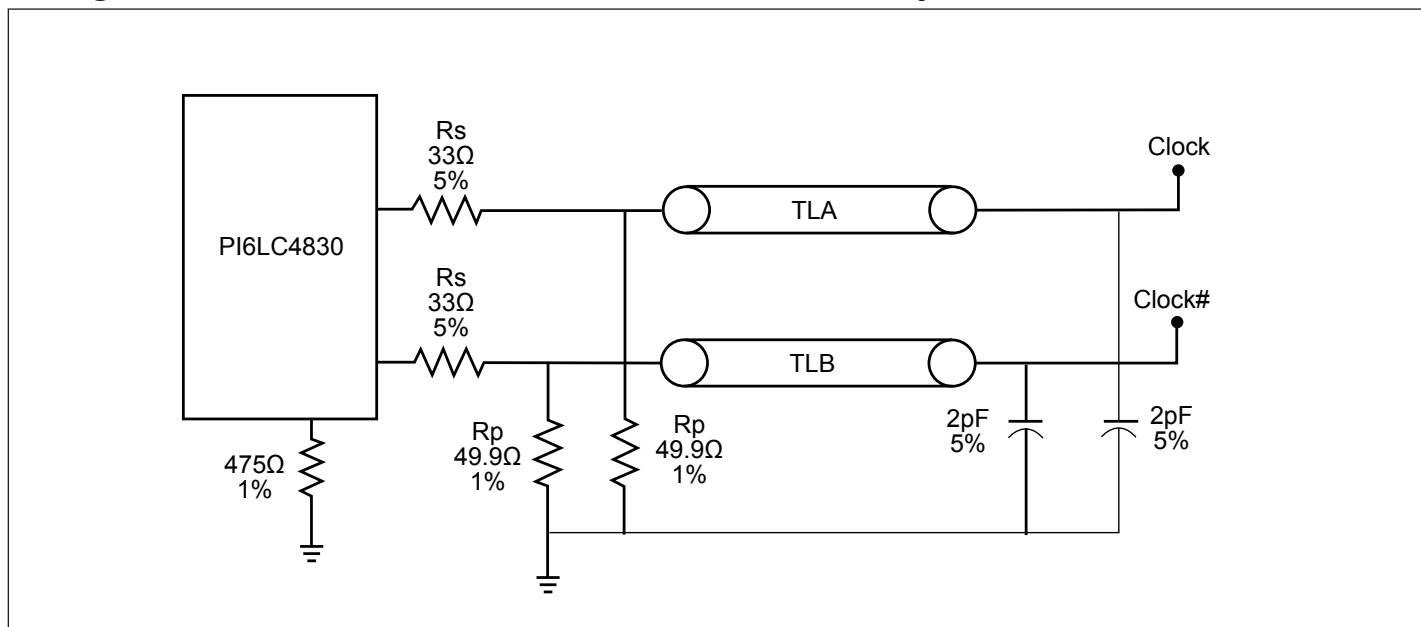
## Typical HCSL Output Phase Noise (3.3V, 25°C)



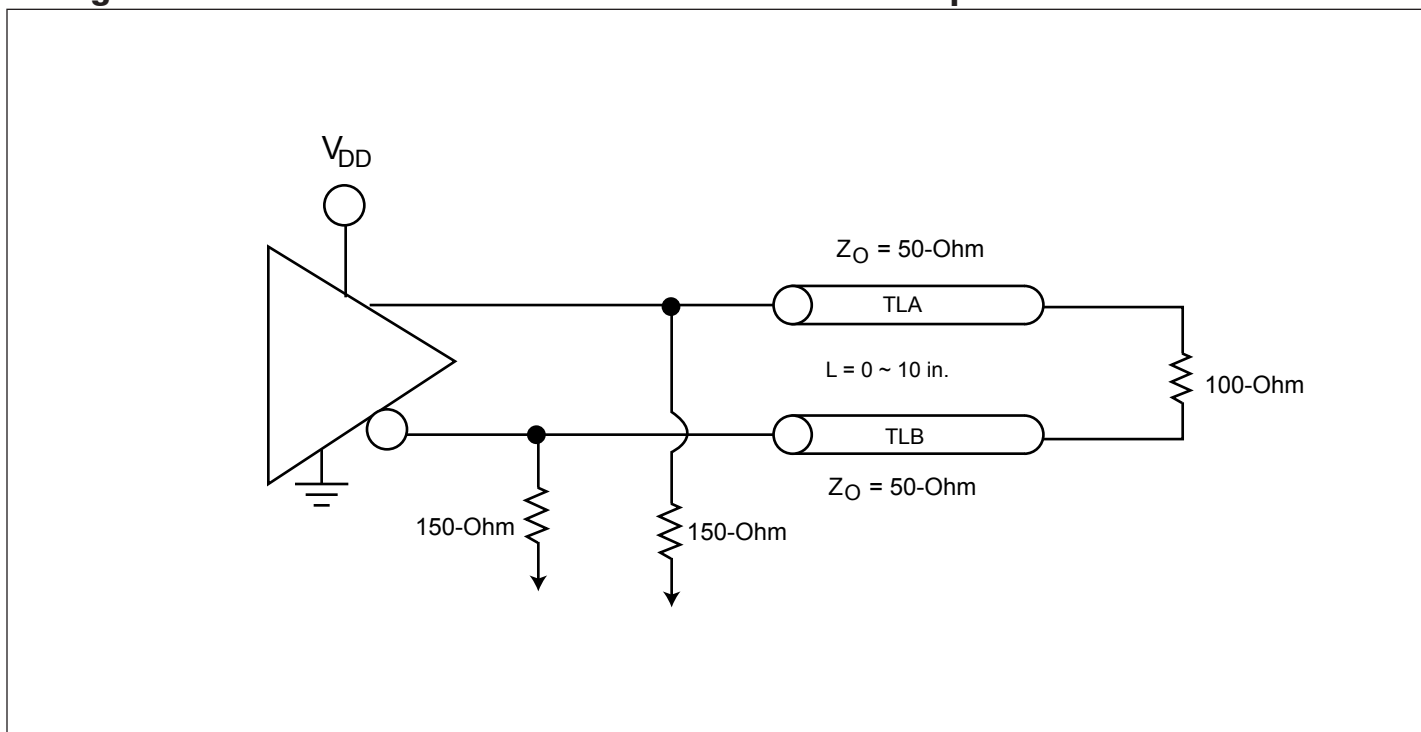
## Typical LVCMOS Output Phase Noise (3.3V, 25°C)



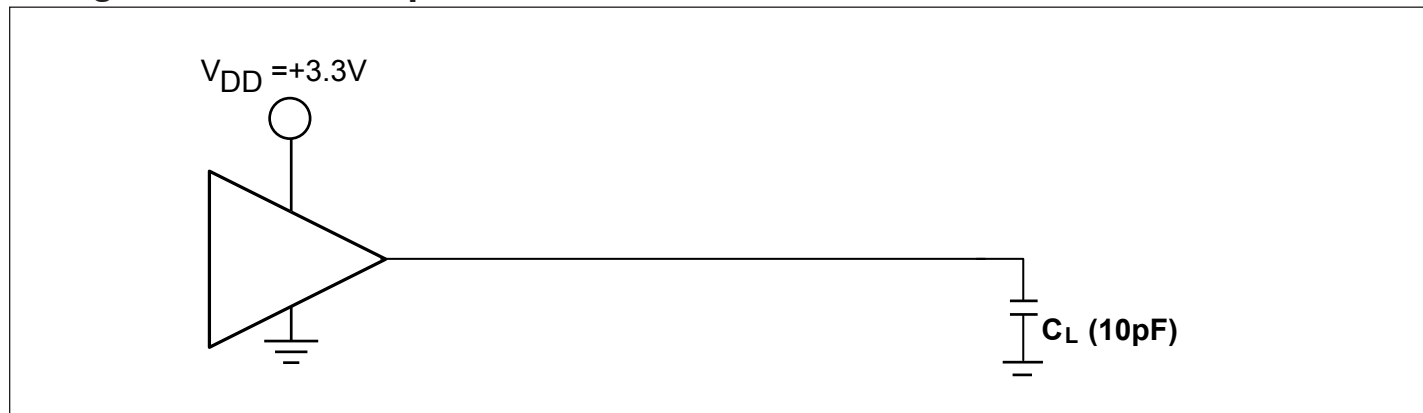
### Configuration Test Load Board Termination for HCSL outputs



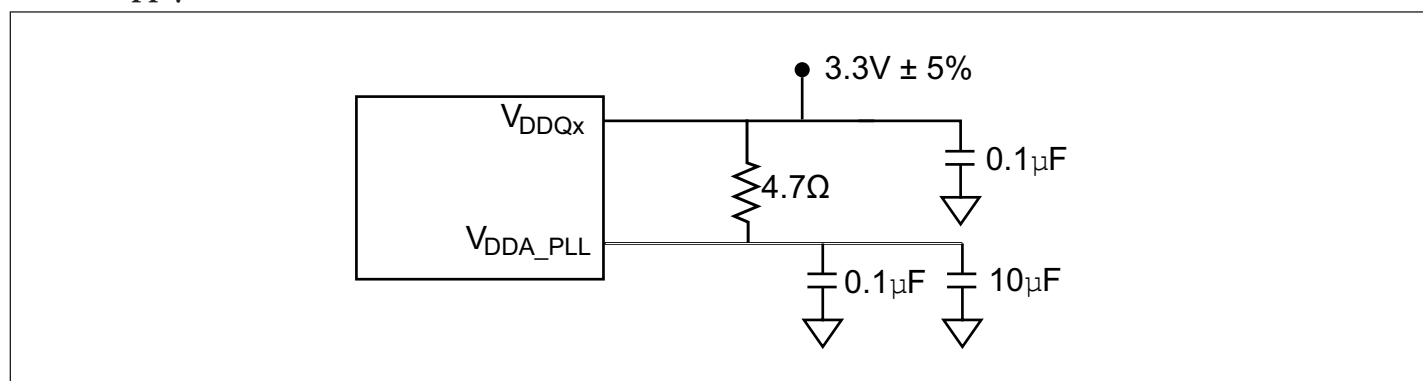
### Configuration Test Load Board Termination for LVPECL outputs



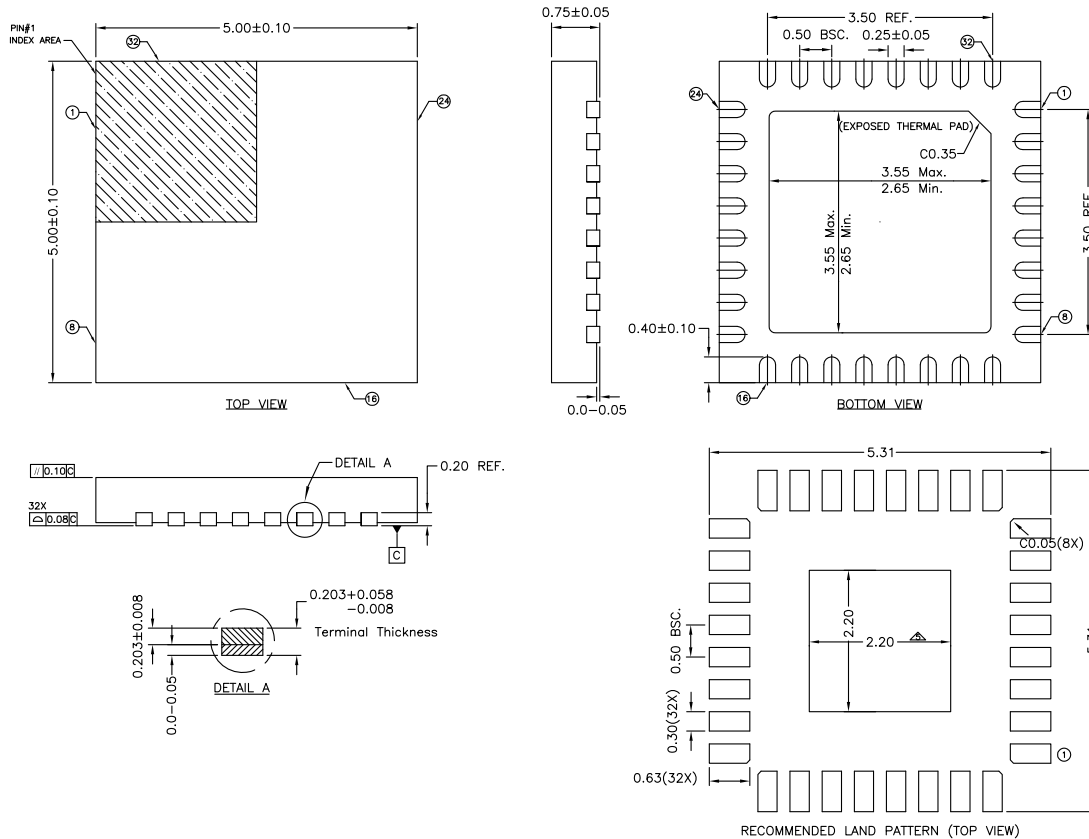
### Configuration CMOS Output



### Power Supply Filter



## Packaging Mechanical: 32-Pin TQFN (ZH)



### Notes:

1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area (mesh stencil design is recommended)



DATE: 06/30/11

DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH32

DOCUMENT CONTROL #: PD-2070

REVISION: B

11-0147

### Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

## Ordering Information<sup>(1-3)</sup>

| Ordering Code | Package Code | Package Description            |
|---------------|--------------|--------------------------------|
| PI6LC4830ZHE  | ZH           | 32-Pin, Pb-free & Green (TQFN) |

### Notes:

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel