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PI6LC48L0201A

2-Output LVDS Networking Clock Generator

Features

- Two differential LVDS output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 62.5MHz, 125MHz, 156.25MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz – 20MHz): 0.3ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz – 20MHz): 0.5ps (max)
- Full 3.3V or 2.5V supply modes
- Industrial operating temperature
- Available in lead-free package: 20-TQFN

Description

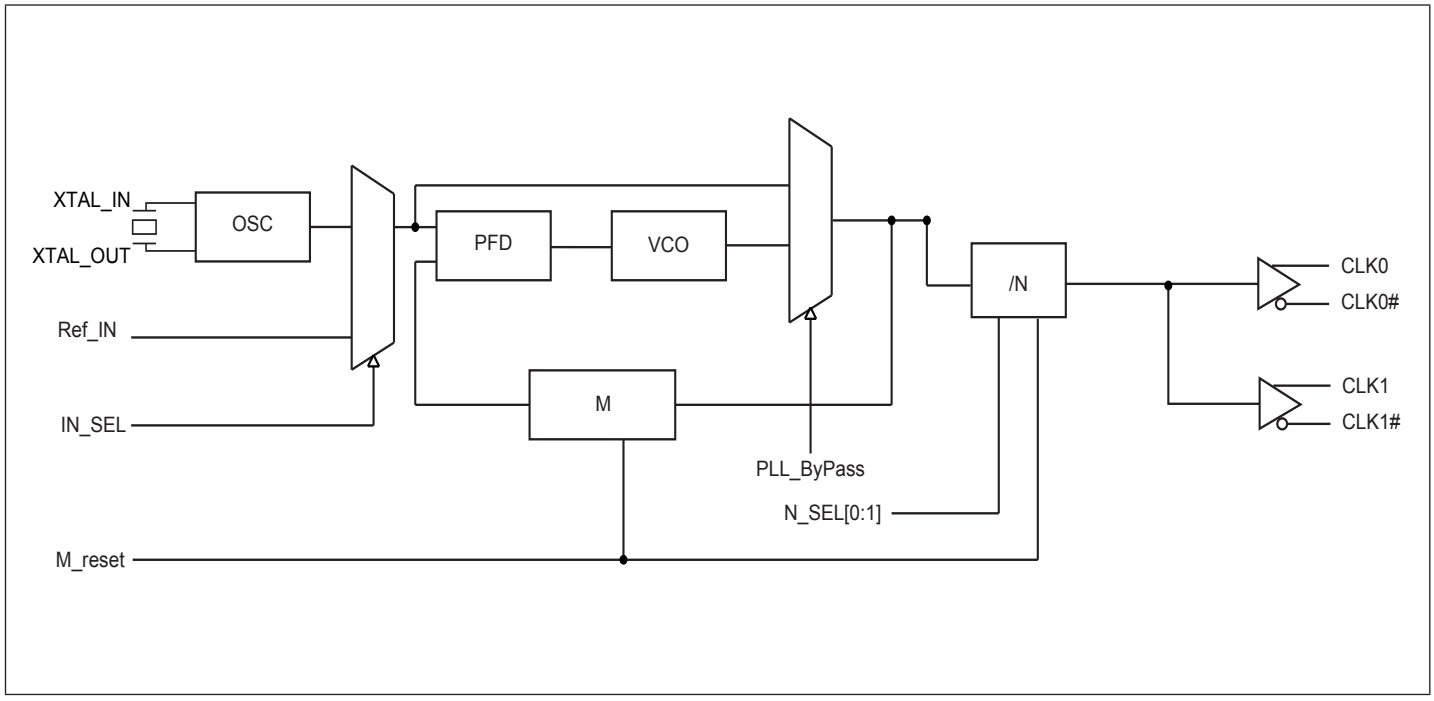
The PI6LC48L0201A is a 2-output LVDS synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 25MHz crystal, the most popular Ethernet frequencies can be generated based on the settings of 2 frequency select pins.

The PI6LC48L0201A uses Pericom's proprietary low phase noise PLL technology to achieve ultra low phase jitter, so it is ideal for Ethernet interface in all kind of systems.

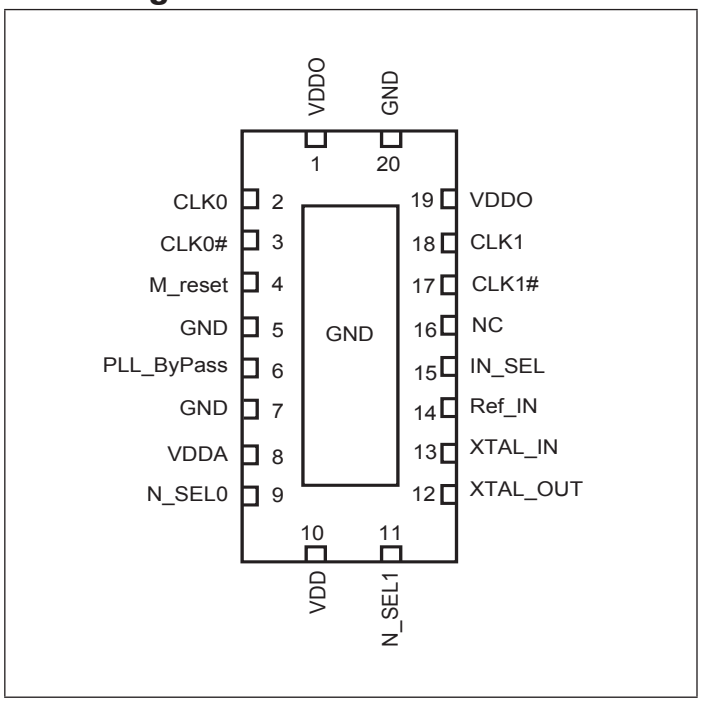
Applications

- Networking systems

Block Diagram



Pin Configuration



Pinout Table

Pin No.	Pin Name	I/O Type		Description
1, 19	VDDO	Power	-	Output Power Supply
2, 3	CLK0, CLK0#	Output	-	LVDS Output clock 0
4	M_reset	Input	Pull-down	Master reset. “1”, CLK0CLK1 go to “low”, CLK0#/CLK1# go to “high”; “0” outputs are enabled
5, 7, 20	GND	Ground	-	Ground
6	PLL_ByPass	Input	Pull-down	PLL bypass select. “0” PLL is enabled, “1” PLL is bypassed
8	VDDA	Power	-	Analog Power Supply
9, 11	N_SEL0, N_SEL1	Input	Pull-down	Output frequency select
10	VDD	Power	-	Core Power Supply
12, 13	XTAL_OUT, XTAL_IN	Crystal	-	Crystal input and output
14	Ref_IN	Input	Pull-down	CMOS reference clock input
15	IN_SEL	Input	Pull-down	“0” selects Crystal, “1” selects reference input
16	NC			No connection
17, 18	CLK1#, CLK1	Output	-	LVDS Output clock 1
Epad	GND	Ground	-	Ground

Output Frequency Selection Table

Xtal Frequency	N_SEL1 N_SEL0	Output Frequency
25	00	156.25
	01	125
	10	62.5
	11	Reserved

Typical Crystal Requirement

Parameter	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental		
Frequency	22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)			50	Ω
Shunt Capacitance			7	pF
Drive Level			1	mW

Recommended Crystal Specification

Pericom recommends:

a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

Maximum Ratings (Over operating free-air temperature range)

Storage Temperature..... -65°C to+155°C
Temperature with Power Applied .....-40°C to+85°C
Supply Voltage .....-0.5 to +3.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Power Supply DC Characterisitcs, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}, V_{DDA}, V_{DDO}	Supply Voltage		3.135	3.3	3.465	V
V_{DD}, V_{DDA}, V_{DDO}	Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	V_{DD} =V_{DDA} = V_{DDO} = 3.3V +/-5%			105	mA
		V_{DD} =V_{DDA} = V_{DDO} = 2.5V +/-5%			98	
I_{DDA}	Analog Supply Current	V_{DD} =V_{DDA} = V_{DDO} = 3.3V +/-5%			26	mA
		V_{DD} =V_{DDA} = V_{DDO} = 2.5V +/-5%			26	
I_{DDO}	Output Supply Current	V_{DD} =V_{DDA} = V_{DDO} = 3.3V +/-5%			55	mA
		V_{DD} =V_{DDA} = V_{DDO} = 2.5V +/-5%			55	

LVCMOS/LVTTL DC Characterisitcs, (T_A = -40°C to 85°C)

Symbol	Parameter		Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3 V +/- 5%	2		V_{DD}+ 0.3	V
			V_{DD} = 2.5 V +/- 5%	1.7		V_{DD}+ 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3 V +/- 5%	-0.3		0.8	V
			V_{DD} = 2.5 V +/- 5%	-0.3		0.7	V
I_{IH}	Input High Current		M_reset, PLL_ByPass, N_SEL[0:1], IN_SEL, Ref_IN V_{DD} = VIN = 3.465V			150	µA
I_{IL}	Input Low Current		M_reset, PLL_ByPass, N_SEL[0:1], IN_SEL, Ref_IN V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Pin Characterisitcs

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWNN}$	Pull down resistor			51		kΩ

LVDS DC Characterisitcs, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	V_{DD} = 3.3V	247		454	mV
		V_{DD} = 2.5V	247		454	
ΔV_{OD}	Change of V_{OD}	V_{DD} = 3.5V		50		mV
		V_{DD} = 2.5V		50		
V_{OS}	Output Offset Voltage	V_{DD} = 3.3V	1.125		1.375	V
		V_{DD} = 2.5V	1.125		1.375	
ΔV_{OS}	Change of V_{OS}	V_{DD} = 3.5V		50		mV
		V_{DD} = 2.5V		50		

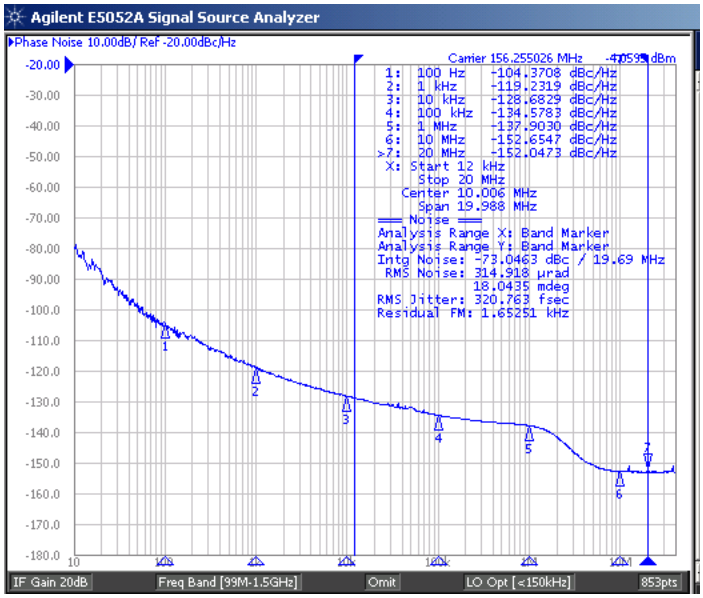
AC Electrical Characteristics, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
f_{OUT}	Output Frequency	N_SEL[1:0] = 00	140		170	MHz
		N_SEL[1:0] = 01	112		136	MHz
		N_SEL[1:0] = 10	56		68	MHz
$t_{sk(o)}$	Output Skew(1, 3)	Outputs @ same loading		50		ps
$t_{jit(Ø)}$	RMS Phase Jitter, (Random)(2)	156.25MHz, (1.875MHz - 20MHz)		0.15	0.3	ps
		156.25MHz, (12kHz - 20MHz)		0.3	0.5	ps
		125MHz, (1.875MHz - 20MHz)		0.15	0.3	ps
		125MHz, (12kHz - 20MHz)		0.3	0.5	ps
		62.5MHz, (1.875MHz - 20MHz)		0.32	0.5	ps
		62.5MHz, (12kHz - 20MHz)		0.4	0.7	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%			400	ps
odc	Output Duty Cycle		48		52	%

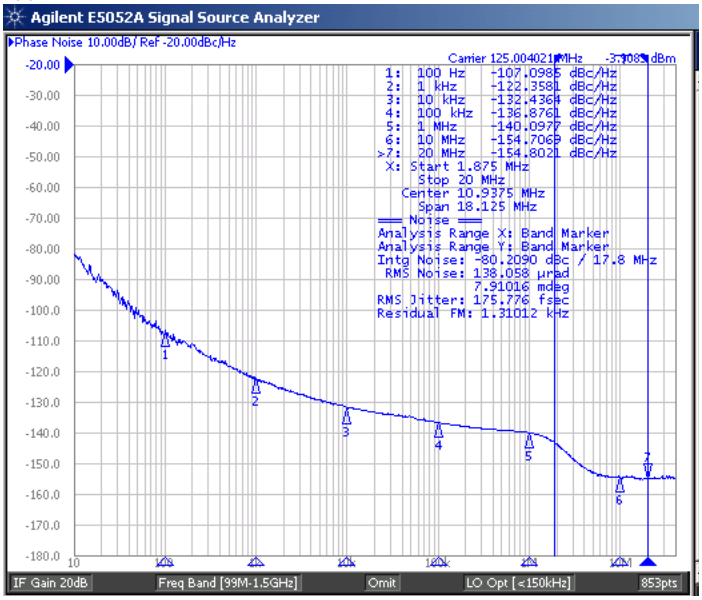
Note:
1. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
2. Please refer to the Phase Noise Plots.
3. This parameter is defined in accordance with JEDEC Standard 65.

Phase Noise Plots

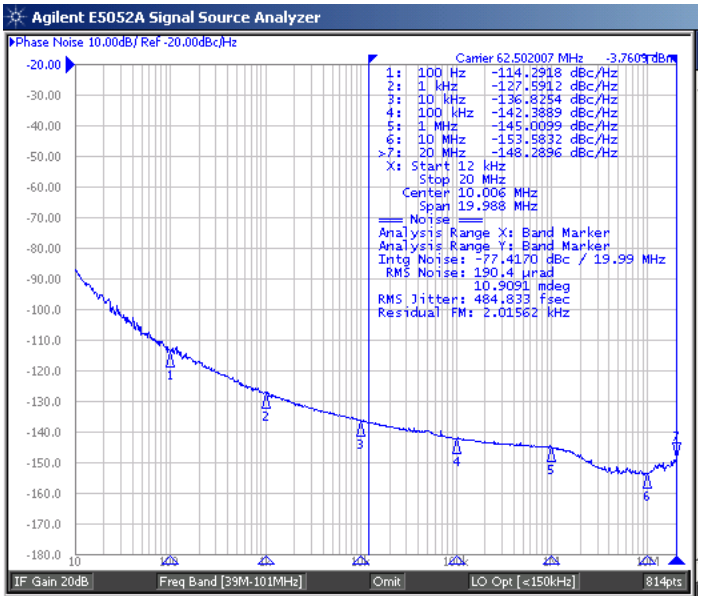
f_{OUT} = 156.25MHz



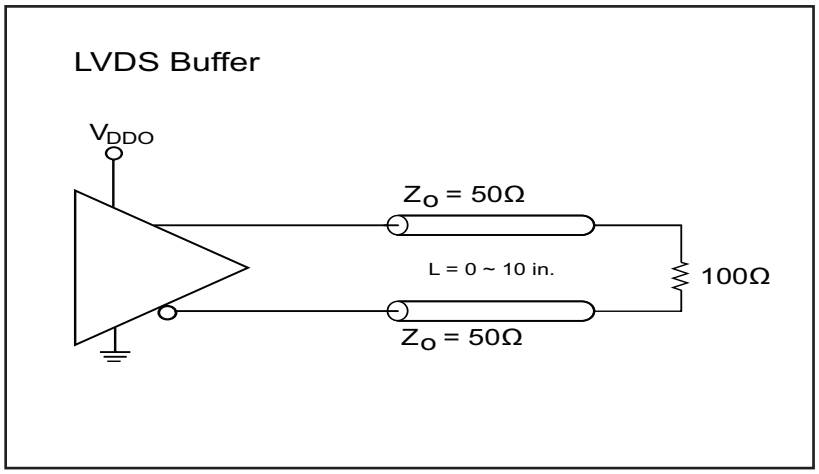
f_{OUT} = 125MHz



f_{OUT} = 62.5MHz

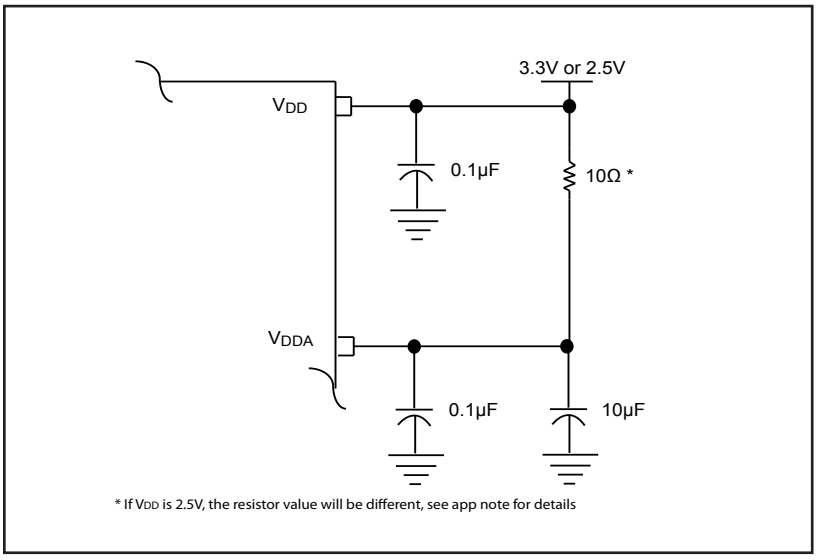


LVDS Test Circuit



Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48L0201A provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. A 1kΩ resistor can be tied from XTAL_IN to ground for additional protection.

Ref_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref_IN to ground can provide additional protection.

LVCMOS Control Pins:

All control pins have internal pulldowns; A 1kΩ resistor tied from each control pin to ground can provide additional protection.

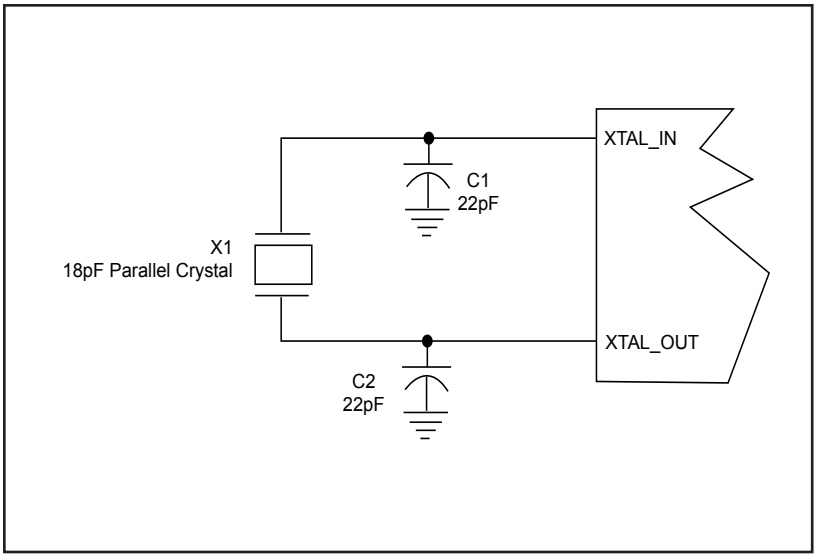
Outputs:

LVDS Outputs:

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

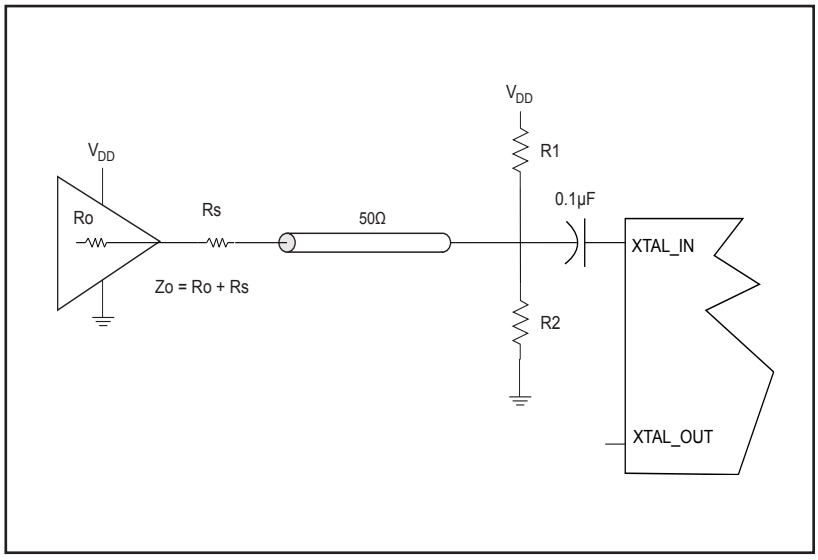
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



LVCMOS to XTAL Interface

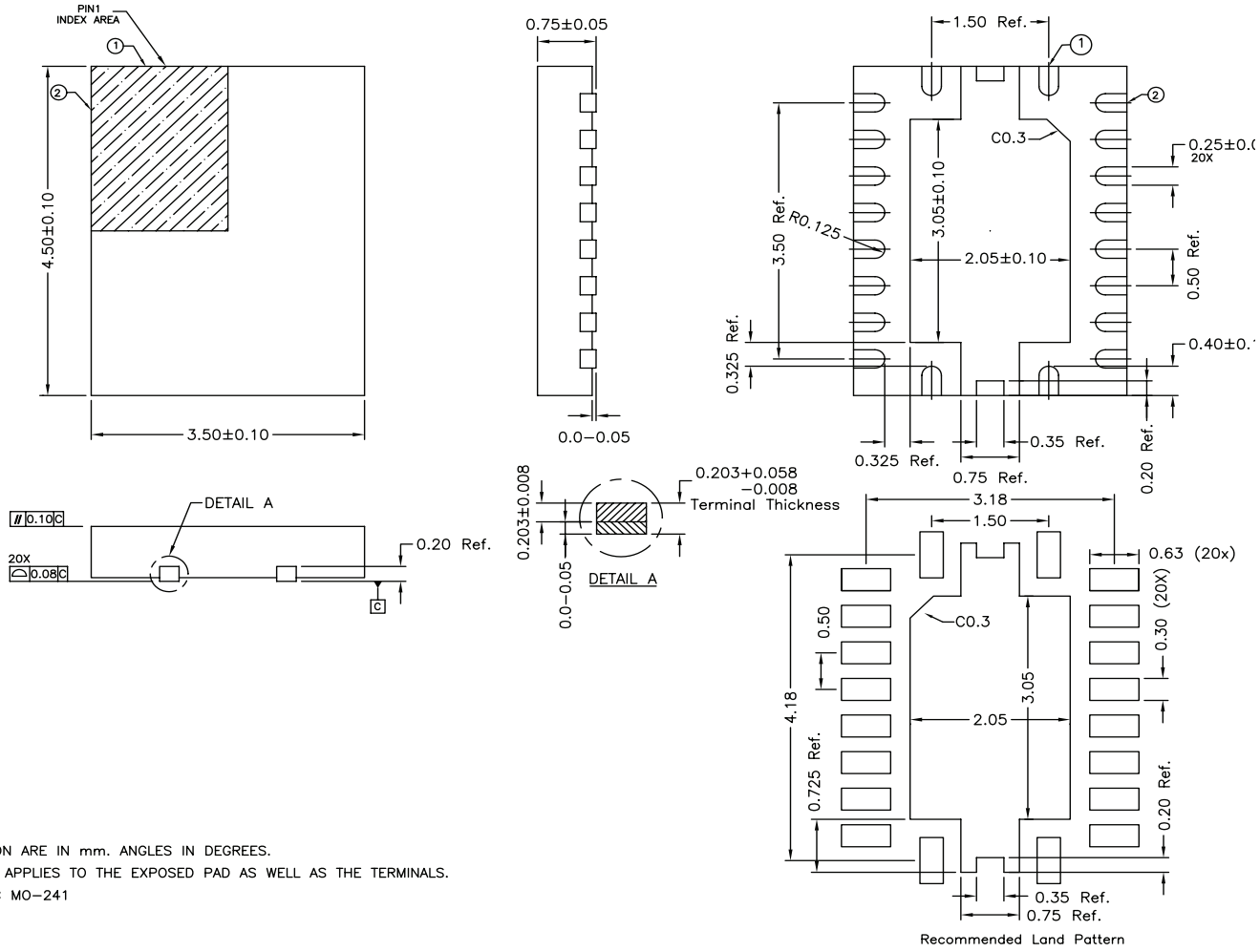
The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.



Thermal Information

Symbol	Description	
Θ_{JA}	Junction-to-ambient thermal resistance	19.80 °C/W
Θ_{JC}	Junction-to-case thermal resistance	8.10 °C/W

Packaging Mechanical: 20-Contact TQFN (ZH)



NOTE :
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–241

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48L0201AZHIE	ZH	Pb-free & Green, 20-pin TQFN	Industrial
PI6LC48L0201AZHIEX	ZH	Pb-free & Green, 20-pin TQFN, Tape & Reel	Industrial

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging