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Level Translating I²C Bus/SMBus Repeater

Features

- 2 channel, bidirectional buffer
- I²C-bus and SMBus compatible
- Port A operating supply voltage range of 0.8 V to 5.5 V
- Port B operating supply voltage range of 2.2 V to 5.5 V
- Voltage level translation from 0.8 V to 5.5 V and from 2.2 V to 5.5 V
- Active HIGH repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- 5.5 V tolerant I²C-bus and enable pins
- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ESD protection exceeds 8KV HBM per JESD22-A114
- Package: MSOP-8L, SOIC-8L and DFN2x3-8L

Description

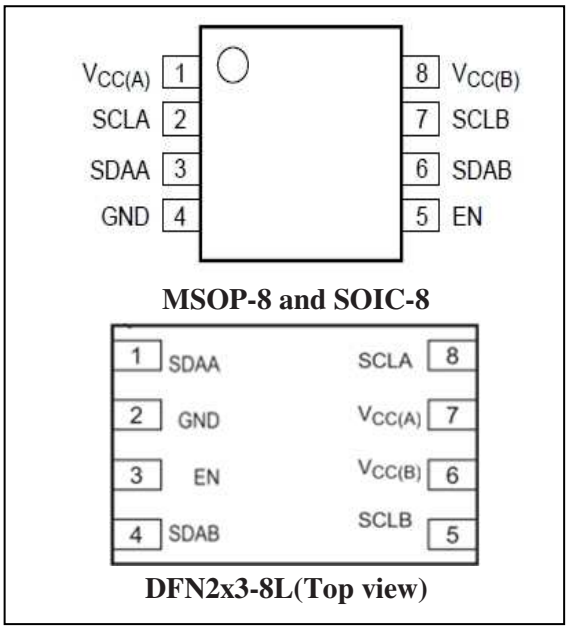
The PI6ULS5V9517A is a CMOS integrated circuit intended for I²C-bus or SMBus applications. It can provide level shifting between low voltage (down to 0.8 V) and higher voltage (2.2V to 5.5V) in mixed-mode applications. And it enables I²C and similar bus system to be extended, without degeradation of peformance even during level shifting.

The PI6ULS5V9517A enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I²C devices or longer trace length. It also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400 pF to be connected in an I²C application.

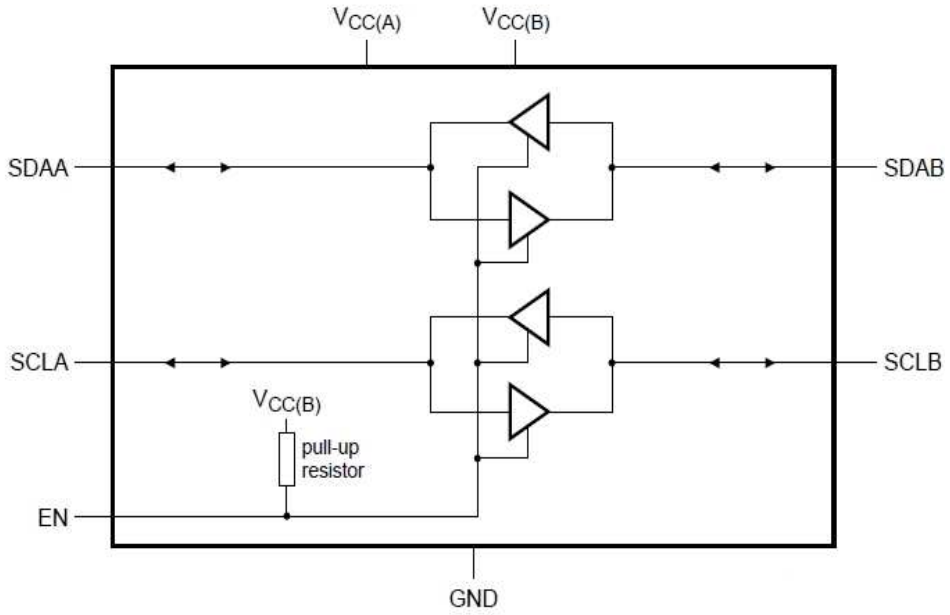
Pin Description

Pin No		Name	Description
MSOP-8 SOIC-8	DFN2x3-8L		
1	7	$V_{CC(A)}$	port A supply voltage (0.8 to 5.5 V)
2	8	SCLA	serial clock port A bus
3	1	SDAA	serial data port A bus
4	2	GND	supply ground (0 V)
5	3	EN	active HIGH repeater enable input
6	4	SDAB	serial data port B bus
7	5	SCLB	serial clock port B bus
8	6	$V_{CC(B)}$	port B supply voltage (2.2 to 5.5 V)

Pin Configuration



Block Diagram



EN	Function
H	SCLA = SCLB; SDAA = SDAB;
L	disabled

Figure 1: Block Diagram

Maximum Ratings

Storage Temperature	-55°C to +125°C
Supply Voltage port B	-0.5V to +6.0V
Supply Voltage port A	-0.5V to+6.0V
DC Input Voltage	-0.5V to +6.0V
Control Input Votage(EN)	-0.5V to+6.0V
Total Power Dissipation	100mA
Input/Output Current (portA&B)	50mA
Input Current (EN, $V_{CC(A)}$, $V_{CC(B)}$, GND)	50mA
ESD: HBM Mode	8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

V_{CC} = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CC(B)}$	supply voltage port B	-	2.2	-	5.5	V
$V_{CC(A)}$	supply voltage port A	-	0.8	-	5.5	V
$I_{CC(A)}$	supply current on pin $V_{CC(A)}$	-	-	-	500	µA
I_{CCH}	HIGH-level supply current	both channels HIGH; V_{CC} = 5.5 V; SDAn = SCLn = V_{CC}	-	0.5	2	mA
I_{CCL}	LOW-level supply current	both channels LOW; V_{CC} = 5.5 V; one SDA and one SCL = GND; other SDA and SCL open	-	0.5	2	mA
$I_{CC(B)c}$	contention port B supply current	V_{CC} = 5.5 V; SDAn = SCLn = V_{CC}	-	0.5	2	mA

DC Electrical Characteristics

V_{CC} = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage	-	$0.7V_{CC(B)}$	-	5.5	V
V_{IL} [1]	LOW-level input voltage	-	-0.5	-	$+0.3Vcc_{(B)}$	
V_{ILc}	contention LOW-level input voltage	-	-0.5	0.4	-	
V_{IK}	input clamping voltage	I_I = -18 mA	-	-	-1.2	V
I_{LI}	input leakage current	V_I = 3.6 V	-	-	±1	µA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V	-	10	-	µA
V_{OL}	LOW-level output voltage	I_{OL} = 100µA or 6 mA	0.47	0.52	0.6	V
V_{OL}-V_{ILc}	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design	-	70	-	mV
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V	-	-	10	µA
Cio	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V V_I = 3 V or 0 V; V_{CC} = 0 V	-	6	-	pF
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage	-	$0.7V_{CC(A)}$	-	5.5	V
V_{IL} [2]	LOW-level input voltage	-	-0.5	-	$+0.25V_{CC(A)}$	
V_{IK}	input clamping voltage	I_I = -18 mA	-	-	-1.2	V
I_{LI}	input leakage current	V_I = 3.6 V	-	-	±1	µA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V	-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA	-	0.1	0.2	V
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V	-	-	10	µA
Cio	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V V_I = 3 V or 0 V; V_{CC} = 0 V	-	6	-	pF
Enable						
V_{IH}	HIGH-level input voltage	-	$0.7V_{cc(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage	-	-0.5	-	$+0.3V_{cc(B)}$	V
I_{IL}	LOW-level input current	V_I = 0.2 V, EN; V_{CC} = 3.6 V	-	-10	-30	µA
I_{LI}	input leakage current	V_I=Vcc(B)	-1	-	+1	µA
Ci	input capacitance	V_I = 3.0 V or 0 V	-	6	-	pF

Notes:
1 V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{IL}c is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.
2, V_{IL} for port A with envelope noise must be below $0.3V_{CC(A)}$ for stable performance.

Dynamic characteristics

V_{CC} = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified. [1][2]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	LOW-to-HIGH propagation delay	B-side to A-side	-	169	255	ns
t_{PHL}	HIGH-to-LOW propagation delay	B-side to A-side, $V_{CC(A)} \leq 2.7$ V	15	68	110	ns
		B-side to A-side, $V_{CC(A)} \geq 3$ V	10	103	300	ns
t_{TLH}	LOW-to-HIGH transition time	A-side	-	50	60	ns
t_{THL}	HIGH-to-LOW transition time	A-side, $V_{CC(A)} \leq 2.7$ V	1	3	105	ns
		A-side, $V_{CC(A)} \geq 3$ V	1	25	175	ns
t_{PLH}	LOW-to-HIGH propagation delay	A-side to B-side	25	67	110	ns
t_{PHL}	HIGH-to-LOW propagation delay	A-side to B-side	-	118	230	ns
t_{TLH}	LOW-to-HIGH transition time	B-side	-	140	170	ns
t_{THL}	HIGH-to-LOW transition time	B-side	-	40	105	ns
t_{SU}	set-up time	EN HIGH before START condition	100	-	-	ns
t_H	hold time	EN HIGH after STOP condition	100	-	-	ns

Notes:
(1) Times are specified with loads of 1.35kΩ pull-up resistance and 57 pF load capacitance on port B, and 167Ω pull-up resistance and 57 pF load capacitance on port A. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.
(2) Pull-up voltages are $V_{CC(A)}$ on port A and $V_{CC(B)}$ on port B.
(3) Typical values were measured with $V_{CC(A)}$ = 3.3 V at Tamb = 25 , unless otherwise noted.

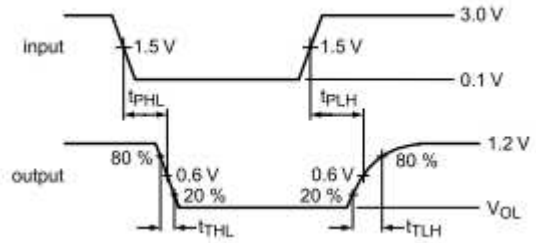


Figure 2: Propagation Delay and Transition Times B→A

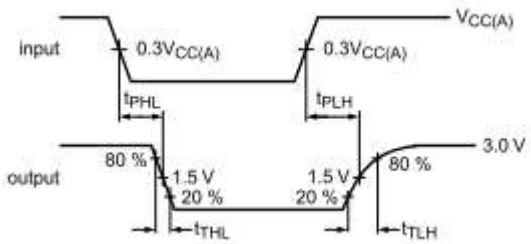


Figure 3: Propagation Delay and Transition Times A→B

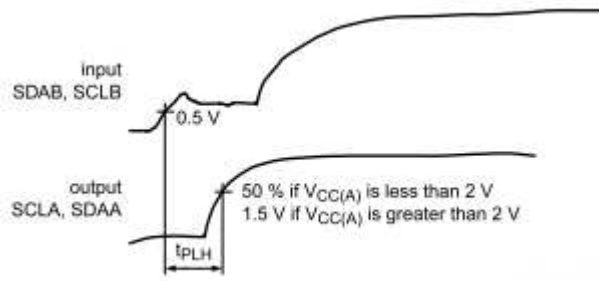
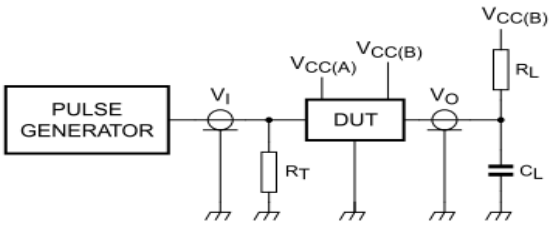


Figure 4: Propagation Delay



R_L=Load resistor: 1.35kΩ on port B; 167Ω on port A(0.8V to 2.7V) and 450Ω on port A (3.0V to 5.5V)
C_L = Load capacitance includes jig and probe capacitance: 57pF
R_T = Termination resistance should be equal to Z of pulse generators

Figure 5: Test Circuit

Functional Description

The PI6ULS5V9517A is a CMOS integrated circuit intended for I^2C-bus or SMBus applications. It can provide level shifting between low voltage (down to 0.8 V) and higher voltage (2.2 V to 5.5 V) in mixed-mode applications. And it enables I^2C and similar bus system to be extended, without degradation of performance even during level shifting.

The PI6ULS5V9517A enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I2C devices or longer trace length. It also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400 pF to be connected in an I^2C application.

The B-side drivers operate from 2.2 V to 5.5 V. The output low level of port B internal buffer is approximately 0.5 V, while the input voltage must be 70mV lower (0.43V) or even more lower. The nearly 0.5V low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design on B port prevents it from being used in series with another PI6ULS5V9517A (B side) or similar devices ,because they don't recognize buffer low signals as a valid low .

The A-side drivers operate from 0.8 V to 5.5 V. The output low level of port A internal buffer is nearly 0V,while the input low level is set at $0.3V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8 V. Port A of two or more PI6ULS5V9517As can be connected together to allow a star topography with port A on the common bus. And port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PI6ULS5V9517As can be connected in series, port A to port B, with no build-up in offset voltage with only time off light delays to consider.

The EN pin can also be used to turn the drivers on and off. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled. The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

After power-up and with the EN HIGH, a LOW level on port A (below $0.3V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.5 V. When port A rises above $0.3V_{CC(A)}$, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below $0.3V_{CC(B)}$ the port A driver is turned on and port A pulls down to 0 V. The port B pull-down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage does not go below 0.5 V, the port A driver will turn off when port B voltage is above $0.7V_{CC(B)}$. If the port B low voltage goes below 0.4 V, the port B pull-down driver is enabled and port B will only be able to rise to 0.5 V until port A rises above $0.3V_{CC(A)}$. Then port B will continue to rise being pulled up by the external pull-up resistor. The $V_{CC(A)}$ is only used to provide the $0.3V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PI6ULS5V9517A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

The EN pin is active high and allows the user to select when the repeater is active.This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled. The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

As with the standard I^2C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The PI6ULS5V9517A has standard open-collector configuration of the I^2C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I^2C devices in addition to SMBus devices. Standard mode I^2C devices only specify 3 mA in a generic I^2C system, where Standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

Application Information

A typical application is shown in Figure 6. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz.Master devices can be placed on either bus.

The PI6ULS5V9517A is 5V tolerant, so it does not require any additional circuitry to translate between 0.8V to 5.5V bus voltages and 2.2V to 5.5V bus voltages.

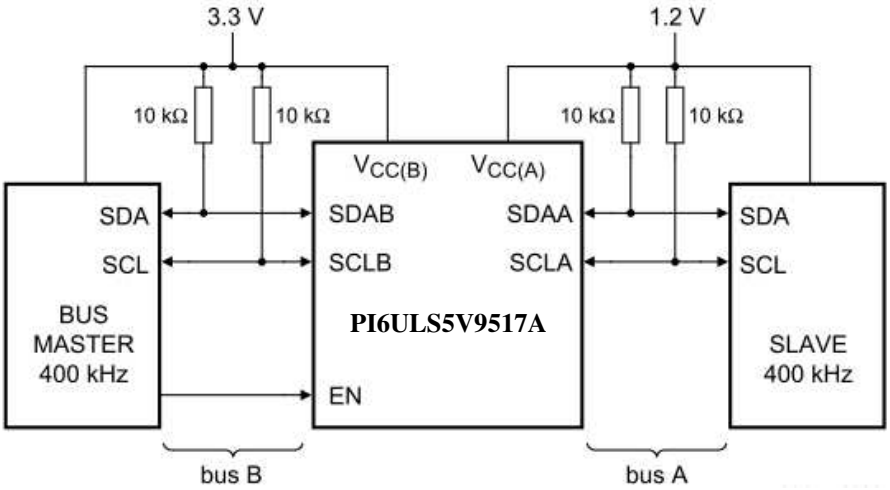


Figure 6:Typical Application

When port A of the PI6ULS5V9517A is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below 0.3 $V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PI6ULS5V9517A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 6 were to write to the slave through the PI6ULS5V9517A, waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 0.8 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the PI6ULS5V9517A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PI6ULS5V9517A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the PI6ULS5V9517A for a short delay, while the A-bus side rises above 0.3 $V_{CC(A)}$ and then it continues high.

Multiple PI6ULS5V9517A port A sides can be connected in a star configuration (Figure 7), allowing all nodes to communicate with each other.

Multiple PI6ULS5V9517As can be connected in series (Figure 8) as long as port A is connected to port B. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

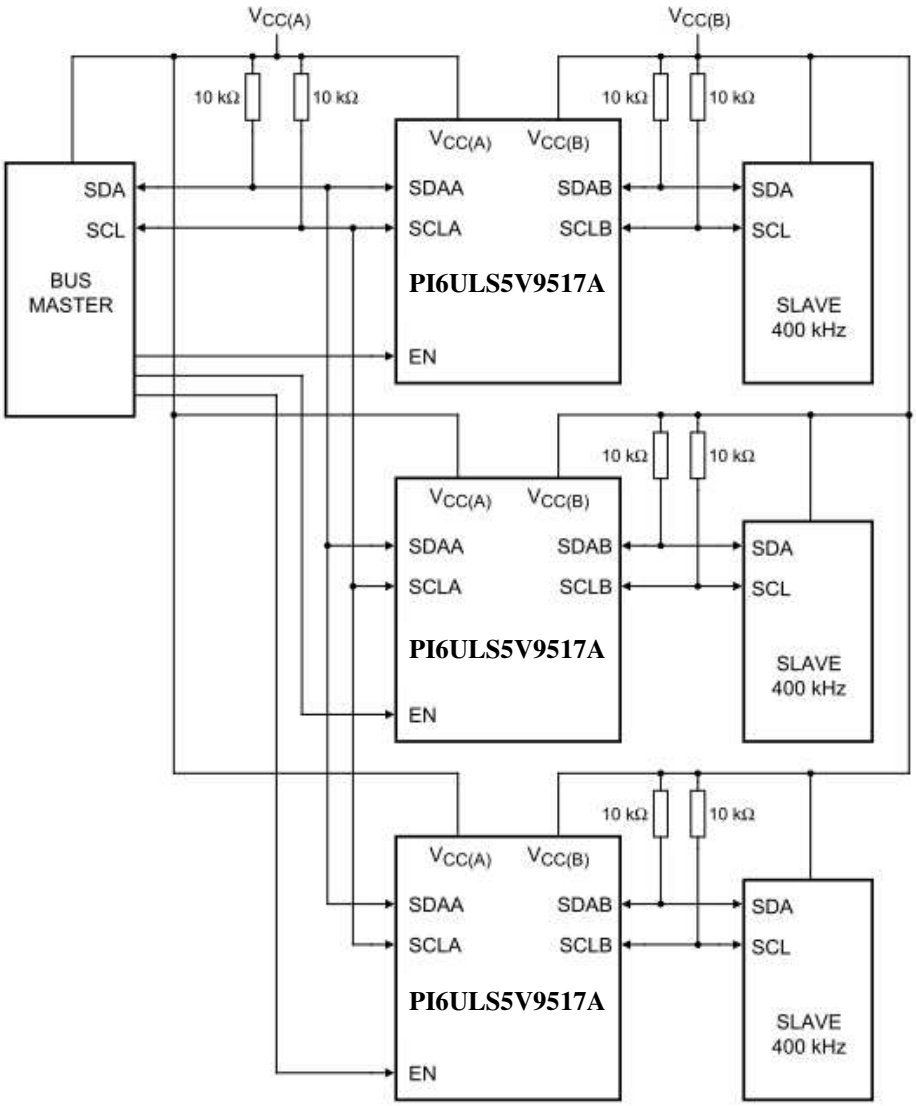


Figure 7:Typical Star Application

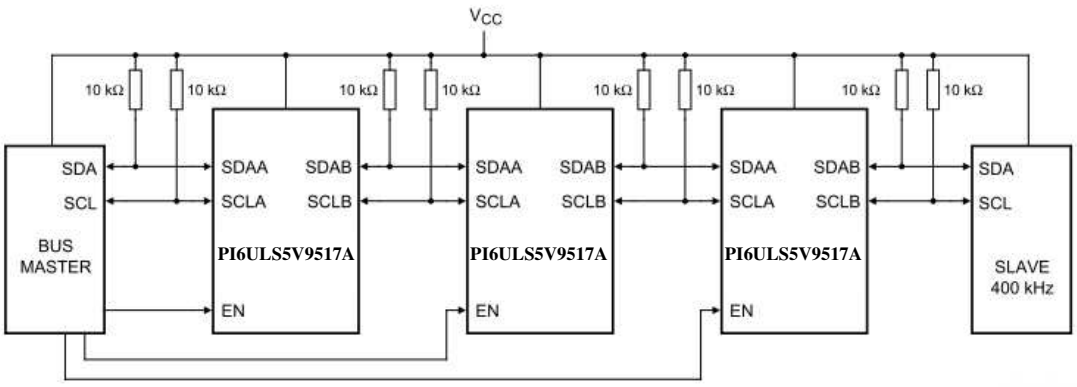


Figure 8:Typical Series Application

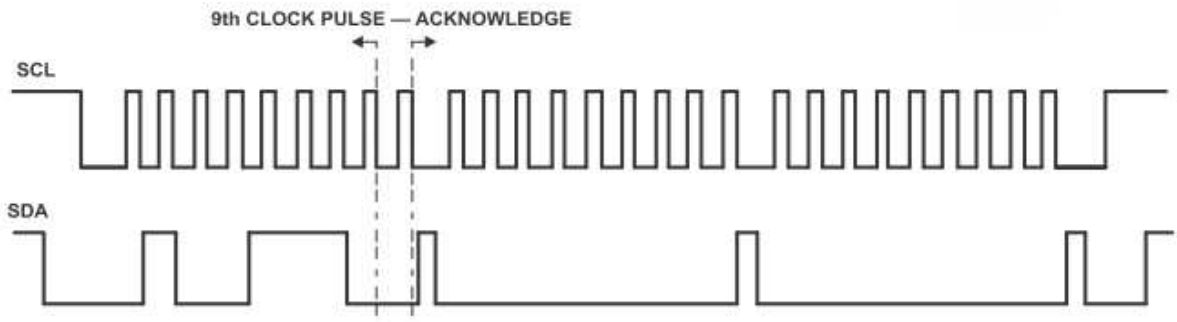


Figure 9: Bus A (0.8V to 5.5V Bus) Waveform

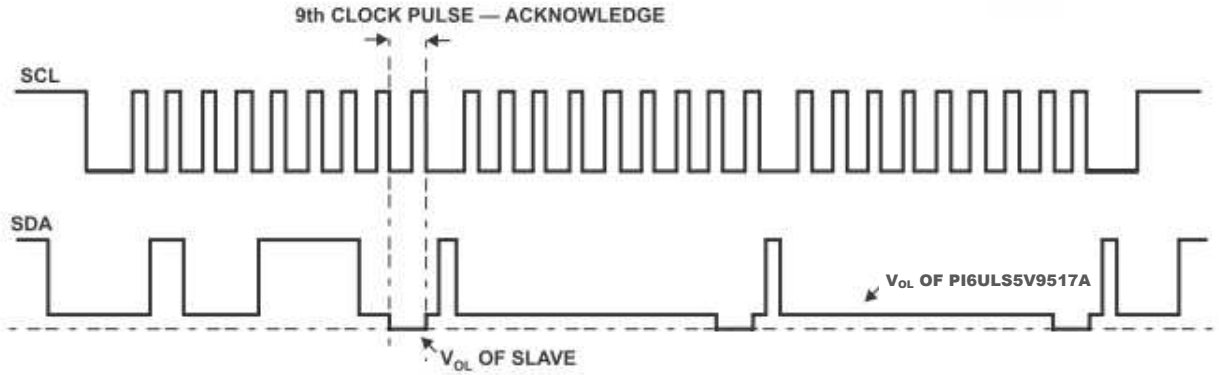
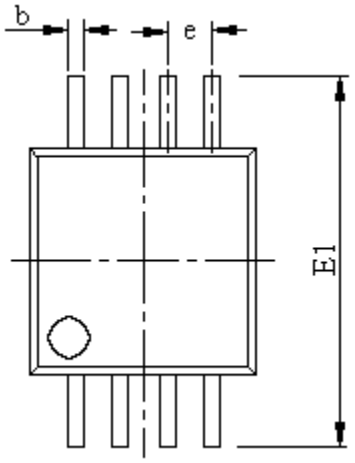
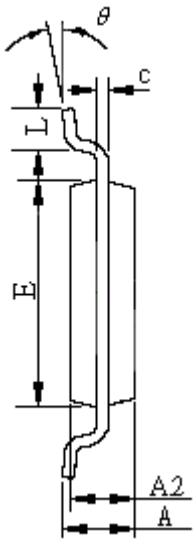


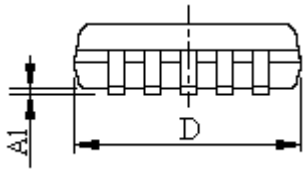
Figure 10: Bus B (2.2V to 5.5V Bus) Waveform

Mechanical Information

MSOP-8



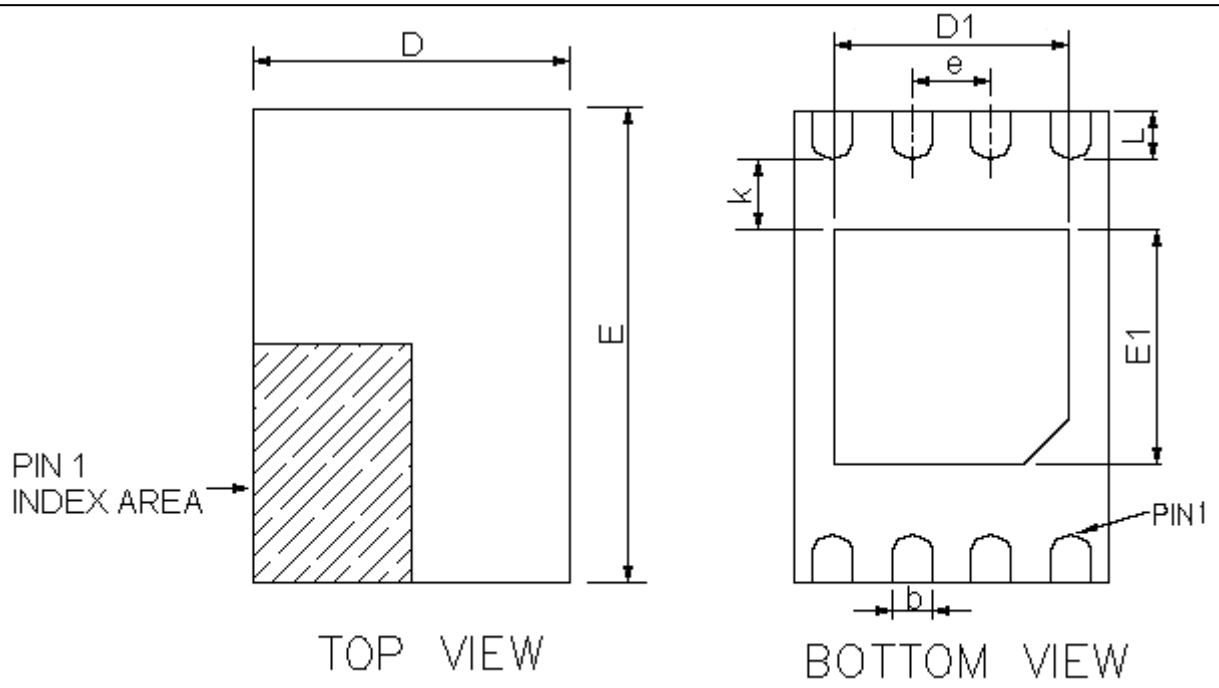




Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-187E/BA

Symbol	Dimensions In Millimeters	
	Min	Max
A	0.82	1.10
A1	0.02	0.15
A2	0.75	0.95
b	0.25	0.38
c	0.09	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.75	5.05
e	0.65 BSC	
L	0.40	0.80
θ	0°	6°

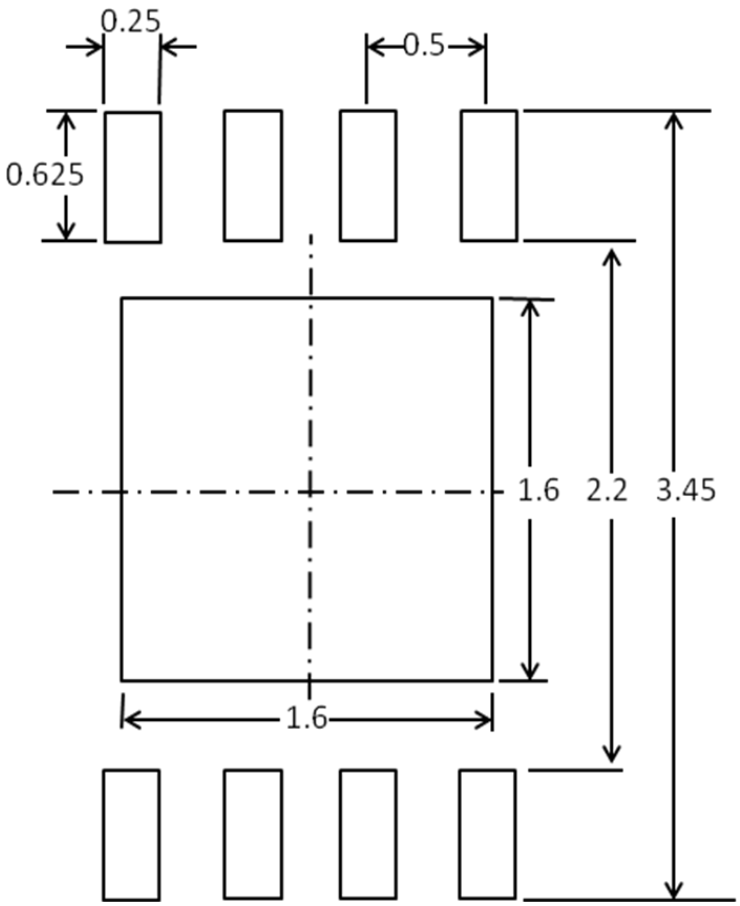
TDFN2x3-8L



Note:
Ref: JEDEC MO-229

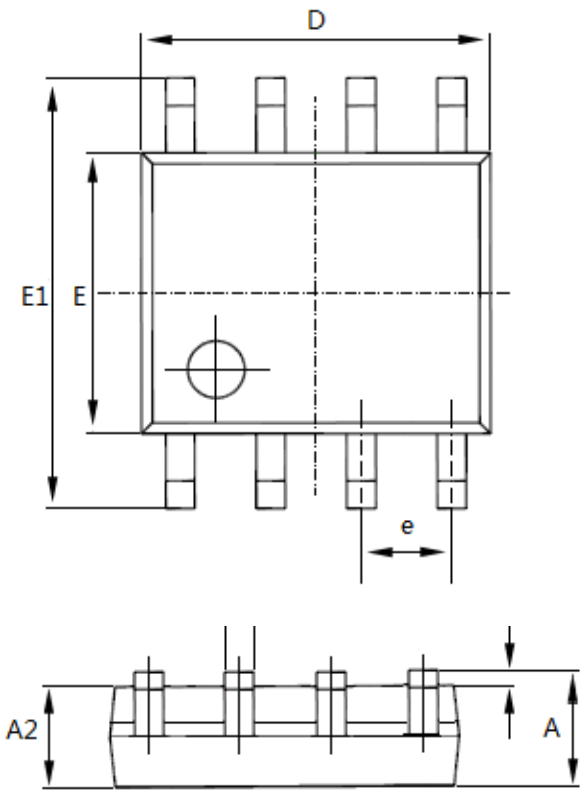
PKG. DIMENSIONS(MM)		
SYMBOL	MIN.	MAX
A	0.70	0.80
A1	0.00	0.50
A3	0.20REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20MIN	
b	0.20	0.30
e	0.50TYP	
L	0.22	0.38

Recommended Land pattern for TDFN2*3-8L



Note:
All linear dimensions are in millimeters

SOIC-8



Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012E/AA

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.27 BSC	
L	0.400	1.270
θ	0°	8°

Ordering Information

Part No.	Package Code	Package
PI6ULS5V9517AUE	U	Lead free and Green 8-pin MSOP
PI6ULS5V9517AUEX	U	Lead free and Green 8-pin MSOP, Tape & Reel
PI6ULS5V9517AWE	W	Lead free and Green 8-pin SOIC
PI6ULS5V9517AUEX	U	Lead free and Green 8-pin MSOP, Tape & Reel
PI6ULS5V9517AZEEX	ZE	Lead free and Green 8 TDFN2x3-8L, Tape & Reel

Note:
- E = Pb-free
- Adding X Suffix= Tape/Reel