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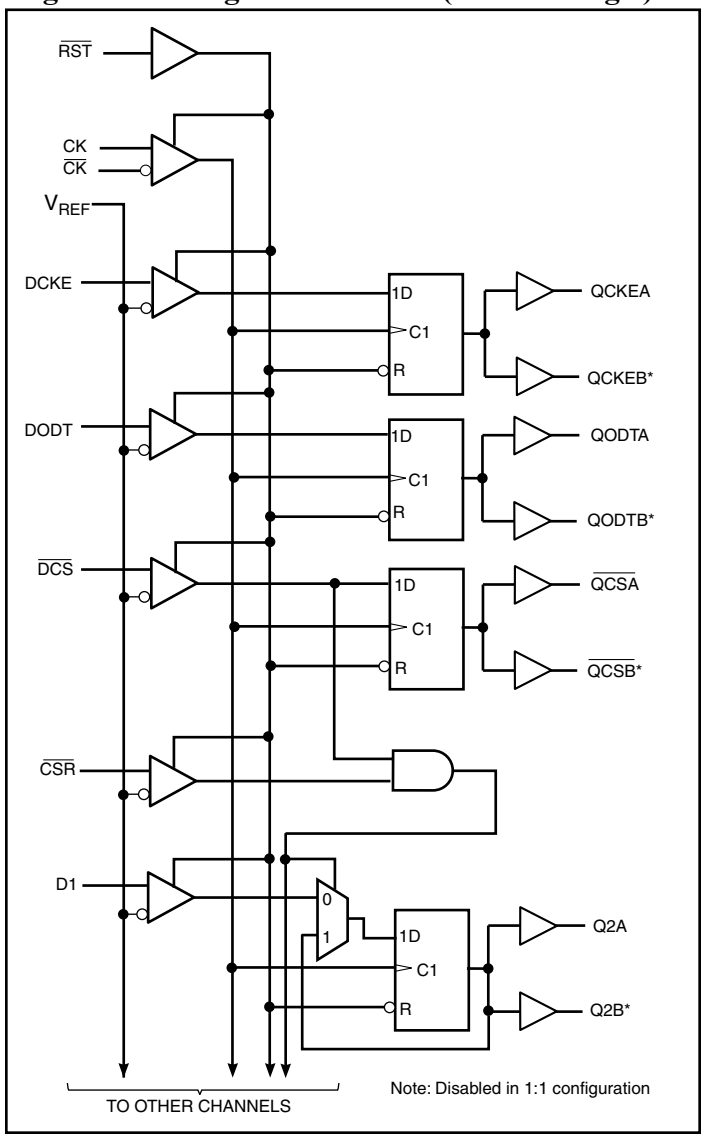
25-bit 1:1 or 14-bit 1:2 Configurable Registered Buffer with Parity

Product Features

- PI74SSTU32866 is a low-voltage device with V_{DD} = 1.8V
- Supports Low Power Standby Operation
- All Inputs are SSTL_18 Compatible, except $\overline{RST}$, C0, C1, which are LVCMOS.
- Output drivers are optimized to drive DDR-II DIMM loads
- Packaging (Pb-free & Green):
  — 96-Ball LFBGA (NB)
- PI74SSTU32866 supports DDR2-533/400

Logic Block Diagram 1:2 Mode (Positive Logic)



Product Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation. All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control and reset ($\overline{RST}$) inputs are LVCMOS. All data outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR-II DIMM load, and meet SSTL_18 specifications. The error ($\overline{QERR}$) output is 1.8 V open-drain driver.

The PI74SSTU32866 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low.

The PI74SSTU32866 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D2–D3, D5–D6, D8–D25 when

C0 = 0 and C1 = 0; D2–D3, D5–D6, D8–D14 when C0 = 0 and C1=1; or D1–D6, D8–D13 when C0 = 1 and C1=1) and indicates whether a parity error has occurred on the open-drain $\overline{QERR}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent data inputs must be tied to a known logic state.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. The partial-parity-out (PPO) and $\overline{QERR}$ signals are valid three cycles after the corresponding data inputs.

When used in pairs, the C0 input of the first register is tied low and the C0 input of the second register is tied high. The C1 input of both registers are tied high. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the first device. The PPO and $\overline{QERR}$ signals are produced on the second device three clock cycles after the corresponding data inputs. The PPO output of the first register is cascaded to the PAR_IN of the second register. The $\overline{QERR}$ output of the first register is left floating and the valid error information is latched on the $\overline{QERR}$ output of the second register.

If an error occurs and the $\overline{QERR}$ output is driven low, it stays latched low for two clock cycles or until RST is driven low. The DIMM-dependent signals (DCKE, $\overline{DCS}$, DODT, and $\overline{CSR}$) are not included in the parity check computation.

The C0 input controls the pinout configuration for the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

In the DDR-II RDIMM application, RST is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore,

Product Description - Continued

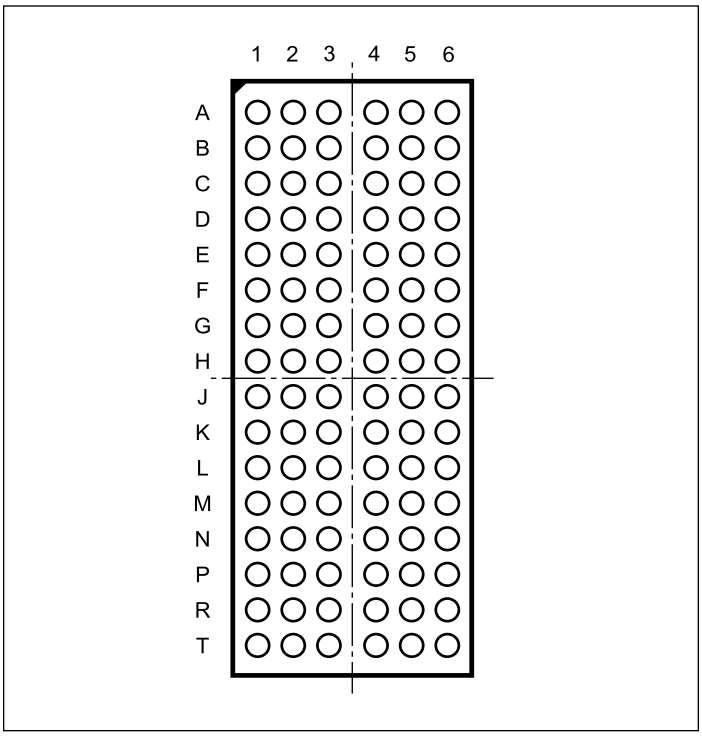
no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the Qn outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RST}$ until the input receivers are fully enabled, the design of the PI74SSTU32866 must ensure that the outputs will remain low, thus ensuring no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RST}$ must be held in the low state during power up.

The device supports low-power standby operation. When $\overline{RST}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when RST is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{RST}$, C0, and C1 inputs must always be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{DCS}$ and $\overline{CSR}$) inputs and will gate the Qn and PPO outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are high. If either $\overline{DCS}$ or $\overline{CSR}$ input is low, the Qn and PPO outputs will function normally. The $\overline{RST}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control and when driven low will force the Qn and PPO outputs low, and the $\overline{QERR}$ output high. If the $\overline{DCS}$ control functionality is not desired, then the $\overline{CSR}$ input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{DCS}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{DCS}$ only, then the $\overline{CSR}$ input should be pulled up to V_{DD} through a pullup resistor.

96-ball LFBGA (MO-205CC)



Pin Configuration[1,2] 1:1 Register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	DCKE	PPO	V_{REF}	V_{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{DD}	V_{DD}	Q3	Q15
D	DODT	$\overline{QERR}$	GND	GND	QODT	DNU
E	D5	D17	V_{DD}	V_{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{RST}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCS}$	DNU
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{DD}	V_{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{DD}	V_{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{DD}	V_{DD}	Q13	Q24
T	D14	D25	V_{REF}	V_{DD}	Q14	Q25

Notes:
1. DNU denotes do not use.
2. NC denotes No Internal Connection.

Pin Configuration 1:2 Register A (C0 = 0, C1 = 1)

	1	2	3	4	5	6
A	DCKE	PPO	V_{REF}	V_{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	DODT	$\overline{QERR}$	GND	GND	QODTA	QODTB
E	D5	NC	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RST}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	QCSA	QCSB
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{DD}	V_{DD}	Q10A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	D14	DNU	V_{REF}	V_{DD}	Q14A	Q14B

Pin Configuration[3,4] 1:2 Register B (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	PPO	V_{REF}	V_{DD}	Q1A	QB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	D4	$\overline{QERR}$	GND	GND	Q4A	Q4B
E	D5	DNU	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RST}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V_{DD}	V_{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	DCKE	DNU	V_{REF}	V_{DD}	QCKEA	QCKEB

Notes:
3. DNU denotes do not use.
4. NC denotes No Internal Connection.

Terminal Functions

Name	Description	Characteristics
GND	Ground	Ground Input
V_{DD}	Power Supply	1.8V nominal
V_{REF}	Input Reference Voltage	0.9V nominal
CK	Positive master clock input	Differential Clock input
$\overline{CK}$	Negative master clock input	Differential Clock input
C0, C1	Configuration control inputs	LVCMOS inputs
$\overline{RST}$	Asynchronous reset input - resets registers and disables V_{REF} data and clock differential - input receivers	LVCMOS inputs
$\overline{CSR}$, $\overline{DCS}$	Chip select inputs disables D1-D25 outputs switching when both inputs are high(5)	SSTL_18 input
D1-D25	Data input - clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$	SSTL_18 input
DODT	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	SSTL_18 input
PAR_IN	Parity input - arrives one clock cycle after the corresponding data input	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	SSTL_18 input
Q1-Q25	Data outputs that are suspended by the $\overline{DCS}$ and $\overline{CSR}$ control(6)	1.8V CMOS output
PPO	Partial Parity out - indicates odd parity of inputs D1- D25(5)	1.8V CMOS output
$\overline{QCS}$	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS output
QODT	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS output
QCKE	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS output
$\overline{QERR}$	Output error bit - generated one clock cycle after the corresponding data output	Open-drain output
NC	No internal connection	
DNU	Do not use - inputs are in stand-by-equivalent mode and outputs are driven low	

Notes:

5. Data inputs = D2, D3, D5, D6, D8-D25 when C0=0 and C1=0
   Data inputs = D2, D3, D5, D6, D8-D14 when C0=0 and C1=1
   Data inputs = D1-D6, D8-D10, D12, D13 when C0=1 and C1=1
6. Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0=0 and C1=0
   Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0=0 and C1=1
   Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0=1 and C1=1

Function Table (each flip flop)

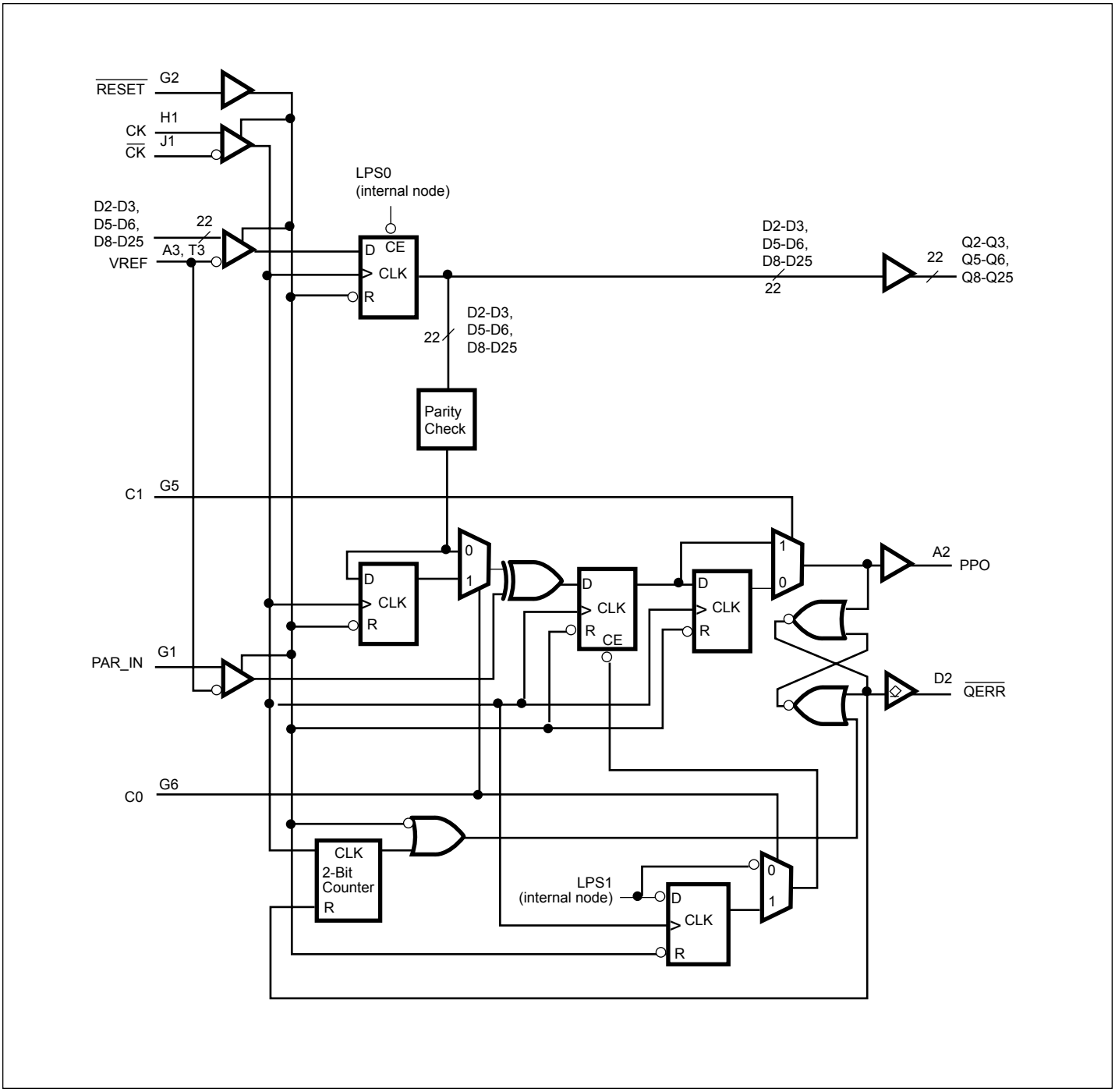
Inputs						Outputs		
$\overline{RST}$	$\overline{DCS}$	$\overline{CSR}$	CK	$\overline{CK}$	Dn, DODT, DCKE	Qn	$\overline{QCS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q0	Q0	Q0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q0	Q0	Q0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q0	Q0	Q0
H	H	H	↑	↓	L	Q0	H	L
H	H	H	↑	↓	H	Q0	H	H
H	H	H	L or H	L or H	X	Q0	Q0	Q0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

Function Table (Parity and Stand-by)

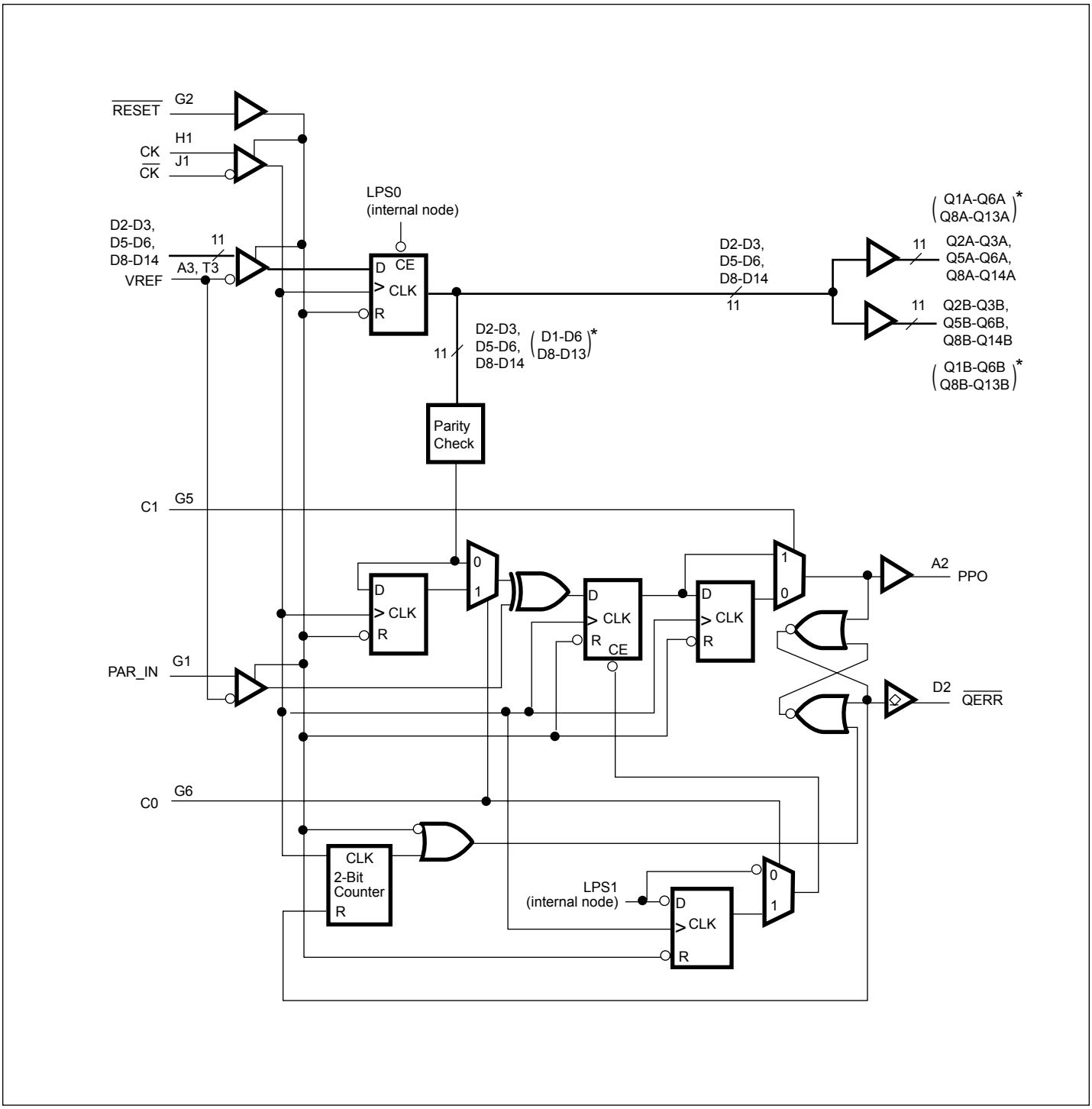
Inputs							Outputs	
$\overline{RST}$	$\overline{DCS}$	$\overline{CSR}$	CK	$\overline{CK}$	$\sum$ of inputs = H (D1- D25)[7]	PAR_IN[8]	PPO	$\overline{QERR}$[9]
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	H	L	↑	↓	Even	L	L	H
H	H	L	↑	↓	Odd	L	H	L
H	H	L	↑	↓	Even	H	H	L
H	H	L	↑	↓	Odd	H	L	H
H	H	H	↑	↓	X	X	PPO_0	$\overline{QERR}_0$
H	X	X	L or H	L or H	X	X	PPO_0	$\overline{QERR}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	H

Notes:

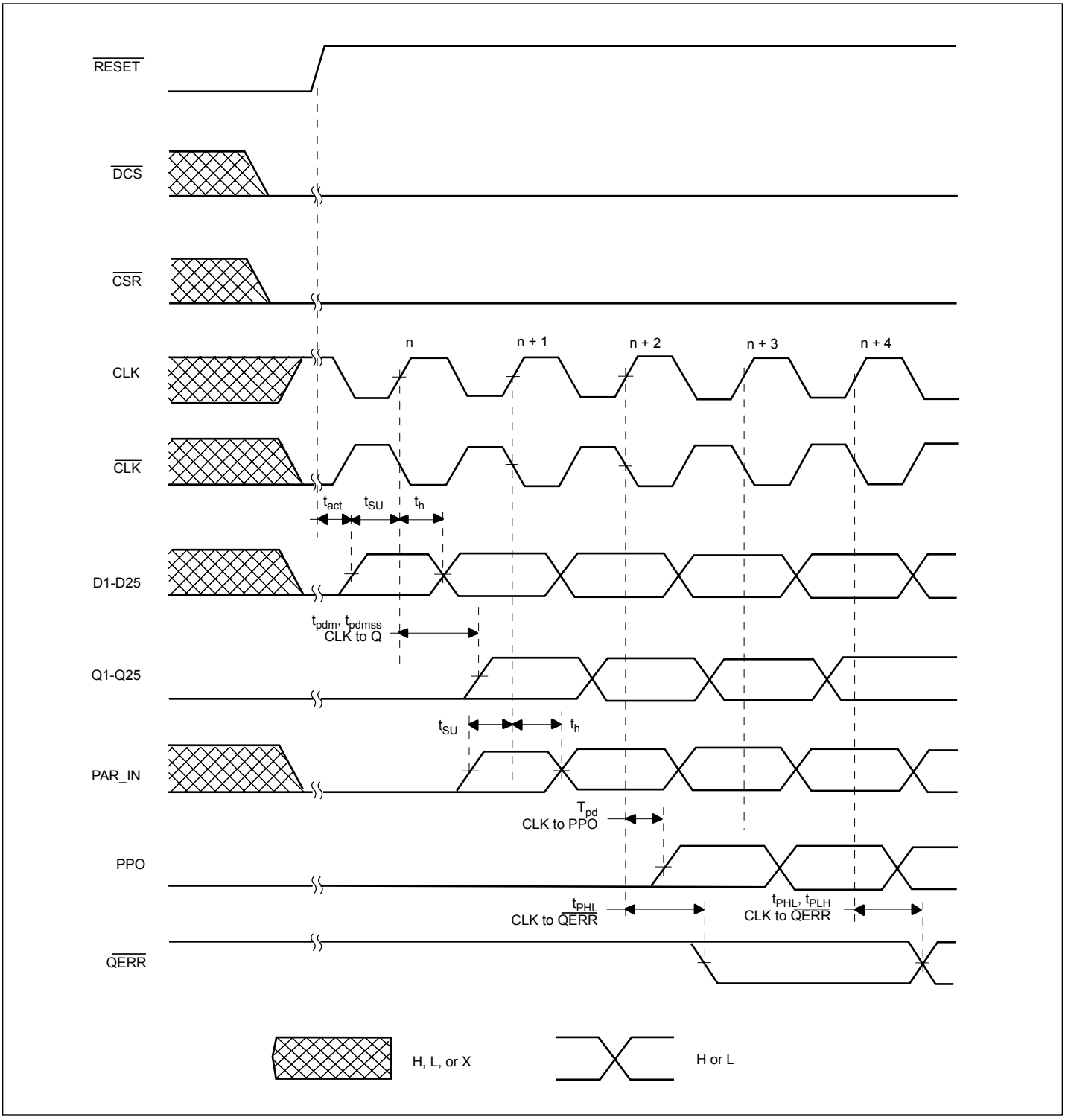
7. Data inputs = D2, D3, D5, D6, D8-D25 when C0=0 and C1=0
   Data inputs = D2, D3, D5, D6, D8-D14 when C0=0 and C1=1
   Data inputs = D1-D6, D8-D10, D12, D13 when C0=1 and C1=1
8. PAR_IN arrives one clock cycle (C0=0), or two clock cycles (C0=1), after the data to which it applies
9. this transition assumes $\overline{QERR}$ is high at the crossing of CK going high and $\overline{CK}$ going low. If $\overline{QERR}$ is low, it stays latched low for two clock cycles or until $\overline{RST}$ is driven low



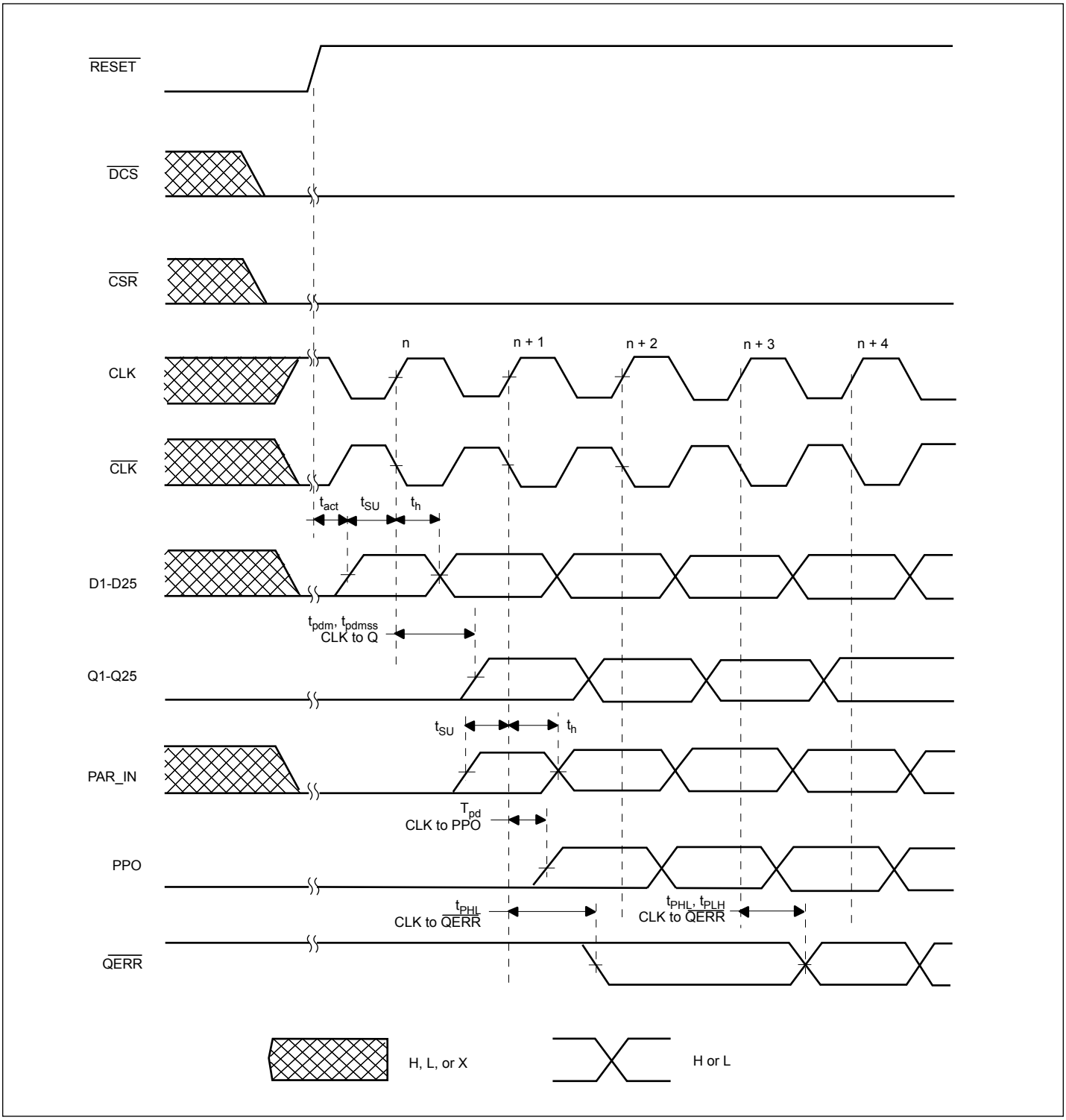
Parity Logic Diagram 1:1 Configuration (C0 = 0, C1 = 0)



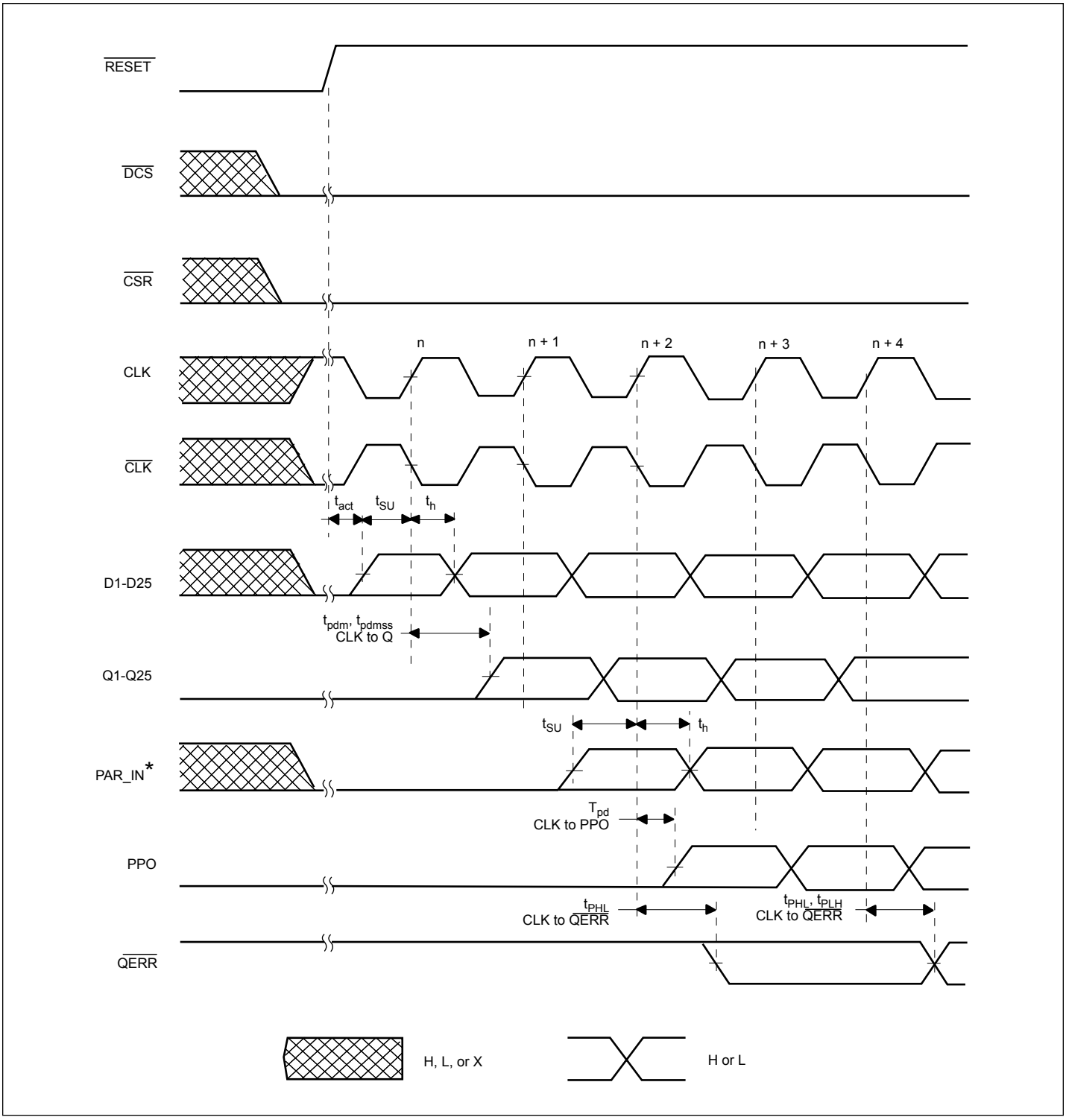
Parity Logic Diagram for 1:2 configuration Register A (C0 = 0, C1 = 1)
***Parity Logic Diagram for 1:2 configuration Register B (C0 = 1, C1 = 1)**



Timing Diagram for 1:1 Configuration (C0 = 0, C1 = 0)



Timing Diagram for 1:2 Configuration Register A (C0 = 0, C1 = 1)



Timing Diagram for 1:2 Configuration Register B (C0 = 1, C1 = 1)
* PAR_IN is driven from PPO of Regiser A (C0 =0, C1 = 1)

Maximum Ratings(10,11,12)

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage Range, V_{DD} .....–0.5V to 2.5V
Input Voltage Range,V_I : (See Notes 2 and 3): .....–0.5V to 2.5V
Output Voltage Range, V_O (See Notes 2 and 3)....–0.5V to V_{DD} + 0.5V
Input Clamp current, I_{IK} (V_I < 0 or V_I = V_{DD}) ..... –50mA
Output Clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})..... ±50mA
Continous Output Current, I_O (V_O = 0 to V_{DD}) ..... ±50mA
Continous Current through each V_{DD} or GND..... ±100mA
Storage Temperature, T_{STG}..... 150 ºC

Notes:

10. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
11. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
12. This value is limited to 2.5V maximum

Recommended Operating Conditions(13)

Parameters	Description		Min.	Nom.	Max.	Units
V_{DD}	Supply Voltage		1.7		1.9	V
V_{REF}	Reference Voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 xV_{DD}	
V_{TT}	Termination Voltage		V_{REF} -40mA	V_{REF}	V_{REF} -40mA	
V_I	Input Voltage		0		V_{DD}	
V_{IH}	AC High - Level Input Voltage	Data, $\overline{CSR}$ and PAR_IN Inputs	V_{REF} +250mV			
V_{IL}	AC Low- Level Input Voltage				V_{REF} -250mV	
V_{IH}	DC High - Level Input Voltage		V_{REF} +25mV			
V_{IL}	DC Low- Level Input Voltage				V_{REF} -125mV	
V_{IH}	High Level Input Voltage	$\overline{RST}$, CN	0.65 x V_{DD}			
V_{IL}	Low Level Input Voltage				0.35 x V_{DD}	
V_{ICR}	Common-mode input Voltage	CK, $\overline{CK}$	0.675		1.125	
V_{ID}	Differential Input Voltage		600			mV
I_{OH}	High-Level Output Current				-8	mA
I_{OL}	Low-Level Output Current				8	
T_A	Operating Free-air Temperature		0		70	ºC

Note:

13. The $\overline{RST}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RST}$ is low.

Electrical Characteristics (Over Recommended Operating Free Air Temperature range)

Parameter	Description	Test Conditions		V_{DD}	Min.	Nom.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -6 mA		1.7V	1.2			V
V_{OL}	Output Low Voltage	I_{OL} = 6 mA		1.7V			0.5	
I_I	All inputs	$V_I = V_{DD}$ or GND		1.9V			±5	µA
I_{DD}	Static Stand-by	$\overline{RST}$ = GND	I_O = 0	1.9V			100	
	Static Operating Current	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$		1.9V			40	mA
I_{DDD}	Dynamic Operating Current - clock only	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$, or $V_{IL(AC)}$ CK and $\overline{CK}$ switching 50% duty cycle	I_O = 0	1.8V	28			µA/ MHz
	Dynamic Operating - per each data input, 1:1 mode	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$, or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle		1.8V	36			µA/ MHz
	Dynamic Operating - per each data input, 1:2 mode	$\overline{RST} = V_{DD}$, $V_I = V_{IH(AC)}$, or $V_{IL(AC)}$ CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle		1.8V	36			
C_I	Input capacitance, Data and CSR inputs	$V_I = V_{REF}$ ± 250mV		1.8V	2.5		3.5	pF
	Input capacitance, CK and $\overline{CK}$	V_{ICR} = 0.9V, V_{ID} = 600mV			2		3	
	Input capacitance, $\overline{RST}$	$V_I = V_{DD}$ or GND				2.5		

Timing Requirements Over Recommended Operating Free Air Temperature range (See Figure 1)

Parameter	Description		Min.	Max	Units
f_{clock}	Clock frequency			270	MHz
t_W	Pulse Duration, CK, $\overline{CK}$, High or low		1		ns
t_{act}	Differential inputs active time[14, 15]			10	
t_{inact}	Differential inputs inactive time[14, 15, 16]			15	
t_{su}	Setup time	$\overline{DCS}$ before CK↑, $\overline{CK}$↓, $\overline{CSR}$ high, $\overline{CSR}$ before CK↑, $\overline{CK}$↓, $\overline{DCS}$ high	0.7		
		$\overline{DCS}$ before CK↑, CK↓, $\overline{CSR}$ low	0.5		
		DODT, DCKE and data before CK↑, $\overline{CK}$↓	0.5		
		PAR_IN before CK↑, $\overline{CK}$↓	0.5		
th	Hold Time	DCS, DODT, DCKE and data before CK↑, $\overline{CK}$↓	0.5		
		PAR_IN after CK↑, $\overline{CK}$↓	0.5		

Notes: 14. This parameter is not necessarily production tested.
15. Data and V_{REF} inputs must be a low minimum time of t_{act} max, after $\overline{RST}$ is taken high.
16. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max after $\overline{RST}$ is taken low.

Switching Characteristics Over Recommended Operating Free Air Temperature range (See Figure 1)

Symbol	Parameter	Measure Condition	Min.	Max.	Units
f_{MAX}	Maximum input clock frequency		270		MHz
t_{PDM}	Propagation Delay, single bit switching	From CK↑ and $\overline{CK}$↓ to Qn	1.41	2.15	ns
t_{PDMS}(17,18)	Propagation Delay Simultaneous Switching			2.35	ns
t_{PD}	Propagation Delay	From CK↑ and $\overline{CK}$↓ to $\overline{PPO}$	0.5	1.8	ns
t_{LH}	Low-to-High propagation delay	From CK↑ and CK↓ to $\overline{QERR}$	1.2	3	ns
t_{HL}	High-to-Low propagation delay		1	2.4	ns
t_{PHL}	High-to-Low propagation delay	From $\overline{RST}$↓ to Qn↓		3	ns
t_{PHL}	High-to-Low propagation delay	From $\overline{RST}$↓ to PPO↓		3	ns
t_{PLH}	Low-to-high propagation delay	From $\overline{RST}$↓ to $\overline{QERR}$↓		3	ns

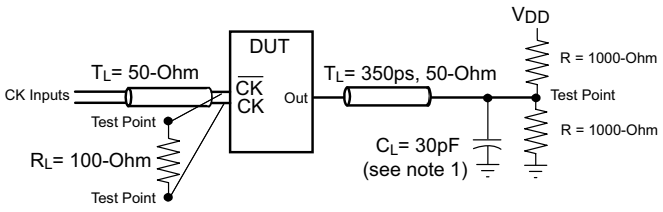
Notes:
17. Includes 350ps test load transmission-line delay.
18. This parameter is not necessarily production tested.

Data Output Edge Rates Over Recommended Operating Free Air Temperature range (See Figure 2)

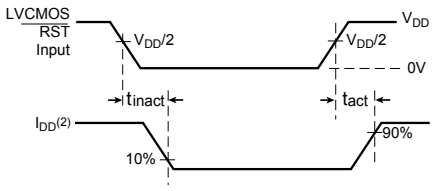
Symbol	Parameter	Measurement Condtions	Min.	Max.	Units
dV/dt_r	Rising edge slew rate	From 20% to 80%	1	4	V/ns
dV/dt_f	Falling edge slew rate	From 20% to 80%	1	4	
dV/dt_Δ(19)	absolute difference between dV/dt_r and dV/dt_f	From 20% or 80% to 80% or 20%		1	

Notes:
19. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

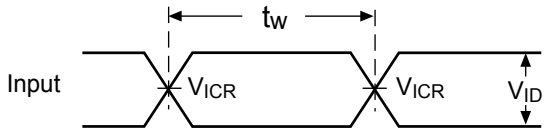
Test Circuit and Switching Waveforms(20-28)



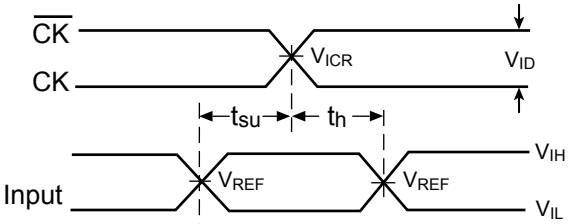
Load Circuit



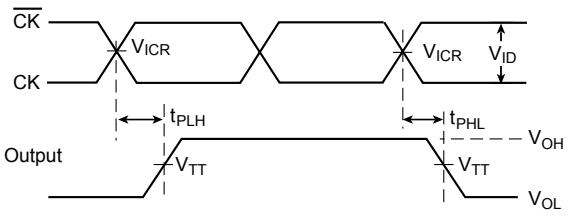
Voltage and Current Waveforms
Input Active and Inactive Times



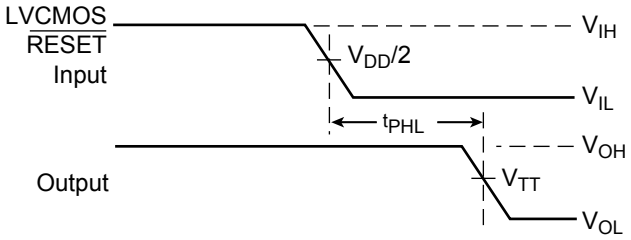
Voltage Waveforms - Pulse Duration



Voltage Waveforms - Setup and Hold Times



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Propagation Delay Times

Figure 1. Parameter Measurement Information (V_{DD} = 1.8V ± 0.1V)

Notes:

20. C_L includes probe and jig capacitance

21. I_{DD} tested with clock and data inputs held at V_{DD} or GND and I_O = 0mA

22. All input pulses are supplied by generators having the following characteristics: Pulse Repertition Rate ≥ 10 MHz, ZO = 50Ω, input slew rate = 1V/ns ± 20% (unless otherwise specified).

23. The outputs are measured one at a time with one transition per measurement.

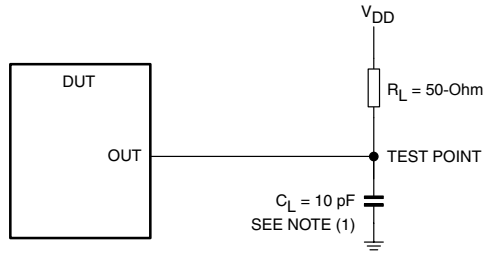
24. V_{REF} = V_{DD} /2

25. V_{IH} = V_{REF} +250mV (ac voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.

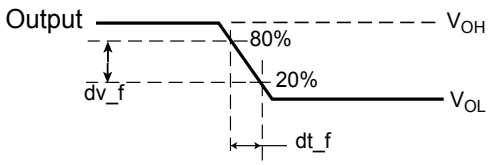
26. V_{IL} = V_{REF} -250mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

27. V_{ID} = 600mV

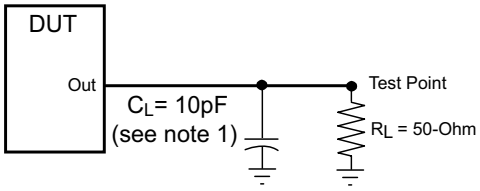
28. t_{PLH} and t_{PHL} are the same as t_{pdm}.



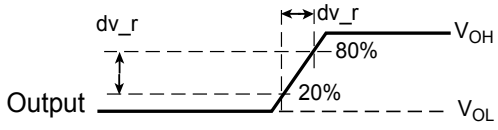
Load Circuit, High-to-Low slew measurement(29,30)



Voltage Waveforms - High-to-Low Slew Rate Measurement



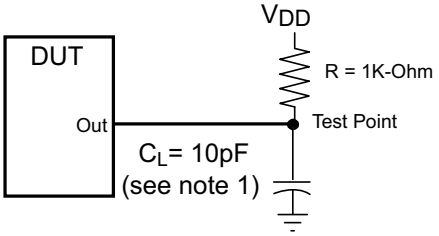
Load Circuit - Low-to-High Slew Rate Measurement(29,30)



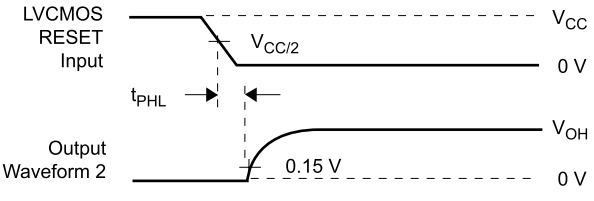
Voltage Waveforms - Low-to-High Slew Rate Measurement

Figure 2. Data Output Slew-Rate Measurement Information (V_{DD} = 1.8V ± 0.1V)

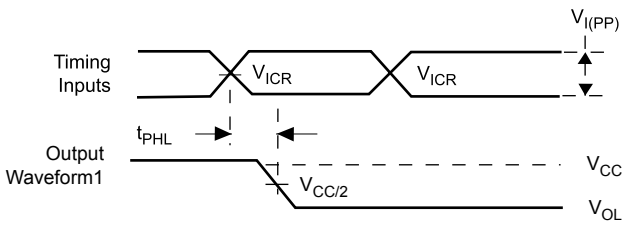
Notes:
29. C_L includes probe and jig capacitance
30. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, ZO = 50Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).



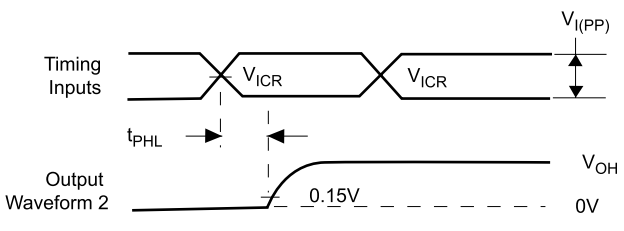
Load Circuit - Error Output Slew Rate Measurement



Voltage waveform, open-drain output low-to-high transition time with respect to reset inputs

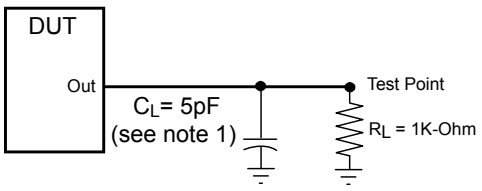


Voltage waveform, open-drain output high-to-low transition time with respect to clock inputs

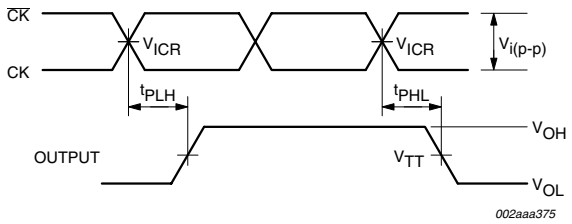


Voltage Waveforms - Open-drain output low-to-high transtion time with respect to clock inputs

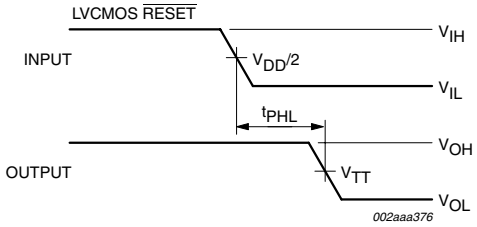
Figure 3. Error output Measurement Information (V_{DD} = 1.8V ± 0.1V)



Partial-Parity-Out (PPO) load circuit



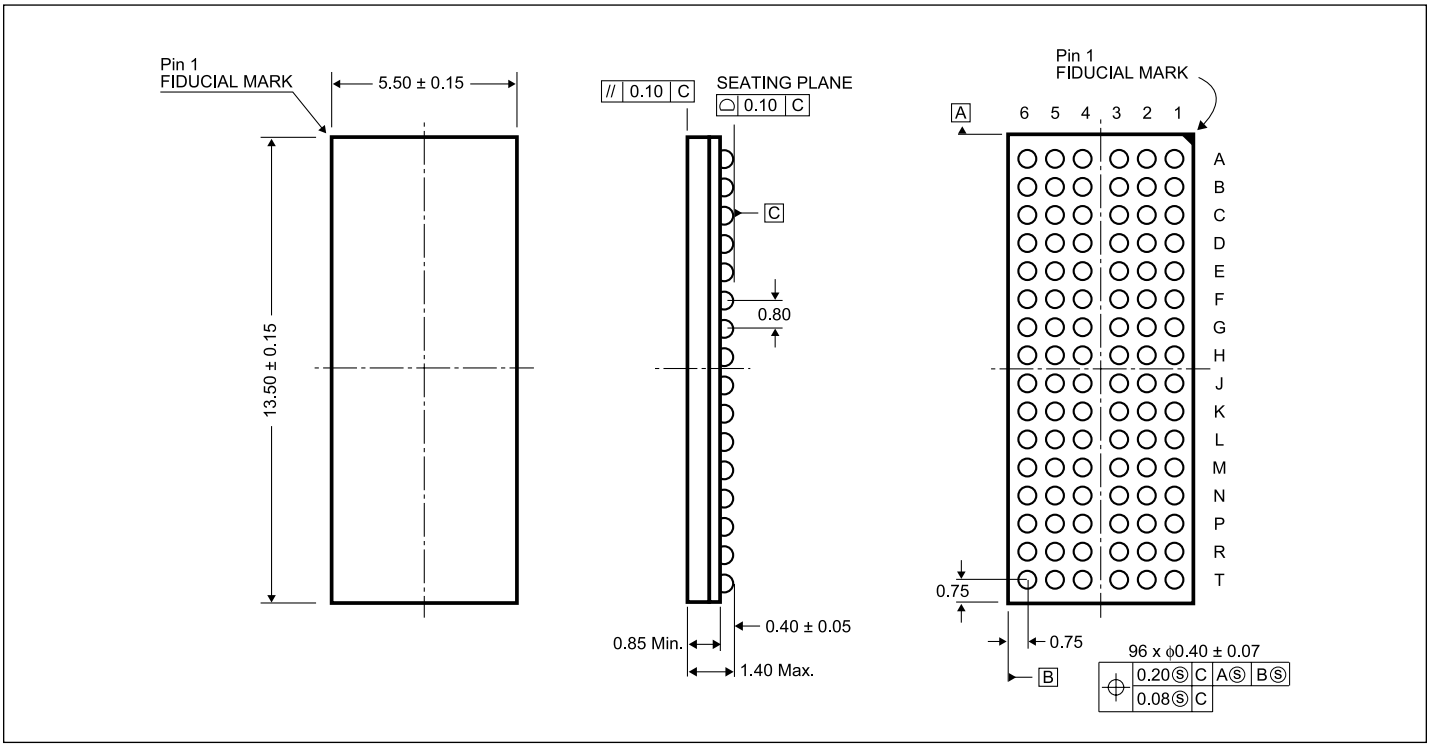
Partial-Parity-Out (PPO) voltage wavefroms; propagation delay times wtih respect to clock inputs



Partial-Parity-Out (PPO) voltage wavefroms; propagation delay times wtih respect to reset inputs

Figure 4. Partial-Parity-Out (PPO) Measurement Information (V_{DD} = 1.8V ± 0.1V)

Packaging Mechanical: 96-ball LFBGA (NB)



Ordering Information (1,2,3)

Ordering Code	Package Code	Package Type
PI74SSTU32866NB	NB	96-Ball LFBGA
PI74SSTU32866NBE	NB	Pb-free & Green, 96-Ball LFBGA

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. X suffix = Tape/Reel