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PI7C8952

PCI Dual UART

Datasheet
Revision 1.2
September 2016

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REVISION HISTORY

Date	Revision Number	Description
09/12/14	0.1	Preliminary Datasheet
12/09/15	1.0	Updated Section 1 Feature Updated Section 6.3 Configuration Registers Updated Section 9 Electrical Specification
01/06/16	1.1	Updated Section 9 Electrical Specification Updated Section 11 Ordering Information
09/09/16	1.2	Updated Section 4 Pin Assignment Updated Section 11 Ordering Information

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- Universal PCI Bus Buffers – Auto sense 3.3V or 5V operation
- 32-bit PCI Bus 2.3 target signaling compliance
- Fully 16C550 software compatible UARTs
- 128-byte FIFO for each transmitter and receiver
- Baud rate up to 15 Mbps in asynchronous mode
- Flexible clock prescaler from 4 to 46
- Data Transfer in Byte, Word and Double-word
- Data Read/Write Burst Operation
- Automated in-band flow control using programmable Xon/Xoff in both directions
- Automated out-of-band flow control using CTS#/RTS# and/or DSR#/DTR#
- Arbitrary trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-of-band flow control
- Global Interrupt Status and readable FIFO levels to facilitate implementation of efficient device drivers
- Detection of bad data in the receiver FIFO
- Data framing size including 5, 6, 7, 8 and 9 bits
- Infrared (IrDA 1.0/1.1) Data Encoder/Decoder
- Auto RS-485 Half-duplex Output with Control Polarity Selector
- Eight General Purpose Inputs/Outputs
- A General Purpose 16-bit Timer/Counter
- Hardware reconfiguration through Microwire compatible EEPROM
- Operations via I/O or memory mapping
- Sleep Mode with Automatic Wake-up
- Dual power operation (3.3V or 5.0V for PCI I/O and 1.8V-5.0V for UART I/O)
- Power dissipation: 0.2W typical in normal mode
- Industrial Temperature Range -40^{o} to 85^{o}
- 100-pin LQFP package

2. APPLICATIONS

- Remote Access Servers
- Network / Storage Management
- Factory Automation and Process Control
- Instrumentation
- Multi-port RS-232/ RS-422/ RS-485 Cards
- Point-of-Sale Systems (PoS)
- Industrial PC (IPC)
- Industrial Control
- Gaming Machines
- Building Automation
- Embedded Systems

3. GENERAL DESCRIPTION

The PI7C8952 is a PCI Dual UART (Universal Asynchronous Receiver-Transmitters) I/O Bridge. It is specifically designed to meet the latest system requirements of high performance and lead (Pb) -free. The bridge can be used in a wide range of applications such as Remote Access Servers, Automation, Process Control, Instrumentation, POS, ATM and Multi-port RS232/ RS422/ RS485 Cards. The bridge supports two high performance UARTs, each of which supports Baud rate up to 15 Mbps in asynchronous mode. The UARTs support in-band and out-band auto flow control, arbitrary trigger level, I/O mapping and memory mapping, IrDA (Infrared Data Association) encoder/decoder, 8 general purpose I/O and 16-bit timer counter. The PI7C8952 is fully software compatible with 16C550 type device drivers and can be configured to fit the requirements of RS232, RS422 and RS485 applications. The EEPROM interface is provided for system implementation convenience. Some registers can be pre-programmed via hardware pin settings to facilitate system initialization. For programming flexibility, all of the default configuration registers can be overwritten by EEPROM data, such as sub-vendor and sub-system ID.

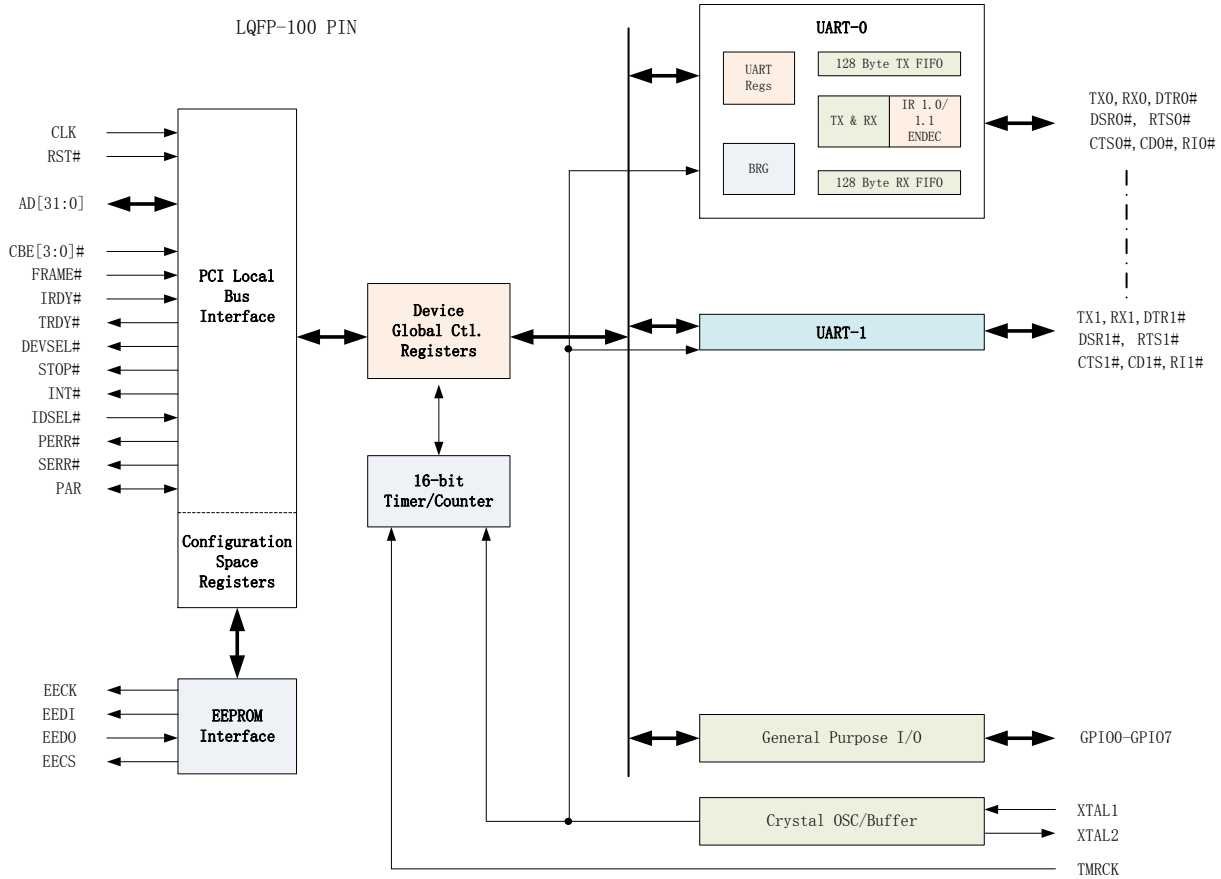

Figure 3-1 PI7C8952 Block Diagram

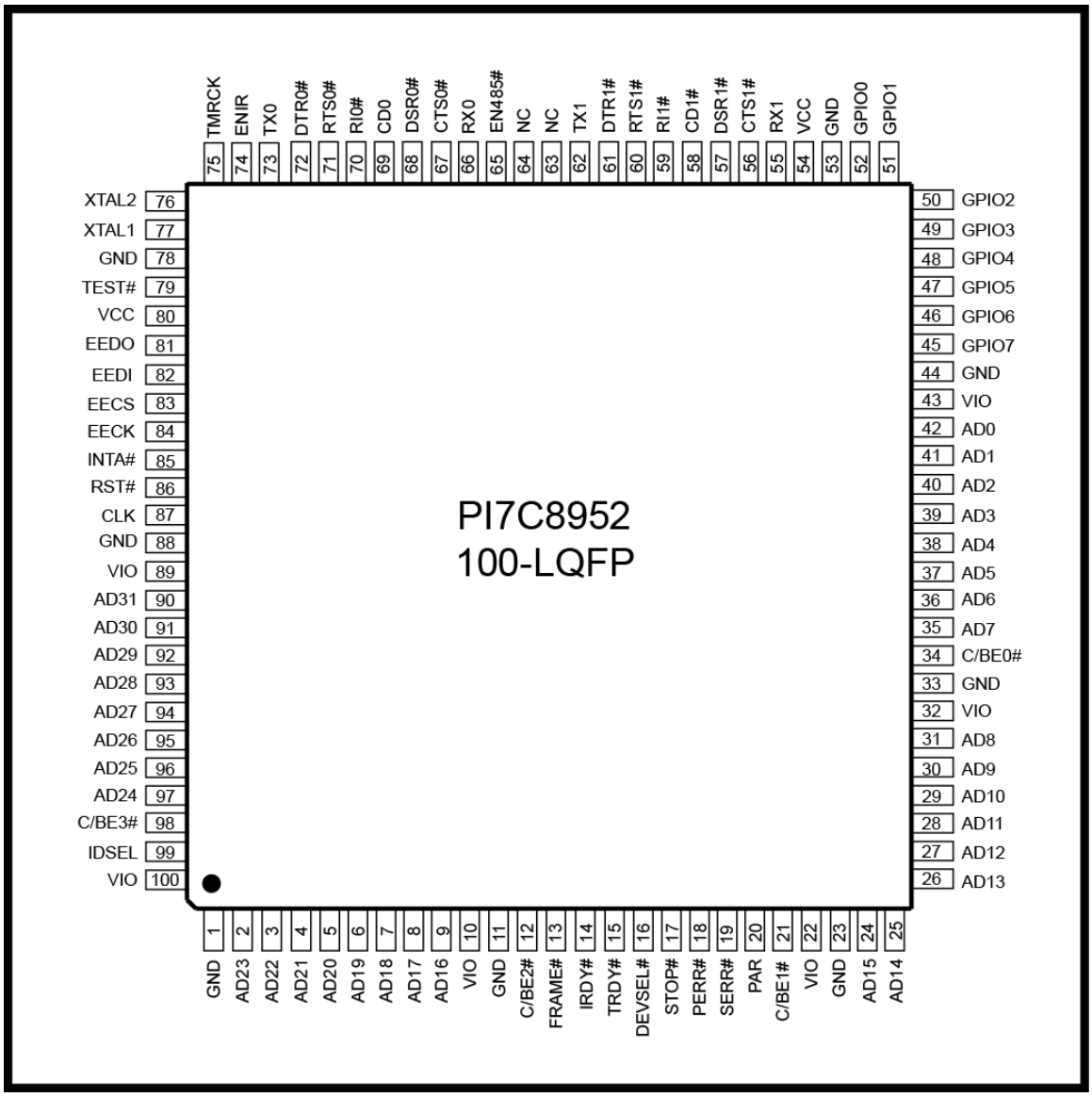

Figure 3-2 Pin Out

4. PIN ASSIGNMENT

NAME	PIN#	TYPE	DESCRIPTION
PCI LOCAL BUS INTERFACE			
RST#	86	I	PCI Bus reset input (active low). It resets the PCI local bus configuration space registers, device configuration registers and UART channel registers to the default condition.
CLK	87	I	PCI Bus clock input of up to 33.34MHz.
AD31-AD24, AD23-AD16, AD15-AD8, AD7-AD0	90-97, 2-9, 24-31, 35-42	I/O	Address data lines [31:0] (bidirectional).
FRAME#	13	I	Bus transaction cycle frame (active low). It indicates the beginning and duration of an access.
C/BE3#-C/BE0#	98,12,21,34	I	Bus Command/Byte Enable [3:0] (active low). This line is multiplexed for bus Command during the address phase and Byte Enables during the data phase.
IRDY#	14	I	Initiator Ready (active low). During a write, it indicates that valid data is present on data bus. During a read, it indicates the master is ready to accept data.
TRDY#	15	O	Target Ready (active low).
STOP#	17	O	Target request to stop current transaction (active low).
IDSEL	99	I	Initialization device select (active high).
DEVSEL#	16	O	Device select to the PI7C8952 (active low).
INTA#	85	OD	Device interrupt from PI7C8952 (open drain, active low)
PAR	20	I/O	Parity is even across AD[31:0] and C/BE[3:0]#. (bidirectional, active high).
PERR#	18	O	Data Parity error indicator, except for Special Cycle transactions (active low). Optional in bus target application.
SERR#	19	OD	System error indicator, Address parity or Data parity during Special Cycle transactions (open drain, active low). Optional in bus target application
MODEM OR SERIAL I/O INTERFACE			
TX0	73	O	UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX0	66	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via SFR bit-3.
RTS0#	71	O	UART channel 0 Request to Send or general purpose output (active low). If this output is not used, leave it unconnected.
CTS0#	67	I	UART channel 0 Clear to Send or general purpose input (active low). This input should be connected to VCC when not used.
DTR0#	72	O	UART channel 0 Data Terminal Ready or general purpose output (active low). If this output is not used, leave it unconnected.
DSR0#	68	I	UART channel 0 Data Set Ready or general purpose input (active low). This input should be connected to VCC when not used.
CD0#	69	I	UART channel 0 Carrier Detect or general purpose input (active low). This input should be connected to VCC when not used.
RI0#	70	I	UART channel 0 Ring Indicator or general purpose input (active low). This input should be connected to VCC when not used.
TX1	62	O	UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX1	55	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via SFR bit-3.
RTS1#	60	O	UART channel 1 Request to Send or general purpose output (active low). If this output is not used, leave it unconnected.
CTS1#	56	I	UART channel 1 Clear to Send or general purpose input (active low). This input should be connected to VCC when not used.
DTR1#	61	O	UART channel 1 Data Terminal Ready or general purpose output (active low). If this output is not used, leave it unconnected.
DSR1#	57	I	UART channel 1 Data Set Ready or general purpose input (active low). This input should be connected to VCC when not used.
CD1#	58	I	UART channel 1 Carrier Detect or general purpose input (active low). This input should be connected to VCC when not used.
RI1#	59	I	UART channel 1 Ring Indicator or general purpose input (active low). This input should be connected to VCC when not used.
ANCILLARY SIGNALS			

NAME	PIN#	TYPE	DESCRIPTION
GPIO0-GPIO7	52-45	I/O	Multi-purpose inputs/outputs 0-7. This function of these pin are defined thru the Configuration Register GPSEL,GPLVL,GPINV,GP3T and GPINT.
EECK	84	O	Serial clock to EEPROM. An internal clock of CLK divide by 256 is used for reading the vendor and sub-vendor ID during power up or reset.
EECS	83	O	Chip select to a EEPROM device like 93C46. Requires a pull-up 4.7K ohm resister for external sensing of EEPROM during power up.
EEDI	82	O	Write data to EEPROM device.
EEDO	81	I	Read data from EEPROM device.
XTAL1	77	I	Crystal of up to 24MHz or external clock input of up to 50MHz for data rates up to 6.25Mbps at 5V and 8X sampling. See AC Characterization table. Caution: this input is not 5V tolerant at 3.3V.
XTAL2	76	O	Crystal or buffered clock output.
TMRCK	75	I	16-bit timer/counter external clock input.
ENIR	74	I	Global Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register SFRST). It can be used to start up both UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART. Software can override this pin thereafter and enable or disable it.
EN485#	65	I	Global Auto RS485 half-duplex direction control enable (active low). During power up or reset, this pin is sampled and if it is a logic high, both UARTs are set for Auto RS485 Mode. Also, the Auto RS485 bit, SFR[2], is set in both channels. Software can override this pin thereafter and enable or disable it.
TEST#	79	I	Factory Test. Connect to VCC for normal operation.
VCC	54, 80	PWR	Power supply for non-PCI signals and core logic. it can be 1.8V to 5.0V, no matter if VIO is 3.3V or 5.0V. However VCC must equal VIO at sleep mode to minimize the power current.
VIO	10, 22, 32, 43, 89, 100	PWR	PCI bus I/O power supply – 3.3V or 5V, detected by the auto-sense circuitry of the PI7C8952. This power supply determines the VOH level of the PCI bus interface outputs. (PCI 2.3 signalling compliant at both 3.3V and 5V operation, suitable for universal form factor add-in card application.)
GND	1, 11, 23, 33, 44, 53, 78, 88	PWR	Power supply common, ground.
NC	63, 64		No Connection.

Note: Pin Type : I = Input, O = Output, I/O = Input/output, OD = Output Open Drain.

5. FUNCTIONAL DESCRIPTION

The PI7C8952 is an integrated solution of two high-performance 16C550 UARTs with one PCI host interface. The PCI interface allows direct access to the configuration and status registers of the UART channels.

The UARTs in the PI7C8952 support the complete register set of the 16C550-type devices. The UARTs support Baud Rates up to 15 Mbps in asynchronous mode. Each UART channel has 128-byte deep transmit and receive FIFOs. The high-speed FIFOs reduce CPU utilization and improve data throughput. In addition, the UARTs support enhanced features including automated in-band flow control using programmable Xon/Xoff in both directions, automated out-band flow control using CTS#/RTS# and/or DRS#/DTR#, and arbitrary transmit and receive trigger levels.

5.1. CONFIGURATION SPACE

The PI7C8952 has two sets of registers to allow various configuration and status monitoring functions. The PCI Configuration Space Registers enable the plug-and-play and auto-configuration when the device is connected to the PCI system bus. The UART configuration and internal registers enable the general UART operation functions, status control and monitoring.

5.1.1. PCI Configuration Space

The PI7C8952 is recognized as a PCI endpoint, which is mapped into the configuration space as a single logical device. Each endpoint in the system, including the PI7C8952, is part of a Hierarchy Domains originated by the Host, which is a tree with a Root Port at its head in the configuration space. The device configuration registers are implemented for the user to access the functionalities provided by the PCI specification.

All PCI endpoints facilitate a PCI-compatible configuration space to maintain compatibility with PCI software configuration mechanism. PCI Local Bus Specification, Revision 3.0 allocates 256 bytes per device function. The user can access the PCI 3.0 compatible region either by conventional PCI 3.0 configuration addresses.

5.1.2. UART Configuration Space

Through the UART registers, the user can control and monitor various functionalities of the UARTs on the PI7C8952 including FIFOs, interrupt status, line status, modem status and sample clock. Each of the UART's transmitter and receive data FIFOs can be conveniently accessed by reading and writing the registers in the UART configuration space. These registers allow flexible programming capability and versatile device operations of the PI7C8952. Each UART is accessed through an 8-byte I/O blocks. The addresses of the UART blocks are offset by the base address referred by the Base Address Register (BAR). The value of the base address is loaded from the I/O or Memory Base Address defined in the PCI configuration space.

The PI7C8952 also supports enhanced features such as Xon/Xoff, automatic flow control, Baud Rate prescaling and various status monitoring. These enhanced features are available through the memory address offset by the BAR in the PCI configuration space.

The basic features available in the registers in I/O mode are also available in the registers in memory-mapping mode. Accesses to these registers are equivalent in these two modes.

The UARTs on the PI7C8952 supports operations in 16C450, 16C550 and 16C950 modes. These modes of operation are selected by writing the SFR, FCR and EFR registers. The PI7C8952 is backward compatible with these modes of operation.

5.2. DEVICE OPERATION

The PI7C8952 is configured by the Host in the bootstrap process during system start-up. The Host performs bus scans and recognizes the device by reading vendor and device IDs. Upon successful device identification, the system then loads device-specific driver software and allocates I/O, memory and interrupt resources. The driver software allows the user to access the functions of the device by reading and writing the UART registers. The PCI interface incorporates convenient device operation and high system performance.

5.2.1. Configuration Access

The PI7C8952 accepts type 0 configuration read and write accesses defined in the PCI 3.0 Specification.

5.2.2. I/O Reads/Writes

The PCI interface of the PI7C8952 decodes incoming transaction packets. If the address is within the region assigned by the I/O Base Address Registers, the transaction is recognized as an I/O Read or Write.

5.2.3. Memory Reads/Writes

Similar to the I/O Read/Write, if the address of the transaction packet is within the memory range, a Memory Read/Write occurs.

5.2.4. Mode Selection

All of the internal UART channels in the I/O Bridge support the 16C450, 16C550, Enhanced 16C550, and Enhanced 950 UART Modes. The mode of the UART operation is selected by toggling the Special Function Register (SFR[5]) and Enhanced Function Register (EFR[4]). The FIFO depth of each mode and the mode selection is tabulated in the table below.

Table 5-1 Mode Selection

UART Mode	SFR[5]	EFR[4]	FIFO Size
450/550	X	0	1/16
Enhanced 550	0	1	128
Enhanced 950	1	1	128

5.2.5. 450/550 Mode

The 450 Mode is inherently supported when 550 Mode is selected. When in the 450 Mode, the FIFOs are in the “Byte Mode”, which refers to the one-byte buffer in the Transmit Holding Register and the Receive Holding Register in each of the UART channels. When in the 550 Mode, the UARTs support an increased FIFO depth of 16.

When EFR[4] is set to “0”, the SFR[5] is ignored, and the 450/550 Mode is selected.

5.2.6. Enhanced 550 Mode

Setting the SFR[5] to “0” and EFR[4] to “1” enables the Enhanced 550 Mode. The Enhanced 550 Mode

further increases FIFO depth to 128.

5.2.7. Enhanced 950 Mode

128-deep FIFOs are supported in the Enhanced 950 Mode. When the Enhanced 950 Mode is enabled, the UART channels support additional features:

- Sleep mode
- Special character detection
- Automatic in-band flow control
- Automatic flow control using selectable arbitrary thresholds
- Readable status for automatic in-band and out-of-band flow control
- Flexible clock prescaler
- Programmable sample clock
- DSR/DTR automatic flow control

5.2.8. Transmit and Receive FIFOs

Each channel of the UARTs consists of 128 bytes of transmit FIFOs and 128 bytes of receive FIFOs, namely the Transmit Holding Registers (THR) and the Receive Holding Registers (RHR). The FIFOs provide storage space for the data before they can be transmitted or processed. The THR and RHR operate simultaneously to transmit and read data.

The transmitter reads data from the THR into the Transmit Shift Register (TSR) and removes the data from top of the THR. It then converts the data into serial format with start and stop bits and parity bits if required. If the transmitter completes transmitting the data in the TSR and the THR is empty, the transmitter is in the idle state. The data that arrive most recently are written to the bottom of the THR. If the THR is full, and the user attempts to write data to the THR, a data overrun occurs and the data is lost.

The receiver writes data to the bottom of the RHR when it finishes receiving and decoding the data bits. If the RHR is full when the receiver attempts to write data to it, a data overrun occurs. Any read operation to an empty RHR is invalid.

The empty and full status of the THR and RHR can be determined by reading the empty and full flags in the Line Status Register (LSR). When the transmitter and receiver are ready to transfer data to and from the FIFOs, interrupts are raised to signal this condition. Additionally, the user can use the Receive FIFO Data Counter (RFDC) and Transmit FIFO Data Counter (TFDC) registers to determine the number of items in each FIFO.

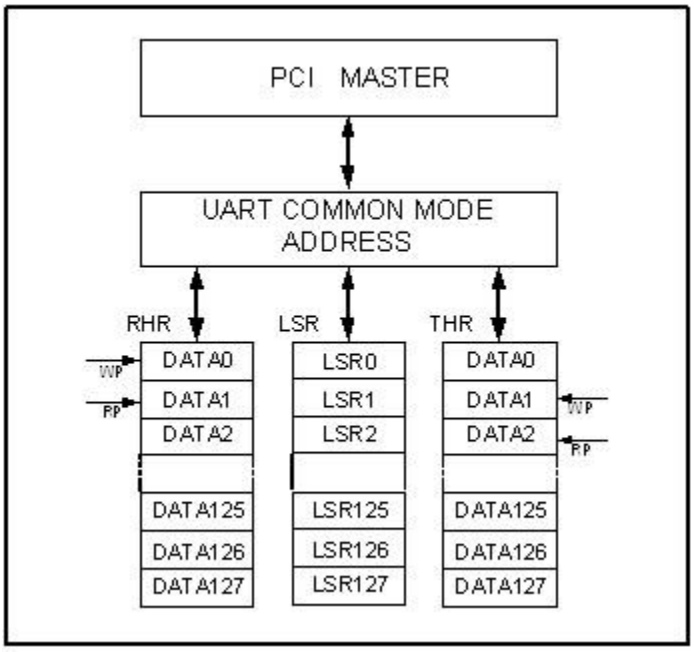

Figure 5-1 Transmit and Receive FIFOs

5.2.9. Automated Flow Control

The device uses automatic in-band flow control to prevent data-overrun to the local receive FIFO and remote receive FIFO. This feature works in conjunction with the special character detection. When an XOFF condition is detected, the UART transmitter will suspend any further data transmission after the current character transmission is completed. The transmitter will resume data-transmission as soon as an XON condition is detected. The automatic in-band feature is enabled by the Enhanced Function Register (EFR). EFR[1:0] enables the in-band receive flow control, and EFR[3:2] enables the in-band transmit flow control.

The out-of-band flow control utilizes RTS# and CTS# pins to suspend and resume the data transmission and to prevent data-overrun. An asserted CTS# pin signals the UART to suspend transmission due to a full remote receive FIFO. Upon detecting an asserted CTS# pin, the UART will complete the current character transmission and enters idle mode until the CTS# pin is deserted.

The UART deasserts RTS# to signal the remote transmitter that the local receive FIFO reaches the programmed upper trigger level. When the local receive FIFO falls below the programmed lower trigger level, the RTS# is reasserted. The automatic out-of-band flow control is enabled by EFR[7:6].

5.2.10. Internal Loopback

The internal loopback capability of the UARTs is enabled by setting Modem Control Register bit-4 (MCR[4]) to 1. When the feature is enabled, the data from the output of the transmit shift register are looped back to the input of the receive shift register. This feature provides the users a way to perform system diagnostics by allowing the UART to receive the same data it is sending.

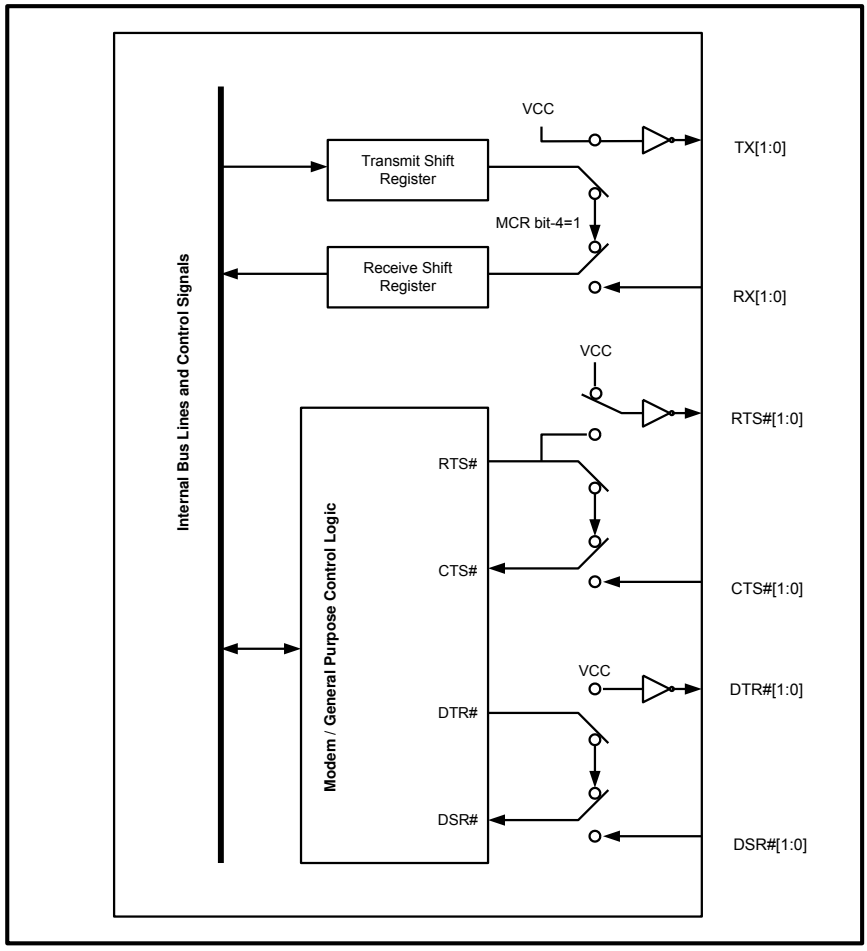

Figure 5-2 Internal Loopback in PI7C8952

5.2.11. Crystal Oscillator

The PI7C8952 uses a crystal oscillator or an external clock source to provide system clock to the Baud Rate Generator. When a clock source is used, the clock signal should be connected to the XTLI pin, and a 2K pull-up resistor should be connected to the XTLO pin.

When a crystal oscillator is used, the XTLI is the input and XTLO is the output, and the crystal should be connected in parallel with two capacitors.

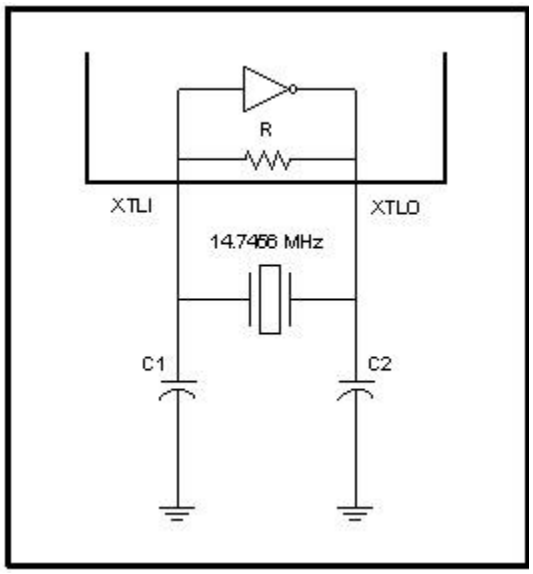

Figure 5-3 Crystal Oscillator as the Clock Source

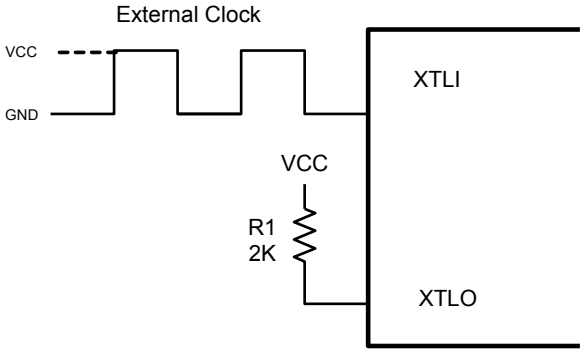

Figure 5-4 External Clock Source as the Clock Source

5.2.12. Baud Rate Generation

The built-in Baud Rate Generator (BRG) allows a wide range of input frequency and flexible Baud Rate generation. To obtain the desired Baud Rate, the user can set the Sample Clock Register (SCR), Divisor Latch Low Register (DLL), Divisor Latch High Register (DLH) and Clock Prescale Registers (CPRM and CPRN). The Baud Rate is generated according to the following equation:

$$BaudRate = \frac{InputFrequency}{Divisor * \Pr escaler}$$

The parameters in the equation above can be programmed by setting the "SCR", "DLL", "DLH", "CPRM" and "CPRN" registers according to the table below.

Table 5-2 Baud Rate Generator Setting

Setting	Description
Divisor	DLL + (256 * DLH)
Prescaler	$2^{M-1} * (SampleClock + N)$
SampleClock	$16 - SCR$, (SCR = '0h' to 'Ch')
M	CPRM, (CPRM = '01h' to '02h')
N	CPRN, (CPRN = '0h' to '7h')

To ensure the proper operation of the Baud Rate Generator, users should avoid setting the value '0' to Sample Clock, Divisor and Prescaler.

The following table lists some of the commonly used Baud Rates and the register settings that generate a specific Baud Rate. The examples assume an Input Clock frequency of 14.7456 Mhz. The SCR register is set to '0h', and the CPRM and CPRN registers are set to '1h' and '0h' respectively. In these examples, the Baud Rates can be generated by different combination of the DLH and DLL register values.

Table 5-3 Sample Baud Rate Setting

Baud Rate	DLH	DLL
1,200	3h	00h
2,400	1h	80h
4,800	0h	C0h
9,600	0h	60h
19,200	0h	30h
28,800	0h	20h
38,400	0h	18h
57,600	0h	10h
115,200	0h	08h
921,600	0h	01h

6. PCI OPERATION

6.1. SUPPORTED PCI TRANSACTION

- Configuration access: The PI7C8952 responds to type 0 configuration reads and writes if the IDSEL signal is asserted and the bus address is selecting function 0 registers. Any other configuration transaction will be ignored.
- I/O read/writes: The address is compared with the addresses reserved in the I/O Base Address Registers (BARs) to decide if the transaction should be ignored (Master abort). Only I/O byte accesses are possible. If multiple bytes is enabled during I/O transaction, only the first byte is valid and all other bytes are ignored.
- Memory reads/writes: The address is compared with the addresses reserved in the Mem Base Address Register. If the memory transaction is targeting to the registers, only first byte is valid and all other bytes are ignored and device will complete the burst transaction as disconnect-with-data. If the memory transaction is targeting to FIFOs, burst (multiple Dword) transaction is supported.
- All other cycles (64-bit, special cycles, reserved encoding etc.) are ignored.
- The PI7C8952 performs medium-speed address decoding as defined by the PCI specification. The Fast back-to-back transactions are supported.
- The PI7C8952 performs parity generation and checking on all PCI bus transactions as defined by PCI spec. If a parity error occurs during the PCI bus address phase, the device will report the error in the standard way by asserting the SERR# bus signal.

6.2. REGISTER TYPES

REGISTER TYPE	DEFINITION
RO	Read Only
RW	Read / Write
RWC	Read / Write 1 to Clear

6.3. CONFIGURATION REGISTERS

The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Master Latency Timer	Cache Line Size	0Ch
IO BAR Register				10h
MEM BAR Register				14h
Reserved				18h~2Bh
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Capability Pointer				34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – D8h
EEPROM Data		EEPROM Address	EEPROM Control / Status	DCh
Reserved				E0h - FCh

6.3.1. VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.

6.3.2. DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this I/O bridge as the PI7C8952. The default value may be changed by auto-loading from EEPROM. Reset to 8952h.

6.3.3. COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. Reset to 0b.
1	Memory Space Enable	RW	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to response to memory Space accesses. Reset to 0b.
2	Bus Master Enable	RO	It is not implemented. Hardwired to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	Controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error Status bit when an error is detected. Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI. Must be hardwired to 0b.
8	SERR# enable	RW	This bit, when set, enables the assertion of SERR# when detected System Error by the device. Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of the I/O bridge to generate INTx interrupt Messages. Reset to 0b.
15:11	Reserved	RO	Reset to 00000b.

6.3.4. STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000b.
19	Interrupt Status	RO	Indicates that an INTx interrupt Message is pending internally to the device. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
20	Capabilities List	RO	RO as 0b.
21	66MHz Capable	RO	Reset to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	RO as 1b.
24	Master Data Parity Error	RWC	It is not implemented. Hardwired to 0b.
26:25	DEVSEL# Timing	RO	Reset to 01b.
27	Signaled Target Abort	RWC	This bit does not apply to UART device.
28	Received Target Abort	RWC	It is not implemented. Hardwired to 0b.
29	Received Master Abort	RWC	Reset to 0b.
30	Signaled System Error	RWC	Reset to 0b.
31	Detected Parity Error	RWC	Reset to 0b.

6.3.5. REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of the I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 00h.

6.3.6. CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 02h to indicate no programming interfaces have been defined for PCI-to-PCI bridges
23:16	Sub-Class Code	RO	Read as 00h to indicate device is PCI-to-PCI bridge
31:24	Base Class Code	RO	Read as 07h to indicate device is a bridge device

6.3.7. CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system to system cache line size. This field is implemented by PCI devices as a RW field for legacy compatibility purposes but has no impact on any PCI device functionality. Reset to 00h.

6.3.8. MASTER LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Latency timer	RO	Does not apply to PCI. Must be hardwired to 00h.

6.3.9. HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 00h to indicate that the register layout conforms to the standard PCI-to-PCI bridge layout. Reset to 00h.
31:24	Reserved	RO	Reset to 00h

6.3.10. BASE ADDRESS REGISTER 0 – OFFSET 10h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Base Address 0	RW	Use this I/O base address to map the UART 16550 compatible registers. The base address can be allocated to 64 Bytes. Reset to 00000001h.

6.3.11. BASE ADDRESS REGISTER 1 – OFFSET 14h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Base Address 1	RW	Use this memory base address to map the UART 16550 compatible and enhanced registers. The base address can be allocated to 4096 Bytes. Reset to 00000000h

6.3.12. SUBSYSTEM VENDOR REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Sub Vendor ID	RO	Indicates the sub-system vendor id. The default value may be changed by auto-loading from EEPROM. Reset to 0000h.

6.3.13. SUBSYSTEM ID REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Sub System ID	RO	Indicates the sub-system device id. The default value may be changed by auto-loading from EEPROM. Reset to 0000h.

6.3.14. CAPABILITIES POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capabilities Pointer	RO	This optional register points to a linked list of new capabilities implemented by the device. This default value may be changed by auto-loading from EEPROM. The default value is 00h.
31:8	Reserved	RO	Reset to 000000h.

6.3.15. INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. Reset to 00h.

6.3.16. INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	Identifies the legacy interrupt Message(s) the device uses. Reset to 01h.
31:16	Reserved	RO	Reset to 0000h.

6.3.17. EEPROM CONTROL REGISTER – OFFSET DCh

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
1	Reserved	RO	Reset to 0b.
2	EEPROM Preload Control	RW	Enable preload start. Reset to 0b.
4:3	EEPROM Operation Command	RW	EEPROM Operation Command. 00b: Reserved 01b: Write operation command 10b: Read operation command 11b: Reserved Reset to 00b.
5	Operation Status	RO	When set indicates EEPROM access is ongoing
7:6	Preload Status	RO	EEPROM preload status after finish: 00b: reserved 01b: EEPROM is disabled 10b: EEPROM does not have correct check code 11b: EEPROM data is preloaded normally
15:8	EEPROM Address	RW	EEPROM word address
31:16	EEPROM Write DATA Buffer	RW	EEPROM write data buffer register. Reset to 0000h.

7. UART REGISTER DESCRIPTION

7.1. REGISTER TYPES

REGISTER TYPE	DEFINITION
RO	Read Only
WO	Write Only
RW	Read / Write
WOS	Write 1 to Clear

7.2. REGISTERS IN I/O MODE

Each UART channel has a dedicated 8-byte register block in I/O mode. The register block can be accessed by the UART I/O Base Address, which is obtained by adding the UART Register Offset to the content of the Base Address Register 0 (BAR0). The following diagram shows the arrangement of individual UART register blocks.

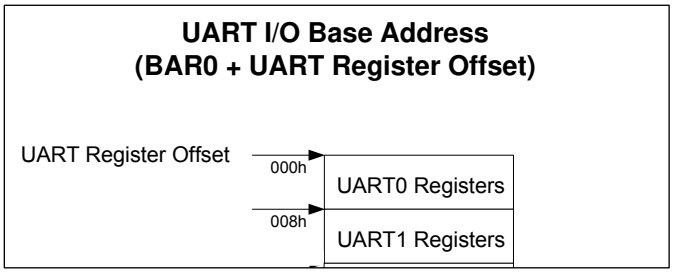

Figure 7-1 UART Register Block Arrangement in I/O Mode

Table 7-1 UART Base Address in I/O Mode

UART	UART I/O Base Address
UART0	BAR0 + 000h
UART1	BAR0 + 008h

Each register in the UART Register Block can be access by adding an offset to the UART I/O Base Address. The following table lists the arrangement of the registers in the UART Register Block in I/O mode.

Table 7-2 Registers in I/O Mode

Offset	Register Name	Mnemonic	Register Type
UART I/O Base Address + 00h	Receive Holding Register	RHR	RO
UART I/O Base Address + 00h	Transmit Holding Register	THR	WO
UART I/O Base Address + 01h	Interrupt Enable Register	IER	RW
UART I/O Base Address + 02h	Interrupt Status Register	ISR	RO
UART I/O Base Address + 02h	FIFO Control Register	FCR	WO
UART I/O Base Address + 03h	Line Control Register	LCR	RW
UART I/O Base Address + 04h	Modem Control Register	MCR	RW
UART I/O Base Address + 05h	Line Status Register	LSR	RO
UART I/O Base Address + 06h	Modem Status Register	MSR	RO
UART I/O Base Address + 07h	Special Function register	SFR	RW
Additional Standard Registers (Required LCR[7] = 1)			
UART I/O Base Address + 00h	Division Latch Low	DLL	RW
UART I/O Base Address + 01h	Division Latch High	DLH	RW
UART I/O Base Address + 02h	Sample Clock Register	SCR	RW