Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PI7C9X112SL

PCI Express-to-PCI Bridge

Datasheet

January 2017

Revision 1.4

A Product Line of Diodes Incorporated

1545 Barber Lane Milpitas, CA 95035
Telephone: 408-232-9100
FAX: 408-434-1040
Internet: http://www.diodes.com

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the
failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com

REVISION HISTORY

DATE	REVISION #	DESCRIPTION
09/27/2008	0.2	Preliminary release of PI7C9X112SL datasheet
04/28/2009	0.3	Revised General Features and Part Ordering Info
09/10/2009	1.0	Production release of PI7C9X112SL datasheet
11/10/2009	1.1	Updated Section 2.2 PCI Express Signal Section
02/09/2010	1.2	Removed reverse mode related description
04/21/2016	1.3	Updated Section 2.5 JTAG Boundary Scan Signals
01/25/2017	1.4	Updated Logo Added Table 14-4 PCI Express Interface - Differential Transmitter (TX) Output Characteristics Added Table 14-5 PCI Express Interface - Differential Receiver (RX) Input Characteristics Added Section 14.4 Operating Ambient Temperature Updated Section 2.8 Pin Assignments Updated Section 14.1 Absolute Maximum Ratings Updated Section 14.2 DC Specifications

PREFACE

The datasheet of PI7C9X112SL will be enhanced periodically when updated information is available. The technical information in this datasheet is subject to change without notice. This document describes the functionalities of PI7C9X112SL (PCI Express Bridge) and provides technical information for designers to design their hardware using PI7C9X112SL.

TABLE OF CONTENTS

TABLE OF FIGURES

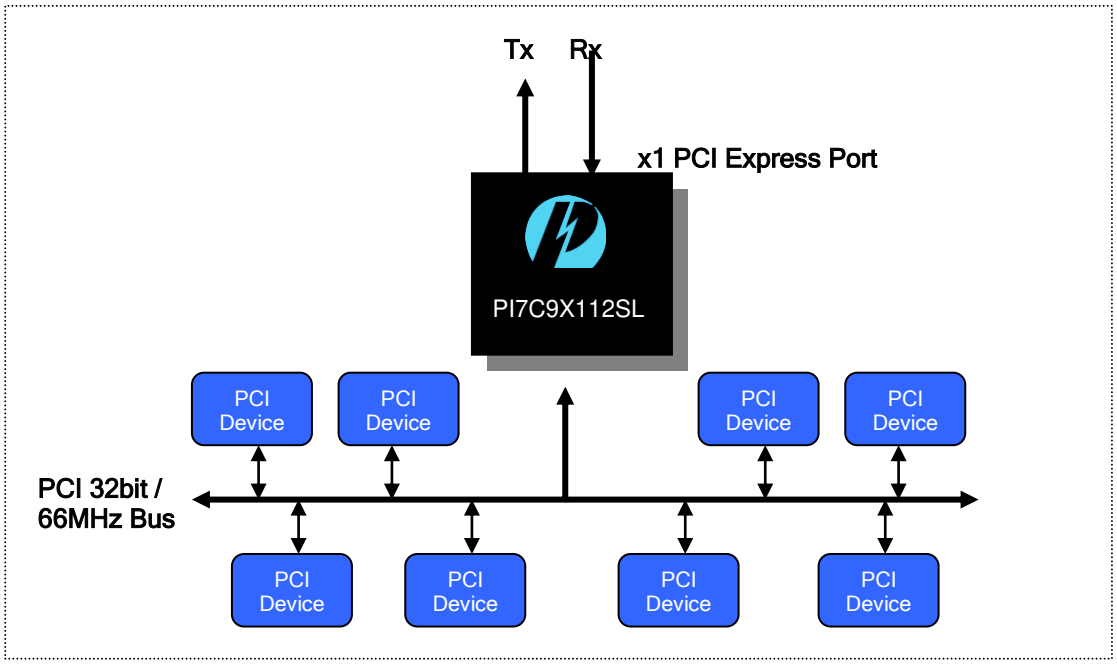
LIST OF TABLES

This page intentionally left blank.

1 INTRODUCTION

PI7C9X112SL is a PCIe-to-PCI bridge. PI7C9X112SL is compliant with the *PCI Express Base Specification,* Revision 1.1, the *PCI Express Card Electromechanical Specification*, Revision 1.1, the *PCI Local Bus Specification,* Revision 3.0 and *PCI Express to PCI Bridge Specification*, Revision 1.0. PI7C9X112SL supports forward transparent mode operation. PI7C9X112SL has an x1 PCI Express upstream port and a 32-bit PCI downstream port. The 32-bit PCI downstream port is 66MHz capable (see figure 1-1). PI7C9X112SL configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software and firmware is needed for the original operation.

Figure 1-1 PI7C9X112SL Topology



1.1 PCI EXPRESS FEATURES

- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express Card Electromechanical Specification, Revision 1.1
- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Physical Layer interface (x1 link with 2.5Gb/s data rate)
- Lane polarity toggle
- Virtual Isochronous support (upstream TC1-7 generation, downstream TC1-7 mapping)
- ASPM support
- Beacon support
- CRC (16-bit), LCRC (32-bit)
- ECRC and advanced error reporting
- PRBS (Pseudo Random Bit Sequencing) generator/checker for chip testing
- Maximum payload size to 512 bytes

1.2 PCI FEATURES

- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Bus PM Interface Specification, Revision 1.1
- Compliant with PCI Hot-Plug Specification, Revision 1.1
- Compliant with PCI Mobile Design Guide, Version 1.1
- 3.3V PCI signaling with 5V I/O tolerance
- Provides two level arbitration support for eight PCI Bus masters using external 4-to-8 de-mux circuit (ie: 74LVC138A).
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support

1.3 GENERAL FEATURES

- Compliant with Advanced Configuration and Power Interface Specification (ACPI), Revision 2.0b
- Compliant with System Management (SM) Bus, Version 2.0
- Forward bridging (PCI Express as primary bus, PCI as secondary bus)
- Transparent mode support
- GPIO support (4 bi-directional pins)
- Power Management (including ACPI, CLKRUN_L,CLKREQ_L, PCI_PM)
- EEPROM (I2C) Interface
- SM Bus Interface
- Auxiliary powers (VAUX, VDDAUX, VDDCAUX) support
- Power consumption less than 0.45 Watt in typical condition
- Industrial temperature range (-40C to 85C)

2 PIN DEFINITIONS

2.1 SIGNAL TYPES

TYPE OF SIGNAL	- DESCRIPTIONS
B	**Bi-directional**
I	**Input**
IU	**Input with pull-up**
ID	**Input with pull-down**
IOD	**Bi-directional with open drain output**
OD	**Open drain output**
O	**Output**
P	**Power**
G	**Ground**

2.2 PCI EXPRESS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
REFCLKP REFCLKN	7 9	I	**Reference Clock Inputs:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors.
RP RN	17 18	I	**PCI Express data inputs:** Differential data receiver input signals
TP TN	14 13	O	**PCI Express data outputs:** Differential data transmitter output signals
PERST_L	36	I	**PCI Express Fundamental Reset:** PI7C9X112SL uses this reset to initialize the internal state machines.

2.3 PCI SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
AD [31:0]	125, 123, 124, 121, 120, 119, 118, 116, 114, 113, 110, 109, 108, 107, 105, 104, 89, 87, 86, 85, 84, 83, 82, 80, 77, 76, 74, 73, 72, 71, 69, 68	B	**Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of CLKOUT[0] when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X112SL drives AD to a valid logic level when arbiter is parked to PI7C9X112SL on PCI bus.
CBE_L[3:0]	115, 102, 90, 79	B	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X112SL drives CBE [3:0] signals to a valid logic level when arbiter is parked to PI7C9X112SL on PCI bus.
PAR	93	B	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [31:0], CBE [3:0]. If PI7C9X112SL is an initiator with a write transaction, PI7C9X112SL will tri-state PAR. If PI7C9X112SL is a target and a write transaction, PI7C9X112SL will drive PAR one clock after the address or data phase. If PI7C9X112SL is a target and a read transaction, PI7C9X112SL will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X112SL drives PAR to a valid logic level when arbiter is parked to PI7C9X112SL on PCI bus.
FRAME_L	66	B	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME_L indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.
IRDY_L	99	B	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
TRDY_L	100	B	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
			not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
DEVSEL_L	98	B	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, PI7C9X112SL waits for the assertion of this signal within 5 cycles of FRAME_L assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.
STOP_L	95	B	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a de-asserted state for one cycle.
LOCK_L	96	B	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. PI7C9X112SL does not support any upstream LOCK transaction.
IDSEL	64	I	**Initialization Device Select:** Used as a chip select line for Type 0 configuration access to bridge's configuration space.
PERR_L	92	B	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
SERR_L	63	IOD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error. If SERR control is enabled, PI7C9X112SL will assert SERR_L. ▪ Address parity error ▪ Posted write data parity error on target bus ▪ Master abort during posted write transaction ▪ Target abort during posted write transaction ▪ Posted write transaction discarded ▪ Delayed write request discarded ▪ Delayed read request discarded ▪ Delayed transaction master timeout ▪ Errors reported from PCI Express port (advanced error reporting) in transparent mode. This signal is an open drain buffer that requires an external pull-up resistor for proper operation.
REQ_L [3:0]	40, 38, 37, 35	I	**Request (Active LOW):** REQ_L's are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ_Ls for at least 2 PCI clock cycles before asserting them again. PI7C9X112SL does not support external arbitor. When powered up, if both REQ_L2 and REQ_L3 and pulled low (Active LOW) and stay low in normal operation, the PI7C9X112SL will change the function of CLKOUT[3]to CLKRUN and CLKOUT[2] to CLKREQ, respectively.
GNT_L [3:0]	44, 43, 42, 41	O	**Grant (Active LOW):** To support arbitration of 8 PCI Master Devices, GNT_L[3:0] signals are to be connected to an external demux (i.e. 74LVC138A) with GNT_[3] connected to E3; GNT_L[2] to A2; GNT_L[1] to A1 and GNT_L[0] to A0 and connect output pins of 74LVC138A to 8 PCI Master Devices.
CLKOUT [3:0]	52,56,59,58	O	**PCI Clock Outputs:** PCI clock outputs are derived from the CLKIN and provide clocking signals to external PCI Devices.
M66EN	103	I	**66MHz Enable:** This input is used to specify if Bridge is capable of running at 66MHz. For 66MHz operation on the PCI bus, this signal should be pulled "HIGH". For 33MHz operation on the PCI bus, this signal should be pulled LOW.
RESET_L	49	B	**RESET_L (Active LOW):** When RESET_L active, all PCI signals should be asynchronously tri-stated.
INTA_L INTB_L INTC_L INTD_L	39 47 62 61	IOD	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA_L, INTB_L, INTC_L, INTD_L signals are inputs and asynchronous to the clock.
CLKIN	48	I	**PCI Clock Input:** PCI Clock Input Signal connects to an external clock source. The PCI Clock Outputs CLKOUT [3:0] pins are derived from CLKIN Input.

2.4 MODE SELECT AND STRAPPING SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TM0	127	I	**Mode Select 0:** Mode Selection Pin to select EEPROM or SM Bus. TM0=0 for EEPROM (I2C) support and TM0=1 for SM Bus support. TM0 is also a strapping pin. See table 3-1 mode selection and 3-2 for strapping control.
TM1	26	I	**Mode Select 1:** Mode Selection Pin for normal operation. Set TM1=0 for normal operation. TM1=1 is reserved.
MSK_IN	126	I	Hot Plug Enable input.
RESERVED 0	31	I	**Reserved 0:** This pin should be tied low for normal operation.

2.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TCK	28	IU	**Test Clock:** TCK is the test clock to synchronize the state information and data on the PCI bus side of PI7C9X112SL during boundary scan operation. At normal operation mode, this pin should be left open(NC).
TMS	27	IU	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.
TDO	32	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. At normal operation mode, this pin should be left open(NC).
TDI	29	IU	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the PCI side of PI7C9X112SL. At normal operation mode, this pin should be left open(NC).
TRST_L	30	IU	**Test Reset (Active LOW):** TRST_L is the test reset to initialize the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.

2.6 MISCELLANEOUS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
GPIO [3:0]	50, 51, 54, 55	B	**General Purpose I/O Data Pins:** GPIO[3:0] pins are utilized as REQ_L[7:4] coupled with REQ_L[3:0] to provide arbitration of 8 PCI Master Devices.
SMBCLK / SCL	3	B	**SMBUS / EEPROM Clock Pin:** When EEPROM (I2C) interface is selected (TM0=0), this pin is an output of SCL clock and connected to EEPROM clock input. When SMBUS interface is selected (TM0=1), this pin is an input for the clock of SMBUS.
SMBDATA / SDA	4	B/IOD	**SMBUS / EEPROM Data Pin:** Data Interface Pin to EERPOM or SMBUS. When EEPROM (I2C) interface is selected (TM0=0), this pin is a bi-directional signal. When SMBUS interface is selected (TM0=1), this pin is an open drain signal.
PME_L	1	B	**Power Management Event Pin:** Power Management Event Signal is asserted to request a change in the device or link power state.

2.7 POWER AND GROUND PINS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDA	8, 20, 21	P	**Analog Voltage Supply for PCI Express Interface:** Connect to the 1.0V Power Supply.
VDDP	11, 23, 24	P	**Digital Voltage Supply for PCI Express Interface:** Connect to the 1.0V Power Supply.
VDDAUX	15	P	**Auxiliary Voltage Supply for PCI Express Interface:** Connect to the 1.0V Power Supply.
VTT	12	P	**Termination Supply Voltage for PCI Express Interface:** Connect to the 1.5V Power Supply.
VDDC	45, 65, 75, 94, 112	P	**Core Supply Voltage:** Connect to the 1.0V Power Supply.
VDDCAUX	5	P	**Auxiliary Core Supply Voltage:** Connect to the 1.0V Power Supply.
VD33	33, 53, 60, 70, 81, 91, 101, 111, 122	P	**I/O Supply Voltage for PCI Interface:** Connect to the 3.3V Power Supply for PCI I/O Buffers.
VAUX	2	P	**Auxiliary I/O Supply Voltage for PCI interface:** Connect to the 3.3V Power

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
			Supply.
VSS	6, 10, 16, 19, 22, 46, 34, 57, 67, 78, 88, 97, 106, 117, 128, 129	P	**Ground:** Connect to Ground.

2.8 PIN ASSIGNMENTS

Table 2-1 Pin Assignments

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	PME_L	34	VSS	67	VSS	100	TRDY_L
2	VAUX	35	REQ_L[0]	68	AD[0]	101	VD33
3	SMBCLK / SCL	36	PERST_L	69	AD[1]	102	CBE_L[2]
4	SMDAT / SDA	37	REQ_L[1]	70	VD33	103	M66EN
5	VDDCAUX	38	REQ_L[2]	71	AD[2]	104	AD[16]
6	VSS	39	INTA_L	72	AD[3]	105	AD[17]
7	REFCLKP	40	REQ_L[3]	73	AD[4]	106	VSS
8	VDDA	41	GNT_L[0]	74	AD[5]	107	AD[18]
9	REFCLKN	42	GNT_L[1]	75	VDDC	108	AD[19]
10	VSS	43	GNT_L[2]	76	AD[6]	109	AD[20]
11	VDDP	44	GNT_L[3]	77	AD[7]	110	AD[21]
12	VTT	45	VDDC	78	VSS	111	VD33
13	TXN	46	VSS	79	CBE[0]	112	VDDC
14	TXP	47	INTB_L	80	AD[8]	113	AD[22]
15	VDDAUX	48	CLKIN	81	VD33	114	AD[23]
16	VSS	49	RESET_L	82	AD[9]	115	CBE_L[3]
17	RXP	50	GPIO[3]	83	AD[10]	116	AD[24]
18	RXN	51	GPIO[2]	84	AD[11]	117	VSS
19	VSS	52	CLKOUT[3]	85	AD[12]	118	AD[25]
20	VDDA	53	VD33	86	AD[13]	119	AD[26]
21	VDDA	54	GPIO[1]	87	AD[14]	120	AD[27]
22	VSS	55	GPIO[0]	88	VSS	121	AD[28]
23	VDDP	56	CLKOUT[2]	89	AD[15]	122	VD33
24	VDDP	57	VSS	90	CBE_L[1]	123	AD[30]
25	VSS	58	CLKOUT[0]	91	VD33	124	AD[29]
26	TM1	59	CLKOUT[1]	92	PERR_L	125	AD[31]
27	TMS	60	VD33	93	PAR	126	MSK_IN
28	TCK	61	INTD_L	94	VDDC	127	TM0
29	TDI	62	INTC_L	95	STOP_L	128	VSS
30	TRST_L	63	SERR_L	96	LOCK_L	129	Center pad
31	RESERVED 0	64	IDSEL	97	VSS		
32	TDO	65	VDDC	98	DEVSEL_L		
33	VD33	66	FRAME_L	99	IRDY_L		

3 MODE SELECTION AND PIN STRAPPING

3.1 FUNCTIONAL MODE SELECTION

PI7C9X112SL uses TM1 and TM0 pins to select different modes of operations. These two input signals are required to be stable during normal operation. One of the two combinations of normal operation can be selected by setting the logic values using the two mode select pins. For example, if the logic values are low for TM1 and TM0 pins, the normal operation will have EEPROM (I2C) support with internal arbiter. The designated operation with respect to the values of the TM1 and TM0 pins are defined on Table 3-1:

Table 3-1 Mode Selection

TM1	TM0	Functional Mode
0	0	EEPROM (I2C) support
0	1	SM Bus support

3.2 PIN STRAPPING

If TM1 is strapped to low, PI7C9X112SL uses REQ_L[3:2] as the strapping pins during PCIe PERST# de-assertion to enable Clock Power Management feature.

Table 3-2 Pin Strapping

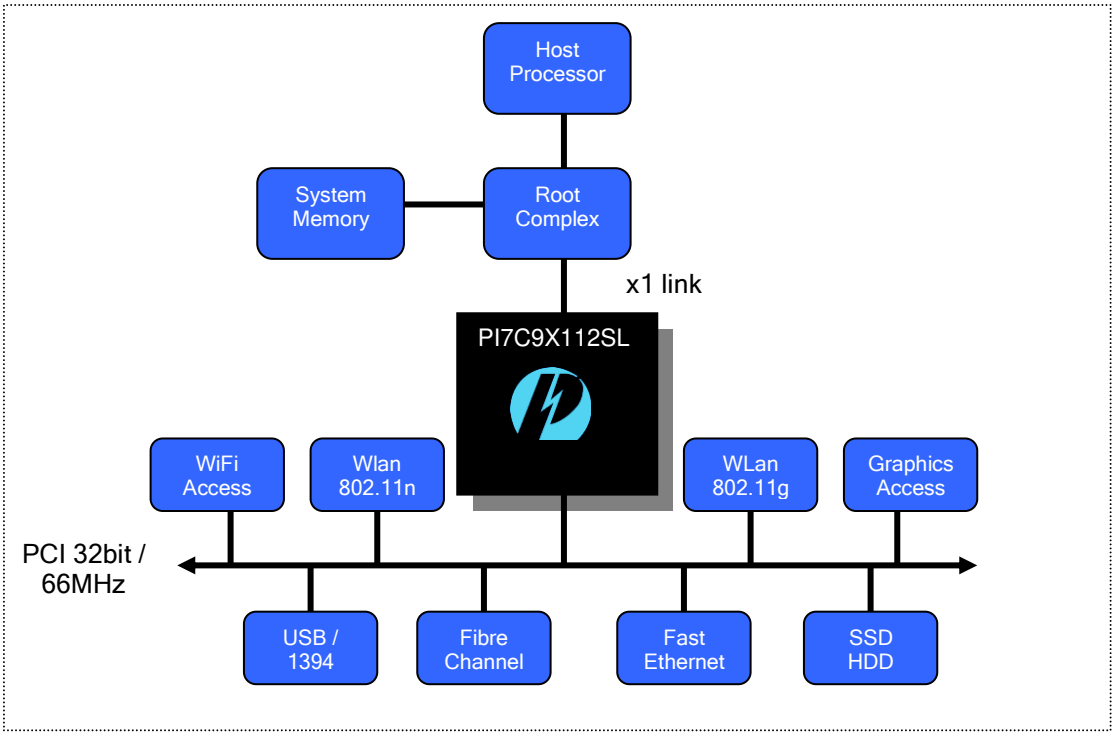
TM1 Strapped	REQ_L[3:2]	Test Functions
0	2'b0	Clock Power Management is enabled, only two PCI devices supported. CLKOUT[2] is used as CLKREQ# CLKOUT[3] is used as CLKRUN#

4 FORWARD (PCIe to PCI) BRIDGING

PI7C9X112SL supports forward mode operation. For example, when PI7C9X112SL is operating in forward PCIe Bridge, its PCI Express interface is connected to a root complex and its PCI bus interface is connected to PCI Master devices.

PCI based systems and peripherals are ubiquitous in the I/O interconnect technology market today. It will be a tremendous effort to convert existing PCI based products to PCI Express systems. PI7C9X112SL provides the drop-in bridging solution to interface legacy PCI I/O Devices to PCI Express Root Complex.

Figure 4-1 Forward Bridging



4.1 TLP STRUCTURE

PCI Express TLP (Transaction Layer Packet) Structure is comprised of format, type, traffic class, attributes, TLP digest, TLP poison, and length of data payload.

There are four TLP formats defined in PI7C9X112SL based on the states of FMT [1] and FMT [0] as shown on Table 4-1.

Table 4-1 TLP Format

FMT [1]	FMT [0]	TLP Format
0	0	3 double word, without data
0	1	4 double word, without data
1	0	3 double word, with data
1	1	4 double word, with data

Data payload of PI7C9X112SL can range from 4 (1DW) to 256 (64DW) bytes. PI7C9X112SL supports three TLP routing mechanisms. They are comprised of Address, ID, and Implicit routings. Address routing is being used for Memory and IO requests. ID based (bus, device, function numbers) routing is being used for configuration requests. Implicit routing is being used for message routing. There are two message groups (baseline and advanced switching). The baseline message group contains INTx interrupt signaling, power management, error signaling, locked transaction support, slot power limit support, vendor defined messages, hot-plug signaling. The other is advanced switching support message group. The advanced switching support message contains data packet and signal packet messages. Advanced switching is beyond the scope of PI7C9X112SL implementation.

The r [2:0] values of the "type" field will determine the destination of the message to be routed. All baseline messages must use the default traffic class zero (TC0).

4.2 VIRTUAL ISOCHRONOUS OPERATION

This section provides a summary of Virtual Isochronous Operation supported by PI7C9X112SL. Virtual Isochronous support is disabled by default. Virtual Isochronous feature can be turned on with setting bit [26] of offset 40h to one. Control bits are designated for selecting which traffic class (TC1-7) to be used for upstream (PCI Express-to-PCI). PI7C9X112SL accepts only TC0 packets of configuration, IO, and message packets for downstream (PCI Express-to-PCI). If configuration, IO and message packets have traffic class other than TC0, PI7C9X112SL will treat them as malformed packets. PI7C9X112SL maps all downstream memory packets from PCI Express to PCI transactions regardless the virtual Isochronous operation is enabled or not.

5 CONFIGURATION REGISTER ACCESS

PI7C9X112SL supports Type-0 and Type-1 configuration space headers and Capability ID of 01h (PCI power management) to 10h (PCI Express capability structure).

With pin REVRSB = 0, device-port type (bit [7:4]) of capability register will be set to 7h (PCI Express-to-PCI). When pin REVRSB = 1, device-port type (bit [7:4]) of capability register will be set to 8h (PCI-to-PCI Express bridge).

PI7C9X112SL supports PCI Express capabilities register structure with capability version set to 1h (bit [3:0] of offset 02h).

5.1 CONFIGURATION REGISTER MAP

PI7C9X112SL supports capability pointer with PCI power management (ID=01h), PCI bridge sub-system vendor ID (ID=0Dh), PCI Express (ID=10h), vital product data (ID=03h), and message signaled interrupt (ID=05h). Slot identification (ID=04h) is off by default and can be turned on through configuration programming.

Table 5-1 Configuration Register Map (00h – FFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
01h - 00h	Vendor ID	Yes1	Yes2
03h – 02h	Device ID	Yes1	Yes2
05h – 04h	Command Register	Yes	Yes
07h – 06h	Primary Status Register	Yes	Yes
0Bh – 08h	Class Code and Revision ID	Yes1	Yes2
0Ch	Cacheline Size Register	Yes	Yes
0Dh	Primary Latency Timer	Yes	Yes
0Eh	Header Type Register	Yes	Yes
0Fh	Reserved	-	-
17h – 10h	Reserved	-	-
18h	Primary Bus Number Register	Yes	Yes
19h	Secondary Bus Number Register	Yes	Yes
1Ah	Subordinate Bus Number Register	Yes	Yes
1Bh	Secondary Latency Timer	Yes	Yes
1Ch	I/O Base Register	Yes	Yes
1Dh	I/O Limit Register	Yes	Yes
1Fh – 1Eh	Secondary Status Register	Yes	Yes
21h – 20h	Memory Base Register	Yes	Yes
23h – 22h	Memory Limit Register	Yes	Yes
25h – 24h	Prefetchable Memory Base Register	Yes	Yes
27h – 26h	Prefetchable Memory Limit Register	Yes	Yes
2Bh – 28h	Prefetchable Memory Base Upper 32-bit	Yes	Yes

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
	Register		
2Dh – 2Ch	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
2Fh – 2Eh	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
31h – 30h	I/O Base Upper 16-bit Register	Yes	Yes
33h – 32h	I/O Limit Upper 16-bit Register	Yes	Yes
34h	Capability Pointer	Yes	Yes
37h – 35h	Reserved	No	Yes
3Bh – 38h	Reserved	No	Yes
3Ch	Interrupt Line	Yes	Yes
3Dh	Interrupt Pin	Yes	Yes
3Eh	Bridge Control	Yes	Yes
3Fh	Bridge Control	Yes	Yes
41h – 40h	PCI Data Prefetching Control	Yes	Yes
43h – 42h	Chip Control 0	Yes	Yes
45h – 44h	Reserved	-	-
47h – 46h	Reserved	-	-
4Bh – 48h	Arbiter Mode, Enable, Priority	-	-
4Ch	Reserved	-	-
4Dh	Reserved	-	-
4Eh	Reserved	-	-
4Fh	Reserved	-	-
53h – 50h	Reserved	-	-
57h – 54h	Reserved	-	-
5Bh – 58h	Reserved	-	-
5Fh – 5Ch	Reserved	-	-
63h – 60h	Reserved	-	-
67h – 64h	Reserved	-	-
69h – 68h	PCI Express Tx and Rx Control	Yes	Yes
6Ah	Reserved	-	-
6Bh	Upstream memory write/read control	Yes	Yes
6Dh – 6Ch	Reserved	-	-
6Fh – 6Eh	Reserved	-	-
73h – 70h	EEPROM (I2C) Control and Status Register	No	Yes
77h – 74h	Reserved	-	-
7Bh – 78h	GPIO Data and Control	Yes	Yes
7Ch	Reserved	-	-
7Dh	Reserved	-	-
7Eh	Reserved	-	-
7Fh	Reserved	-	-
83h – 80h	PCI-X Capability	Yes	Yes
87h – 84h	PCI-X Bridge Status	Yes	Yes
8Bh – 88h	Upstream Split Transaction	Yes	Yes
8Fh – 8Ch	Downstream Split Transaction	Yes	Yes
93h – 90h	Power Management Capability	Yes	Yes

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
97h – 94h	Power Management Control and Status	Yes	Yes
9Bh – 98h	Reserved	-	-
9Fh – 9Ch	Reserved	-	-
A3h – A0h	Slot ID Capability	Yes	Yes
A7h – A4h	Secondary Clock and CLKRUN Control	Yes	Yes
ABh – A8h	SSID and SSVID Capability	Yes	Yes
AFh – ACh	Subsystem ID and Subsystem Vendor ID	Yes	Yes
B3h – B0h	PCI Express Capability	Yes	Yes
B7h – B4h	Device Capability	Yes	Yes
BBh – B8h	Device Control and Status	Yes	Yes
BFh – BCh	Link Capability	Yes	Yes
C3h – C0h	Link Control and Status	Yes	Yes
C7h – C4h	Slot Capability	Yes	Yes
CBh – C8h	Slot Control and Status	Yes	Yes
CFh – CCh	XPIP Configuration Register 0	Yes	Yes
D3h – D0h	XPIP Configuration Register 1	Yes	Yes
D6h – D4h	XPIP Configuration Register 2	Yes	Yes
D7h	Hot Swap Switch debounce count	Yes	Yes
DBh – D8h	VPD Capability Register	Yes	Yes
DFh – DCh	VPD Data Register	Yes3	Yes
E3h – E0h	Extended Config Access Address	Yes	Yes
E7h – E4h	Extended Config Access Data	Yes	Yes
EBh – E8h	Reserved	-	-
EFh – ECh	Reserved	-	-
F3h – F0h	MSI Capability Register	Yes	Yes
F7h – F4h	Message Address	Yes	Yes
FBh – F8h	Message Upper Address	Yes	Yes
FFh – FCh	Message Date	Yes	Yes

Note 1: When masquerade is enabled, it is pre-loadable.
Note 2: The VPD data is read/write through I2C during VPD operation.
Note 3: Read access only.

5.2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP

PI7C9X112SL also supports PCI Express Extended Capabilities with from 257-byte to 4096-byte space. The offset range is from 100h to FFFh. The offset 100h is defined for Advance Error Reporting (ID=0001h). The offset 150h is defined for Virtual Channel (ID=0002h).

Table 5-2 PCI Express Extended Capability Register Map (100h – FFFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	Transparent Mode (type1)	EEPROM (I2C) Access	SM Bus Access
103h – 100h	Advanced Error Reporting (AER) Capability	Yes	Yes2
107h – 104h	Uncorrectable Error Status	No	Yes
10Bh – 108h	Uncorrectable Error Mask	Yes	Yes
10Fh – 10Ch	Uncorrectable Severity	No	Yes
113h – 110h	Correctable Error Status	No	Yes
117h – 114h	Correctable Error Mask	No	Yes
11Bh – 118h	AER Control	No	Yes
12Bh – 11Ch	Header Log Register	No	Yes
12Fh – 12Ch	Secondary Uncorrectable Error Status	No	Yes
133h – 130h	Secondary Uncorrectable Error Mask	No	Yes
137h – 134h	Secondary Uncorrectable Severity	No	Yes
13Bh – 138h	Secondary AER Control	No	Yes
14Bh – 13Ch	Secondary Header Log Register	No	Yes
14Fh – 14Ch	Reserved	No	Yes
153h – 150h	VC Capability	No	Yes
157h – 154h	Port VC Capability 1	No	Yes
15Bh – 158h	Port VC Capability 2	No	Yes
15Fh – 15Ch	Port VC Status and Control	No	Yes
163h – 160h	VC0 Resource Capability	No	Yes
167h – 164h	VC0 Resource Control	No	Yes
16Bh – 168h	VC0 Resource Status	No	Yes
2FFh – 170h	Reserved	No	No
303h – 300h	Extended GPIO Data and Control	No	Yes
307h – 304h	Extended GPI/GPO Data and Control	No	Yes
30Fh – 308h	Reserved	No	No
310h	Replay and Acknowledge Latency Timer	Yes	Yes
4FFh – 314h	Reserved	No	No
503h – 500h	Reserved	No	No
504h	Reserved	No	No
50Fh – 505h	Reserved	No	No
510h	Reserved	No	No
FFFh – 514h	Reserved	No	No

Note 5: Read access only.

5.3 PCI CONFIGURATION REGISTERS

The following section describes the configuration space when the device is in transparent mode. The descriptions for different register type are listed as follow:

Register Type	Descriptions
RO	Read Only
ROS	Read Only and Sticky
RW	Read/Write
RWC	Read/Write "1" to clear
RWS	Read/Write and Sticky
RWCS	Read/Write "1" to clear and Sticky

5.3.1 VENDOR ID – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. Returns 12D8h when read.

5.3.2 DEVICE ID – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X112SL. Returns E112 when read.

5.3.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0: Ignore I/O transactions on the primary interface 1: Enable response to memory transactions on the primary interface Reset to 0
1	Memory Space Enable	RW	0: Ignore memory read transactions on the primary interface 1: Enable memory read transactions on the primary interface Reset to 0
2	Bus Master Enable	RW	0: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on the secondary interface 1: Enable the bridge to operate as a master on the primary interfaces for memory and I/O transactions forwarded from the secondary interface. Reset to 0
3	Special Cycle Enable	RO	0: PI7C9X112SL does not respond as a target to Special Cycle transactions, so this bit is defined as Read-Only and must return 0 when read Reset to 0
4	Memory Write and Invalidate Enable	RO	0: PI7C9X112SL does not originate a Memory Write and Invalidate transaction. Implements this bit as Read-Only and returns 0 when read (unless forwarding a transaction for another master). Reset to 0
5	VGA Palette Snoop Enable	RO / RW	This bit is not supported by PI7C9X112SL. Reset to 0
6	Parity Error Response Enable	RW	0: May ignore any parity error that is detected and take its normal action 1: This bit if set, enables the setting of Master Data Parity Error bit in the Status Register when poisoned TLP received or parity error is detected and takes its normal action Reset to 0
7	Wait Cycle Control	RO	Wait cycle control not supported Reset to 0

BIT	FUNCTION	TYPE	DESCRIPTION
8	SERR_L Enable Bit	RW	0: Disable 1: Enable PI7C9X112SL to report non-fatal or fatal error message to the Root Complex. Reset to 0
9	Fast Back-to-Back Enable	RO	Fast back-to-back enable not supported Reset to 0
10	Interrupt Disable	RW	This bit is not supported by PI7C9X112SL. Reset to 0
15:11	Reserved	RO	Reset to 00000

5.3.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000
19	Reserved	RO	Reset to 0
20	Capability List Capable	RO	1: PI7C9X112SL supports the capability list (offset 34h in the pointer to the data structure) Reset to 1
21	66MHz Capable	RO	This bit is not supported by PI7C9X112SL. Reset to 0
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	This bit is not supported by PI7C9X112SL. Reset to 0
24	Master Data Parity Error Detected	RWC	Bit set if its Parity Error Enable bit is set and either of the conditions occurs on the primary: - Receives a completion marked poisoned - Poisons a write request Reset to 0
26:25	DEVSEL_L Timing (medium decode)	RO	These bits are not supported by PI7C9X112SL. Reset to 00
27	Signaled Target Abort	RWC	This bit is set when PI7C9X112SL completes a request using completer abort status on the primary Reset to 0
28	Received Target Abort	RWC	This bit is set when PI7C9X112SL receives a completion with completer abort completion status on the primary Reset to 0
29	Received Master Abort	RWC	This bit is set when PI7C9X112SL receives a completion with unsupported request completion status on the primary
30	Signaled System Error	RWC	This bit is set when PI7C9X112SL sends an ERR_FATAL or ERR_NON_FATAL message on the primary Reset to 0
31	Detected Parity Error	RWC	This bit is set when poisoned TLP is detected on the primary Reset to 0

5.3.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Reset to 00000000h

5.3.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Subtractive decoding of PCI-PCI bridge not supported Reset to 00000000
23:16	Sub-Class Code	RO	Sub-Class Code 00000100: PCI-to-PCI bridge Reset to 00000100
31:24	Base Class Code	RO	Base class code 00000110: Bridge Device Reset to 00000110

5.3.7 CACHE LINE SIZE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Bit [1:0] not supported Reset to 00
2	Cache Line Size	RW	1: Cache line size = 4 double words Reset to 0
3	Cache Line Size	RW	1: Cache line size = 8 double words Reset to 0
4	Cache Line Size	RW	1: Cache line size = 16 double words Reset to 0
5	Cache Line Size	RW	1: Cache line size = 32 double words Reset to 0
7:6	Reserved	RO	Bit [7:6] not supported Reset to 00

5.3.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency Timer	RO	8 bits of primary latency timer in PCI bus Reset to 00h

5.3.9 PRIMARY HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
22:16	PCI-to-PCI bridge configuration	RO RO	PCI-to-PCI bridge configuration (10 – 3Fh) Reset to 0000001
23	Single Function Device	RO	0: Indicates single function device Reset to 0
31:24	Reserved	RO	Reset to 00h

5.3.10 RESERVED REGISTERS – OFFSET 10h TO 17h