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PI7C9X113SL

PCI Express-to-PCI Bridge

Preliminary Datasheet
Revision 0.3

3545 North 1ST Street, San Jose, CA 95134
Phone: 1-877-PERICOM (1-877-737-4266)
FAX: 1-408-435-1100
Internet: http://www.pericom.com

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REVISION HISTORY

DATE	REVISION #	DESCRIPTION
5/27/2009	0.1	Preliminary Datasheet
9/15/2009	0.2	Updated Section 6.3 (I/O Limit Register – Offset 1Ch, Interrupt Line Register – Offset 3Ch, Arbiter Enable Register – Offset 48h, Memory ReadSmart Range Control Register – Offset 58h, Upstream Memory Read/Write Control Register – Offset 68h, XPIP Configuration Register 1 – Offset D0h) Updated Section 12 IEEE 1149.1 Compatible JTAG Controller (Removed TRST_L) Updated Table 14-2 DC Electrical Characteristics (VDDA)
7/26/2010	0.3	Updated Section 2 Pin Definitions (Pin 22 to NC) Updated Section 6.3 PCI Configuration Registers (Offset 40h, 44h, 6Ch, A4h, D0h, D4h) Updated VDDC and VDDA voltage to 1.1V (Section 2.7, Table 14-2)

PREFACE

The datasheet of PI7C9X113SL will be enhanced periodically when updated information is available. The technical information in this datasheet is subject to change without notice. This document describes the functionalities of PI7C9X113SL (PCI Express Bridge) and provides technical information for designers to design their hardware using PI7C9X113SL.

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TABLE OF FIGURES

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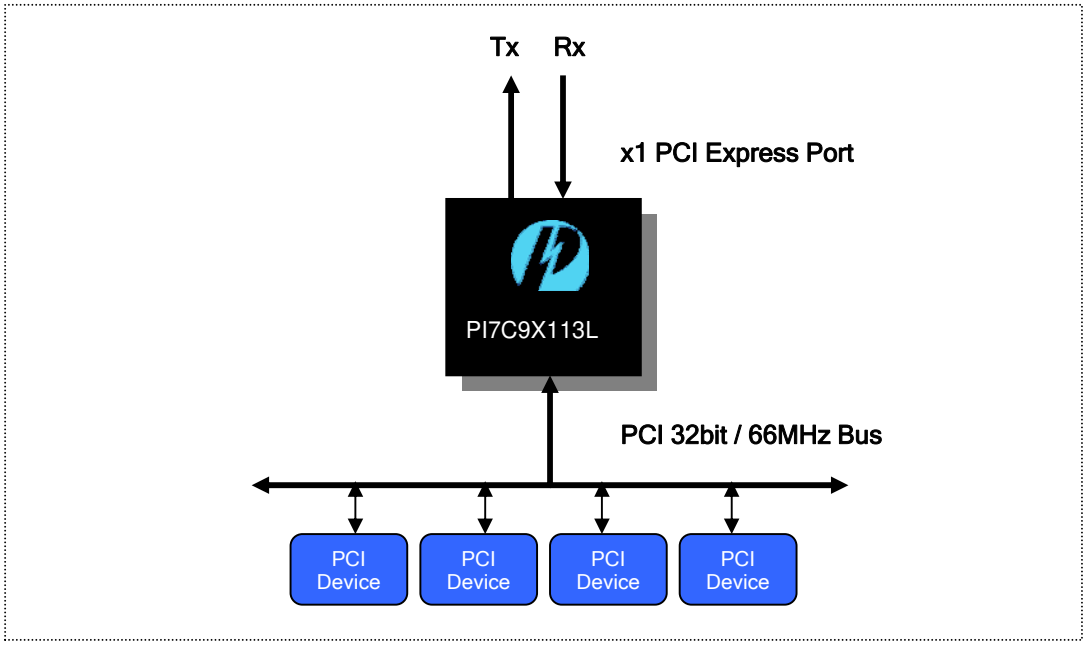
1 INTRODUCTION

PI7C9X113SL is a PCIe-to-PCI/PCI-X bridge. PI7C9X113SL is compliant with the *PCI Express Base Specification,* Revision 1.1, the *PCI Express Card Electromechanical Specification*, Revision 1.1, the *PCI Local Bus Specification,* Revision 3.0 and *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. PI7C9X113SL supports transparent mode operation and forward bridging. PI7C9X113SL has an x1 PCI Express upstream port and a 32-bit PCI downstream port. The 32-bit PCI downstream port is 66MHz capable (see **Figure 1-1**). PI7C9X113SL configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software and firmware is needed for the original operation.

Figure 1-1 PI7C9X113SL Topology



1.1 INDUSTRY SPECIFICATION COMPLIANCE

- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Compliant with PCI Express Card Electromechanical Specification, Revision 1.0a
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI SHPC and Subsystem Specification, Revision 1.0
- Compliant with PCI Mobile Design Guide, Version 1.1
- Compliant with PCI Bus PM Interface Specification, Revision 1.2
- Compliant with System Management (SM) Bus, Version 2.0
- Compliant with Advanced Configuration and Power Interface Specification (ACPI), Revision 2.0b

1.2 GENERAL FEATURES

- Forward bridging (PCI Express as primary bus, PCI as secondary bus)
- x1 PCI Express interface (2.5Gb/s data rate)
- 32-bit PCI interface capable of 66MHz
- GPIO support (4 bi-directional pins). When external arbiter is used, 3 additional GPI (input) and GPO (output) pins
- Power Management (including ACPI, PCI_PM, CLKRUN_L and CLKREQ_L,)
- Transparent mode support
- Subtractive Decoding PCI-to-PCI bridge to support legacy device
- Masquerade support (user-defined vendor, device, revision, subsystem device, and subsystem vendor ID)
- EEPROM (I2C) Interface
- SM Bus Interface
- 10k byte buffer: 2K byte buffer for downstream memory read, 4K bytes for upstream memory read, and 2K byte buffer for memory write in both directions
- Auxiliary powers (VAUX, VDDAUX, VDDCAUX) support
- Power consumption less than 350 mW in typical condition
- Extended commercial temperature range (0C to 85C)

1.3 PCI EXPRESS FEATURES

- Physical Layer interface (x1 link with 2.5Gb/s data rate)
- Virtual Isochronous support (upstream TC1-7 generation, downstream TC1-7 mapping)
- CRC (16-bit), LCRC (32-bit)
- ECRC and advanced error reporting
- Lane polarity toggle
- ASPM support
- WAKE_L support
- Maximum payload size to 512 bytes
- CLKREQ_L support to disable Refclk at L1 and L2 state

1.4 PCI FEATURES

- Provides two level arbitration support for four PCI Bus masters
- 3.3V PCI signaling with 5V I/O tolerance
- PME_L support
- LOCK support
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support
- Adaptive fragmentation support for memory write
- Internal clock generator for PCI bus
- CLKRUN_L support to stop the PCI clock

2 PIN DEFINITIONS

2.1 SIGNAL TYPES

TYPE OF SIGNAL	- DESCRIPTIONS
B	Bi-directional
I	Input
IU	Input with pull-up
ID	Input with pull-down
IOD	Bi-directional with open drain output
OD	Open drain output
O	Output
P	Power
G	Ground

"_L" in signal name indicates Active LOW signal

2.2 PCI EXPRESS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
REFCLKP REFCLKN	13, 12	I	**Reference Clock Inputs:** Connect to external 100MHz differential clock.
RP RN	21, 20	I	**PCI Express Data Inputs:** Differential data receiver input signals
TP TN	17, 16	O	**PCI Express Data Outputs:** Differential data transmitter output signals
PERST_L	29	I	**PCI Express Fundamental Reset (Active LOW):** PI7C9X113SL The device uses this signal reset to initialize the internal state machines.

2.3 PCI SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
AD [31:0]	125, 126, 124, 121, 122, 120, 119, 117, 113, 111, 110, 109, 108, 106, 103, 104, 90, 88, 86, 85, 83, 80, 79, 78, 75, 74, 71, 70, 68, 69, 67, 64	B	**Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of CLKOUT[0] when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X113SL drives AD to a valid logic level when arbiter is parking to PI7C9X113SL on PCI bus.
CBE_L[3:0]	116, 99, 89, 76	B	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X113SL drives CBE [3:0] signals to a valid logic level when arbiter is parking to PI7C9X113SL on PCI bus.
PAR	94	B	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [31:0], CBE [3:0]. If PI7C9X113SL is an initiator with a write transaction, PI7C9X113SL will tri-state PAR. If PI7C9X113SL is a target and a write transaction, PI7C9X113SL will drive PAR one clock after the address or data phase. If PI7C9X113SL is a target and a read transaction, PI7C9X113SL will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X113SL drives PAR to a valid logic level when arbiter is parking to PI7C9X113SL on PCI bus.
FRAME_L	63	B	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME_L indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
IRDY_L	97	B	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
TRDY_L	100	B	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
DEVSEL_L	98	B	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, PI7C9X113SL waits for the assertion of this signal within 5 cycles of FRAME_L assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.
STOP_L	96	B	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a de-asserted state for one cycle.
LOCK_L	93	B	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. PI7C9X113SL does not support any upstream LOCK transaction.
PERR_L	92	B	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
SERR_L	61	IOD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error condition. If SERR control is enabled, PI7C9X113SL will drive this pin on: ▪ Address parity error ▪ Posted write data parity error on target bus ▪ Master abort during posted write transaction ▪ Target abort during posted write transaction ▪ Posted write transaction discarded ▪ Delayed write request discarded ▪ Delayed read request discarded ▪ Delayed transaction master timeout ▪ Errors reported from PCI Express port (advanced error reporting) in transparent mode. This signal is an open drain buffer that requires an external pull-up resistor for proper operation.
REQ_L [3:0]	33, 34, 32, 31	I	**Request (Active LOW):** REQ_L's are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ_Ls for at least 2 PCI clock cycles before asserting them again. If external arbiter is selected, REQ_L [0] will be the bus grant input to PI7C9X113SL. Also, REQ_L [3:1] will become the GPI [2:0]. When powered up, if both REQ_L[2] and REQ_L[3] and pulled low (Active LOW) and stay low in normal operation, the PI7C9X113SL will change the function of CLKOUT[3] to CLKRUN_L and CLKOUT[2] to CLKREQ_L, respectively.
GNT_L [3:0]	41, 39, 40, 37	O	**Grant (Active LOW):** PI7C9X113SL asserts GNT_Ls to release PCI bus control to bus master devices. During idle and all GNT_Ls are de-asserted and arbiter is parking to PI7C9X113SL, PI7C9X113SL will drive AD, CBE, and PAR to valid logic levels. If external arbiter is selected, GNT_L [0] will be the bus request from PI7C9X113SL to external arbiter. Also, GNT_L [3:1] will become the GPO [2:0].
CLKOUT [3:0]	49, 54, 56, 59	B	**PCI Clock Outputs:** PCI clock outputs are derived from the CLKIN and provide clocking signals to external PCI Devices. In external feedback mode, CLKOUT[0] becomes an input for feedback clock and CLKOUT[1:3] remain as clock outputs to provide clock signals to external PCI Devices. Please see Chapter 8 for further information.
M66EN	102	I	**66MHz Enable:** This input is used to specify if Bridge is capable of running at 66MHz. For 66MHz operation on the PCI bus, this signal should be pulled "HIGH". For 33MHz operation on the PCI bus, this signal should be pulled LOW.
RESET_L	46	O	**RESET_L (Active LOW):** When RESET_L active, all PCI signals should be asynchronously tri-stated.
INTA_L INTB_L INTC_L INTD_L	36, 43, 57, 60	I	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA_L, INTB_L, INTC_L, INTD_L signals are inputs and asynchronous to the clock in the forward mode.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
CLKIN	44	I	**PCI Clock Input:** PCI Clock Input Signal connects to an external clock source. The PCI Clock Outputs CLKOUT [3:0] pins are derived from CLKIN Input.

2.4 MODE SELECT AND STRAPPING SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TM0	128	ID	**Mode Select 0:** Mode Selection Pin to select EEPROM or SM Bus. TM0=0 for EEPROM (I2C) support and TM0=1 for SM Bus support. TM0 is a strapping pin. See Table 3-1 mode selection and Table 3-2 for strapping control.
TM1	23	ID	**Mode Select 1:** Mode Selection Pin for normal operation. Set TM1=0 for normal operation. TM1=1 is reserved. TM1 is a strapping pin. See Table 3-1 mode selection and Table 3-2 for strapping control.

2.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TCK	26	IU	**Test Clock:** TCK is the test clock to synchronize the state information and data on the PCI bus side of PI7C9X113SL during boundary scan operation.
TMS	24	IU	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller.
TDO	27	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain.
TDI	28	IU	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the PCI side of PI7C9X113SL.

2.6 MISCELLANEOUS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
GPIO [3:0]	47, 48, 51, 52	B	**General Purpose I/O Data Pins:** The 4 general-purpose signals are programmable as either input-only or bi-directional signals by writing the GPIO output enable control register in the configuration space.
SMBCLK / SCL	3	B	**SMBUS / EEPROM Clock Pin:** When EEPROM (I2C) interface is selected (TM0=0), this pin is an output of SCL clock and connected to EEPROM clock input. When SMBUS interface is selected (TM0=1), this pin is an input for the clock of SMBUS.
SMBDATA / SDA	5	B/IOD	**SMBUS / EEPROM Data Pin:** Data Interface Pin to EERPOM or SMBUS. When EEPROM (I2C) interface is selected (TM0=0), this pin is a bi-directional signal. When SMBUS interface is selected (TM0=1), this pin is an open drain signal.
PME_L	1	I	**Power Management Event Pin:** Power Management Event Signal is asserted to request a change in the device or link power state.
WAKE_L	4	O	**Wakeup Signal (Active LOW):** This signal is asserted when PME_L pin is asserted and the link is in the L2 state
REXTP, REXTN	8, 9	I	**External Precision Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to provide a reference to both the bias currents and impedance calibration circuitry.
NC	22	-	**Not Connected**

2.7 POWER AND GROUND PINS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDA	15, 18	P	**Analog Voltage Supply for PCI Express Interface:** Connect to the 1.1V Power Supply.
VDDA33	10		**High Voltage Supply for PCI Express Interface:** Connect to the 3.3V Power Supply.
VDDC	30, 35, 45, 53, 62, 73, 81, 95, 105, 114, 127	P	**Core Supply Voltage:** Connect to the 1.1V Power Supply.
VDDCAUX	7	P	**Auxiliary Core Supply Voltage:** Connect to the 1.0V Power Supply.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VD33	25, 38, 50, 55, 58, 66 72, 77, 82, 87, 91, 101, 107, 112, 118, 123	P	**I/O Supply Voltage for PCI Interface:** Connect to the 3.3V Power Supply for PCI I/O Buffers.
VAUX	2	P	**Auxiliary I/O Supply Voltage for PCI interface:** Connect to the 3.3V Power Supply.
VSS	6, 11, 14, 19, 42, 65, 84, 115	P	**Ground:** Connect to Ground.

2.8 PIN ASSIGNMENTS

Table 2-1 Pin Assignments

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	PME_L	33	REQ_L[3]	65	VSS	97	IRDY_L
2	VAUX	34	REQ_L[2]	66	VD33	98	DEVSEL_L
3	SMBCLK / SCL	35	VDDC	67	AD[1]	99	CBE[2]
4	WAKE_L	36	INTA_L	68	AD[3]	100	TRDY_L
5	SMBDAT / SDA	37	GNT_L[0]	69	AD[2]	101	VD33
6	VSS	38	VD33	70	AD[4]	102	M66EN
7	VDDCAUX	39	GNT_L[2]	71	AD[5]	103	AD[17]
8	REXTP	40	GNT_L[1]	72	VD33	104	AD[16]
9	REXTN	41	GNT_L[3]	73	VDDC	105	VDDC
10	VDDA33	42	VSS	74	AD[6]	106	AD[18]
11	VSS	43	INTB_L	75	AD[7]	107	VD33
12	REFCLKN	44	CLKIN	76	CBE[0]	108	AD[19]
13	REFCLKP	45	VDDC	77	VD33	109	AD[20]
14	VSS	46	RESET_L	78	AD[8]	110	AD[21]
15	VDDA	47	GPIO[3]	79	AD[9]	111	AD[22]
16	TN	48	GPIO[2]	80	AD[10]	112	VD33
17	TP	49	CLKOUT[3]	81	VDDC	113	AD[23]
18	VDDA	50	VD33	82	VD33	114	VDDC
19	VSS	51	GPIO[1]	83	AD[11]	115	VSS
20	RN	52	GPIO[0]	84	VSS	116	CBE[3]
21	RP	53	VDDC	85	AD[12]	117	AD[24]
22	NC	54	CLKOUT[2]	86	AD[13]	118	VD33
23	TM1	55	VD33	87	VD33	119	AD[25]
24	TMS	56	CLKOUT[1]	88	AD[14]	120	AD[26]
25	VD33	57	INTC_L	89	CBE[1]	121	AD[28]
26	TCK	58	VD33	90	AD[15]	122	AD[27]
27	TDO	59	CLKOUT[0]	91	VD33	123	VD33
28	TDI	60	INTD_L	92	PERR_L	124	AD[29]
29	PERST_L	61	SERR_L	93	LOCK_L	125	AD[31]
30	VDDC	62	VDDC	94	PAR	126	AD[30]
31	REQ_L[0]	63	FRAME_L	95	VDDC	127	VDDC
32	REQ_L[1]	64	AD[0]	96	STOP_L	128	TM0

3 MODE SELECTION AND PIN STRAPPING

3.1 FUNCTIONAL MODE SELECTION

PI7C9X113SL uses TM1 and TM0 pins to select different modes of operations. These input signals are required to be stable during normal operation. One of the four combinations of normal operation can be selected by setting the logic values for the three mode select pins. For example, if the logic values are low for both two (TM1 and TM0) pins, the normal operation will have EEPROM (I2C) support with internal arbiter. The designated operation with respect to the values of the TM1 and TM0 pins are defined on Table 3-1:

Table 3-1 Mode Selection

TM1 Strapped	TM0 Strapped	Functional Mode
0	0	EEPROM (I2C) support
0	1	SM Bus support

3.2 PIN STRAPPING

If TM1 is strapped to low, PI7C9X113SL uses REQ_L[3:2] as the strapping pins at the PCIe PERST_L de-assertion to enable Clock Power Management feature.

Table 3-2 Pin Strapping for Clock Power Management

TM1 Strapped	REQ_L[3:2] Strapped	Test Functions
0	2'b0	Clock Power Management is enabled, only two PCI devices supported. CLKOUT[2] is used as CLKREQ_L CLKOUT[3] is used as CLKRUN_L

4 TRANSPARENT AND FORWARD BRIDGING

4.1 TRANSPARENT MODE

In transparent bridge mode, base class code of PI7C9X113SL is set to be 06h (bridge device). The sub-class code is set to be 04h (PCI-to-PCI bridge). Programming interface is set to either 00h or 01h. If this interface is set to 00h, subtractive decoding is not supported. If it is set to 01h, legacy support is enabled and subtractive decoding is supported.

When Subtractive Decoding PCI-to-PCI bridge is enabled by setting the legacy bit (bit 0 of offset 98h), all cycles (Memory/IO) are forwarded to downstream PCI devices. However, the Type-1 configuration cycle still should be checked for the bus number in order to be forwarded to PCI bus. The PCI-X/PCIe capability is not included in the Capability List and all PCI-X/PCIe capability registers and Extended Configuration registers are treated as reserved registers. As a result, all Write accesses are completed normally but data is discarded, and all Read accesses are returned with data value of 0.

When PCI bus Subtractive Decoding Enable bit (bit 1 of 98h) is set, the device performs subtractive decode at PCI bus when the cycle is outside the range (negative decoding is used).

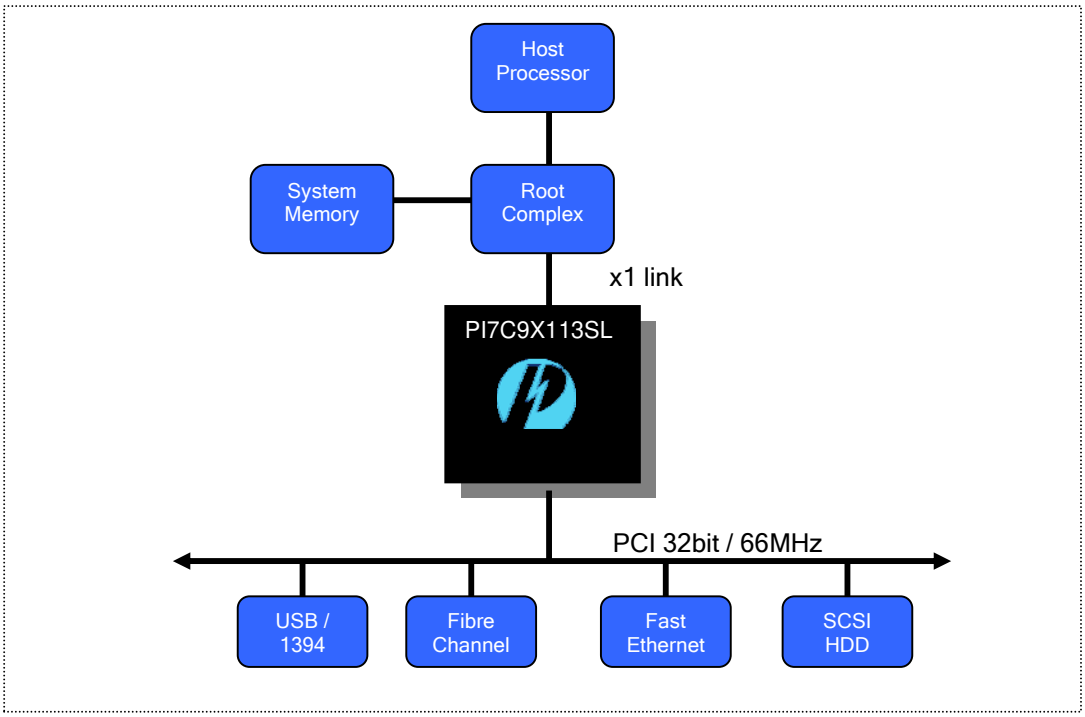
PI7C9X113SL has type-1 configuration header. These configuration registers are the same as traditional transparent PCI-to-PCI Bridge. In fact, it is backward compatible to the software that supporting traditional transparent PCI-to-PCI bridges. Configuration registers can be accessed from several different ways. For PCI Express access, PCI Express configuration transaction is in forward bridge mode. For I2C access, I2C bus protocol is used with EEPROM selected (TM0=0). For SM bus access, SM bus protocol is used with SM bus selected (TM0=1).

4.2 FORWARD BRDIGE

PI7C9X113SL supports forward mode of bridging. In forward bridging mode, its PCI Express interface is connected to a root complex and its PCI bus interface is connected to PCI devices.

PCI based systems and peripherals are ubiquitous in the I/O interconnect technology market today. It will be a tremendous effort to convert existing PCI based products to be used in PCI Express systems. PI7C9X113SL provides a solution to bridge existing PCI based products to the latest PCI Express technology.

Figure 4-1 Forward Bridge Mode



5 PCI EXPRESS FUNCTIONAL OVERVIEW

5.1 TLP STRUCTURE

PCI Express TLP (Transaction Layer Packet) Structure is comprised of format, type, traffic class, attributes, TLP digest, TLP poison, and length of data payload.

There are four TLP formats defined in PI7C9X113SL based on the states of FMT [1] and FMT [0] as shown on Table 5-1 .

Table 5-1 TLP Format

FMT [1]	FMT [0]	TLP Format
0	0	3 double word, without data
0	1	4 double word, without data
1	0	3 double word, with data
1	1	4 double word, with data

Data payload of PI7C9X113SL can range from 4 (1DW) to 512 (128DW) bytes. PI7C9X113SL supports three TLP routing mechanisms. They are comprised of Address, ID, and Implicit routings. Address routing is being used for Memory and IO requests. ID based (bus, device, function numbers) routing is being used for configuration requests. Implicit routing is being used for message routing. There are two message groups (baseline and advanced switching). The baseline message group contains INTx interrupt signaling, power management, error signaling, locked transaction support, slot power limit support, vendor defined messages, hot-plug signaling. The other is advanced switching support message group. The advanced switching support message contains data packet and signal packet messages. Advanced switching is beyond the scope of PI7C9X113SL implementation.

The r [2:0] values of the "type" field will determine the destination of the message to be routed. All baseline messages must use the default traffic class zero (TC0).

5.2 VIRTUAL ISOCHRONOUS OPERATION

This section provides a summary of Virtual Isochronous Operation supported by PI7C9X113SL. Virtual Isochronous support is disabled by default. Virtual Isochronous feature can be turned on with setting bit [26] of offset 40h to one. Control bits are designated for selecting which traffic class (TC1-7) to be used for upstream (PCI -to-PCI Express). PI7C9X113SL accepts only TC0 packets of configuration, IO, and message packets for downstream (PCI Express-to-PCI). If configuration, IO and message packets have traffic class other than TC0, PI7C9X113SL will treat them as malformed packets. PI7C9X113SL maps all downstream memory packets from PCI Express to PCI transactions regardless the virtual Isochronous operation is enabled or not.

6 CONFIGURATION REGISTER ACCESS

PI7C9X113SL supports Type-0 and Type-1 configuration space headers and Capability ID of 01h (PCI power management) to 10h (PCI Express capability structure).

PI7C9X113SL supports PCI Express capabilities register structure with capability version set to 1h (bit [3:0] of offset 02h).

6.1 CONFIGURATION REGISTER MAP

PI7C9X113SL supports capability pointer with PCI power management (ID=01h), PCI bridge sub-system vendor ID (ID=0Dh), PCI Express (ID=10h), and message signaled interrupt (ID=05h).

Table 6-1 Configuration Register Map (00h – FFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
01h - 00h	Vendor ID	Yes1	Yes2
03h – 02h	Device ID	Yes1	Yes2
05h – 04h	Command Register	Yes	Yes
07h – 06h	Primary Status Register	Yes	Yes
0Bh – 08h	Class Code and Revision ID	Yes1	Yes2
0Ch	Cacheline Size Register	Yes	Yes
0Dh	Primary Latency Timer	Yes	Yes
0Eh	Header Type Register	Yes	Yes
0Fh	Reserved	-	-
17h – 10h	Reserved	-	-
18h	Primary Bus Number Register	Yes	Yes
19h	Secondary Bus Number Register	Yes	Yes
1Ah	Subordinate Bus Number Register	Yes	Yes
1Bh	Secondary Latency Timer	Yes	Yes
1Ch	I/O Base Register	Yes	Yes
1Dh	I/O Limit Register	Yes	Yes
1Fh – 1Eh	Secondary Status Register	Yes	Yes
21h – 20h	Memory Base Register	Yes	Yes
23h – 22h	Memory Limit Register	Yes	Yes
25h – 24h	Prefetchable Memory Base Register	Yes	Yes
27h – 26h	Prefetchable Memory Limit Register	Yes	Yes
2Bh – 28h	Prefetchable Memory Base Upper 32-bit Register	Yes	Yes
2Dh – 2Ch	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
2Fh – 2Eh	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
31h – 30h	I/O Base Upper 16-bit Register	Yes	Yes
33h – 32h	I/O Limit Upper 16-bit Register	Yes	Yes
34h	Capability Pointer	Yes	Yes
37h – 35h	Reserved	No	Yes
3Bh – 38h	Reserved	No	Yes
3Ch	Interrupt Line	Yes	Yes
3Dh	Interrupt Pin	Yes	Yes
3Fh – 3Eh	Bridge Control	Yes	Yes
41h – 40h	PCI Data Prefetching Control	Yes	Yes
43h – 42h	Chip Control 0	Yes	Yes
47h – 44h	Reserved	-	-
4Bh – 48h	Arbiter Mode, Enable, Priority	-	-
4Fh – 4Ch	Reserved	-	-
53h – 50h	Memory Readsmart Base Lower 32-Bit Register 1	Yes	Yes
57h – 54h	Memory Readsmart Base Upper 32-Bit Register 1	Yes	Yes
5Bh – 58h	Memory Readsmart Range Control Register 1	Yes	Yes
5Fh – 5Ch	Memory Readsmart Memory Base Lower 32-Bit Register 2	Yes	Yes
63h – 60h	Memory Readsmart Base Upper 32-Bit Register 2	Yes	Yes
67h – 64h	Memory Readsmart Range Size Register 2	Yes	Yes
6Ah – 68h	Reserved	Yes	Yes
6Bh	Upstream Memory Read/Write Control	Yes	Yes
6Fh – 6Ch	PHY TX/RX Control	Yes	Yes
73h – 70h	EEPROM (I2C) Control and Status Register	No	Yes
77h – 74h	Reserved	-	-
7Bh – 78h	GPIO Data and Control	Yes	Yes
7Ch – 7Ch	Reserved	-	-
83h – 80h	PCI-X Capability	Yes	Yes
87h – 84h	PCI-X Bridge Status	Yes	Yes
8Bh – 88h	Upstream Split Transaction	Yes	Yes
8Fh – 8Ch	Downstream Split Transaction	Yes	Yes
93h – 90h	Power Management Capability	Yes	Yes
97h – 94h	Power Management Control and Status	Yes	Yes

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
98h	Subtractive Decoding PCI-to-PCI Bridge Enable	Yes	Yes
9Bh – 99h	Reserved	-	-
9Fh – 9Ch	Reserved	-	-
A3h – A0h	Slot ID Capability	Yes	Yes
A5h – A4h	Secondary Clock and CLKRUN Control	Yes	Yes
A6h	XPIP Configuration Register 3		
A7h	Reserved	Yes	Yes
A9h – A8h	Subsystem ID and Subsystem Vendor ID Capability	Yes	Yes
ABh – AAh	Reserved		
AFh – ACh	Subsystem ID and Subsystem Vendor ID	Yes	Yes
B3h – B0h	PCI Express Capability	Yes	Yes
B7h – B4h	Device Capability	Yes	Yes
BBh – B8h	Device Control and Status	Yes	Yes
BFh – BCh	Link Capability	Yes	Yes
C3h – C0h	Link Control and Status	Yes	Yes
CBh – C4h	Reserved	-	-
CFh – CCh	XPIP Configuration Register 0	Yes	Yes
D3h – D0h	XPIP Configuration Register 1	Yes	Yes
D6h – D4h	XPIP Configuration Register 2	Yes	Yes
D7h	Reserved	-	-
DBh – D8h	VPD Capability Register	Yes	Yes
DFh – DCh	VPD Data Register	Yes3	Yes
E3h – E0h	Extended Config Access Address	Yes	Yes
E7h – E4h	Extended Config Access Data	Yes	Yes
EBh – E8h	Reserved	-	-
EFh – ECh	Reserved	-	-
F3h – F0h	MSI Capability Register	Yes	Yes
F7h – F4h	Message Address	Yes	Yes
FBh – F8h	Message Upper Address	Yes	Yes
FFh – FCh	Message Data	Yes	Yes

Note 1: When masquerade is enabled, it is pre-loadable.
Note 2: Read access only.
Note 3: The VPD data is read/write through I2C during VPD operation.

6.2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP

PI7C9X113SL also supports PCI Express Extended Capabilities with from 257-byte to 4096-byte space. The offset range is from 100h to FFFh. The offset 100h is defined for Advance Error Reporting (ID=0001h). The offset 150h is defined for Virtual Channel (ID=0002h).

When Subtractive Decoding PCI-to-PCI bridge is enabled, the PCI-X/PCIe capability is not included in the Capability List and all PCI-X/PCIe capability registers and Extended Configuration registers are treated as reserved registers.

Table 6-2 PCI Express Extended Capability Register Map (100h – FFFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	Transparent Mode (type1)	EEPROM (I2C) Access	SM Bus Access
103h – 100h	Advanced Error Reporting (AER) Capability	Yes	Yes2
107h – 104h	Uncorrectable Error Status	No	Yes
10Bh – 108h	Uncorrectable Error Mask	Yes	Yes
10Fh – 10Ch	Uncorrectable Severity	No	Yes
113h – 110h	Correctable Error Status	No	Yes
117h – 114h	Correctable Error Mask	No	Yes
11Bh – 118h	AER Capabilities and Control	No	Yes
12Bh – 11Ch	Header Log Registers	No	Yes
12Fh – 12Ch	Secondary Uncorrectable Error Status	No	Yes
133h – 130h	Secondary Uncorrectable Error Mask	No	Yes
137h – 134h	Secondary Uncorrectable Severity	No	Yes
13Bh – 138h	Secondary AER Capability and Control	No	Yes
14Bh – 13Ch	Secondary Header Log Register	No	Yes
14Fh – 14Ch	Reserved	No	Yes
153h – 150h	VC Capability	No	Yes
157h – 154h	Port VC Capability 1	No	Yes
15Bh – 158h	Port VC Capability 2	No	Yes
15Fh – 15Ch	Port VC Status and Control	No	Yes
163h – 160h	VC0 Resource Capability	No	Yes
167h – 164h	VC0 Resource Control	No	Yes
16Bh – 168h	VC0 Resource Status	No	Yes
2FFh – 16Ch	Reserved	No	No
303h – 300h	Extended GPIO Data and Control	No	Yes
307h – 304h	Extended GPI/GPO Data and Control	No	Yes
30Fh – 308h	Reserved	No	No
310h	Replay and Acknowledge Latency Timer	Yes	Yes
FFFh – 314h	Reserved	No	No

Note 5: Read access only.