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PI7C9X130

PCI Express to PCI-X Reversible Bridge

DATASHEET

Revision 5
July 2018

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REVISION HISTORY

Date	Revision Number	Description
02/24/2006	0.1	First Draft of PI7C9X130 Data Sheet
03/20/2006	0.2	Correct INTA, B, C, D buffer type Update configuration map and registers Update JTAG chain order Add PCI/PCI-X selection information
04/07/2006	0.3	Update on configuration register bit definitions. 1) Bit [10, 7:2] of offset 40h 2) Bit [31:30] of offset 68h 3) Bit [0] of offset 70h 4) Bit [23:22] of offset 94h 5) Bit [7:1] of offset 164h Correct typo of pin CLKRUN_L in pin assignment and JTAG section.
06/07/2006	0.4	Add Absolute Maximum Ratings Correct pin description: 1. REQ_L as GPI and GNT_L as GPO 2. CLKOUT [8:0] as CLKOUT [6:0]
06/19/2006	0.5	Correct default setting for bit [31:30] of offset 68h
03/26/2007	0.6	
04/18/2007	0.7	Completed non-transparent function for address 28h – 2Bh in the Configuration Register Map – section 7.1 Corrected pin HSEN (R3) in section 2.6 – Miscellaneous Signals. Should read tie LOW if Hot Swap is not used instead of tie HIGH
05/02/2007	0.8	Revised table 8-1 in section 8 Address bit[5] corrected to equal 0 Address bit[4] corrected to equal GPIO[3]
05/15/2007	0.9	Revised PCIe Base Specification Compliancy from 1.0a to 1.1
06/08/2007	0.91	Corrected pin HSSW (T3) in section 2.6 – Miscellaneous Signals. Remove "Tied high if hot swap function is not used."
07/13/2007	1.0	Corrected bit[13] offset 110h from reserved to "Advisory Non-Fatal Error Status" Changed Logos and some font types
08/07/2007	1.1	Corrected Pin #'s of GNT_L[1], GNT_L[2], GNT_[3], GNT_[4], GNT_[5] on Table 14-1JTAG Boundary Scan Register Definition
09/28//2007	1.2	Recommendation of Pull-up Resistor for PI7C9X130 Control Signals added to section 16.3 of PI7C9X130 Datasheets; pin numbers of SMBCLK and SMBDAT are corrected under section 5.2. Added PCIX Clock Detection to Chapter 9, Clock Scheme.
01/03/2008	1.3	Revised Ambient Temperature Maximum Ratings Compliancy
04/21/2008	1.4	Updated to revision D
04/24/2008	1.5	Added package thermal data. RREF pin description change. Removed CDM information
08/08/2008	1.6	Added Power-Up Sequencing Description
10/30/2008	1.7	Revised Product Ordering Info
07/01/2009	1.8	Added Extended Configuration Access / Data Register under section 7.1 and 7.4
01/20/2010	1.9	Added Asynchronous Clock Support to Section 19
03/29/2010	2.0	Revised configuration register definitions: 1) 7.4.31 bit[5:4] and bit[7:6] of PCI Data Buffering Control Register)Offset 40h) 2) 7.4.87 Extended Configuration Access Address Register (Offset E0h) 3) 7.4.88 Extended Configuration Access Data Register (Offset E4h) 4) 7.4.129 bit[30] of Replay and Acknowledge Latency Timers (Offset 310h) 5) 7.5.24 bit[5:4] and bit[7:6] of PCI Data Buffering Control Register)Offset 40h) 6) 7.5.135 bit[30] of Replay and Acknowledge Latency Timers (Offset 310h) Revised Section 9 Clock Scheme
04/27/2011	2.1	Updated Section 2.2 PCI Express Signals
06/29/2011	2.2	Updated Section 2.3 PCI Signals (REQ_L [3:0], GNT_L [3:0]) Updated Section 7.5.9, 7.5.11, 7.5.12, 7.5.13, 7.5.34, 7.5.36, 7.5.37, 7.5.38 (bit[31:12]).
09/17/2012	2.3	Updated Section 7.4.70 Device Capability Register (bit[2:0]) Updated Section 7.5.76 Device Capability Register (bit[2:0])
04/15/2015	2.4	Updated Section 7.4 PCI Configuration Registers For Transparent Bridge Mode Updated Section 7.5 PCI Configuration Registers For Non-Transparent Bridge Mode
04/20/2016	2.5	Updated Section 7.4 PCI Configuration Registers For Transparent Bridge Mode Updated Section 7.5 PCI Configuration Registers For Non-Transparent Bridge Mode Updated Section 2.5 JTAG Boundary Scan Signals

06/02/2017	2.6	Updated Section 16.1 Absolute Maximum Ratings Updated Section 16.2 DC SPECIFICATIONS Added Table 16-4 PCIe Reference Clock Timing Parameters Added Table 16-5 PCI Express Interface - Differential Transmitter (TX) Output Characteristics Added Table 16-6 PCI Express Interface - Differential Receiver (RX) Input Characteristics Added Section 16.5 Operating Ambient Temperature
09/27/2017	3	Added Section 16 Power Sequencing Updated Section 19 Ordering Information Revision numbering system changed to whole number
03/16/2018	4	Updated Section 19 Ordering Information Added Figure 18-4 PART MARKING
07/30/2018	5	Updated Section 1.3 General Features Updated Section 2.6 Miscellaneous Signals Updated Section 19 Ordering Information

PREFACE

The datasheet of PI7C9X130 will be enhanced periodically when updated information is available. The technical information in this datasheet is subject to change without notice. This document describes the functionalities of PI7C9X130 (PCI Express Bridge) and provides technical information for designers to design their hardware using PI7C9X130.

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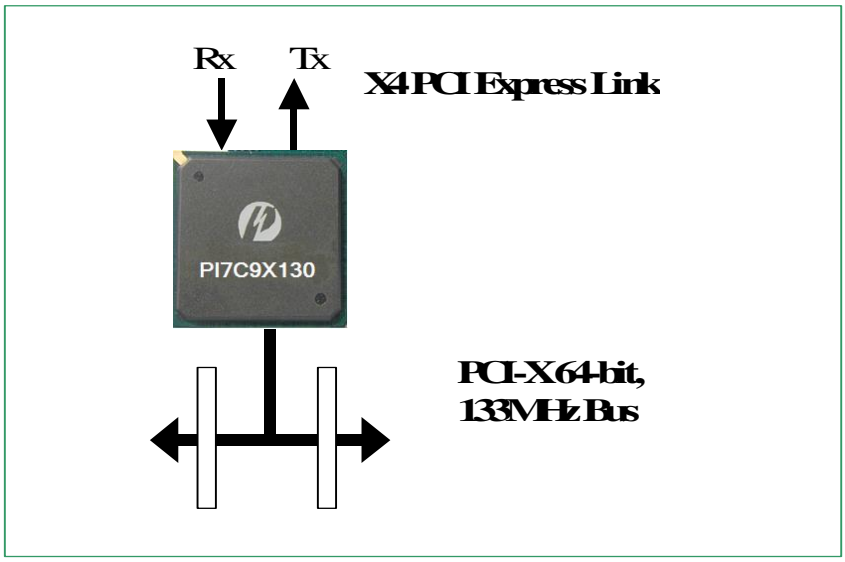
1 INTRODUCTION

PI7C9X130 is a PCIe-to-PCI/PCI-X bridge. PI7C9X130 is compliant with the *PCI Express Base Specification,* Revision 1.1, the *PCI Express Card Electromechnical Specification*, Revision 1.1, the *PCI Local Bus Specification,* Revision 3.0 and *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. PI7C9X130 supports transparent and non-transparent mode of operations. Also, PI7C9X130 supports forward and reverse bridging. In forward bridge mode, PI7C9X130 has an x4 PCI Express upstream port and a 64-bit PCI/PCI-X downstream port. The 64-bit PCI-X downstream port is 133MHz capable (see). In reverse bridge mode, PI7C9X130 has a 64-bit PCI-X upstream port and an x4 PCI Express downstream port. PI7C9X130 configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software and firmware is needed for the original operation.

Figure 1-1 PI7C9X130 Topology



1.1 PCI EXPRESS FEATURES

- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express Card Electromechnical Specification, Revision 1.1
- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Physical Layer interface (x4 link with 2.5Gb/s data rate)
- Lane polarity toggle
- Virtual isochronous support (upstream TC1-7 generation, downstream TC1-7 mapping)
- ASPM support
- Beacon support
- CRC (16-bit), LCRC (32-bit)
- ECRC and advanced error reporting
- PRBS (Pseudo Random Bit Sequencing) generator/checker for chip testing
- Maximum payload size to 512 bytes

1.2 PCI/PCI-X FEATURES

- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Bus PM Interface Specification, Revision 1.1
- Compliant with PCI Hot-Plug Specification, Revision 1.1
- Compliant with PCI Mobile Design Guide, Version 1.1
- Compliant with PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a
- PME support
- 3.3V PCI signaling with 5V I/O tolerance
- Provides two level arbitration support for six PCI Bus masters
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support

1.3 GENERAL FEATURES

- Compliant with Advanced Configuration and Power Interface Specification (ACPI), Revision 2.0b
- Compliant with System Management (SM) Bus, Version 2.0
- Forward bridging (PCI Express as primary bus, PCI as secondary bus)
- Reverse bridging (PCI as primary bus, PCI Express as secondary bus)
- Transparent mode support
- Non-transparent mode Support
- GPIO support (4 bi-directional pins)
- Power Management (including ACPI, CLKRUN_L, PCI_PM)
- Masquerade Mode (pre-loadable vendor, device, and revision IDs)
- EEPROM (I2C) Interface
- Industril Temp Compliant (-40˚C ~ +85˚C)
- SM Bus Interface
- Auxiliary powers (VAUX, VDDAUX, VDDCAUX) support
- Power consumption at about 1.5 Watt in typical condition
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

2 PIN DEFINITION

2.1 SIGNAL TYPES

TYPE OF SIGNAL	DESCRIPTION
B	Bi-directional
I	Input
IU	Input with pull-up
ID	Input with pull-down
IOD	Bi-directional with open drain output
OD	Open drain output
O	Output
P	Power
G	Ground

"_L" in signal name indicates Active LOW signal

2.2 PCI EXPRESS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
REFCLKP REFCLKN	D2, D1	I	**Reference Clock Input s:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors.
RAP RAN	F2, F1	I	**PCI Express data input s:** Differential data receiver input signals for lane A
RBP RBN	H2, H1	I	**PCI Express data input s:** Differential data receiver input signals for lane B
RCP RCN	K2, K1	I	**PCI Express data input s:** Differential data receiver input signals for lane C
RDP RDN	M2, M1	I	**PCI Express data input s:** Differential data receiver input signals for lane D
TAP TAN	E4, E3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane A
TBP TBN	G4, G3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane B
TCP TCN	J4, J3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane C
TDP TDN	L4, L3	O	**PCI Express data outputs:** Differential data transmitter output signals for lane D
RREF	H4	I	**Resistor Reference:** It is used to connect an external resistor (2.1K Ohm +/- 1%) to VSS to provide a reference current for the driver and equalization circuit.
PERST_L	P1	B	**PCI Express Fundamental Reset:** PI7C9X130 uses this reset to initialize the internal state machines.

2.3 PCI SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
AD [31:0]	D5, A6, B6, C6, D6, A7, B7, C7, A8, B8, C8, D8, A9, B9, C9, D9, G16, G15, G14, G13, H16, H15, H14, H13, J15, J14, J13, K16, K15, K14, K13, L16	B	**Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of FBCLKIN when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X130 drives AD [31:0] to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
AD [63:32]	N11, P11, R11, T11, N12, P12, R12, T12, R13, T13, P14, R14, T14, T15, R15, R16, D16, C15, C16, B16, B15, A15, C14, B14, C13, B13, A13, D12, C12, B12, A12, D11	B	**Upper 32-bit Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of FBCLKIN when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X130 drives AD [63:32] to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
CBE [3:0]	D7, A10, F13, J16	B	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X130 drives CBE [3:0] signals to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
CBE [7:4]	P13, P15, A14, C11	B	**Upper 4-bit Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X130 drives CBE [7:4] signals to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
PAR	F14	B	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [31:0], CBE [3:0]. If PI7C9X130 is an initiator with a write transaction, PI7C9X130 will tri-state PAR. If PI7C9X130 is a target and a write transaction, PI7C9X130 will drive PAR one clock after the address or data phase. If PI7C9X130 is a target and a read transaction, PI7C9X130 will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X130 drives PAR to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
PAR64	D15	B	**Parity Bit for Upper 32-bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [63:32], CBE [7:4]. If PI7C9X130 is an initiator with a write transaction, PI7C9X130 will tri-state PAR64. If PI7C9X130 is a target and a write transaction, PI7C9X130 will drive PAR64 one clock after the address or data phase. If PI7C9X130 is a target and a read transaction, PI7C9X130 will drive PAR64 one clock after the address phase and tri-state PAR64 during data phases. PAR64 is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X130 drives PAR64 to a valid logic level when arbiter is parking to PI7C9X130 on PCI bus.
FRAME_L	B10	B	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME_L indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
IRDY_L	C10	B	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
TRDY_L	D10	B	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
DEVSEL_L	A11	B	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, PI7C9X130 waits for the assertion of this signal within 5 cycles of FRAME_L assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.
STOP_L	B11	B	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a de-asserted state for one cycle.
LOCK_L	E13	B	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. PI7C9X130 does not support any upstream LOCK transaction.
IDSEL	M13	I	**Initialization Device Select:** Used as a chip select line for Type 0 configuration access to bridge's configuration space.
PERR_L	F16	B	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
SERR_L	F15	IOD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error condition. If SERR control is enabled, PI7C9X130 will drive this pin on: ▪ Address parity error ▪ Posted write data parity error on target bus ▪ Master abort during posted write transaction ▪ Target abort during posted write transaction ▪ Posted write transaction discarded ▪ Delayed write request discarded ▪ Delayed read request discarded ▪ Delayed transaction master timeout ▪ Errors reported from PCI Express port (advanced error reporting) in transparent mode. This signal is an open drain buffer that requires an external pull-up resistor for proper operation.
REQ_L [5:0]	P3, N3, T2, R2, P2, R1	I	**Request (Active LOW):** REQ_Ls are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ_Ls for at least 2 PCI clock cycles before asserting them again. If the device is in reverse mode or if external arbiter is selected (CFN_L=1), REQ_L [0] will be the bus grant input to PI7C9X130. Also, REQ_L [5:2] will become the GPI [3:0].
GNT_L [5:0]	T5, R5, P5, N5, T4, R4	O	**Grant (Active LOW):** PI7C9X130 asserts GNT_Ls to release PCI bus control to bus master devices. During idle and all GNT_Ls are de-asserted and arbiter is parking to PI7C9X130, PI7C9X130 will drive AD, CBE, and PAR to valid logic levels. If the device is in reverse mode or if external arbiter is selected (CFN_L=1), GNT_L [0] will be the bus request from PI7C9X130 to external arbiter. Also, GNT_L [5:2] will become the GPO [3:0].
REQ64_L	D14	B	**Request for 64-bit transfer (Active LOW):** PI7C9X130 asserts REQ64_L to request for 64-bit transactions on the PCI bus when PI7C9X130 is the bus master. REQ64_L is an input when PI7C9X130 is a target device.
ACK64_L	E16	B	**Acknowledge for 64-bit transfer (Active LOW):** When PI7C9X130 is a target device and drives ACK64_L to signal the bus master to use 64-bit transfer. When PI7C9X130 is the bus master, ACK64_L is an input.
CLKOUT [6:0]	N10, T9, R9, P9, N9, T8, R8	O	**PCI Clock Outputs:** PCI clock outputs are derived from the CLKIN and provide clocking signals to external PCI Devices.
RESET_L	N7	B	**RESET_L (Active LOW):** When RESET_L active, all PCI signals should be asynchronously tri-stated.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
INTA_L INTB_L INTC_L INTD_L	P4 R6 T10 N15	IOD	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA_L, INTB_L, INTC_L, INTD_L signals are inputs and asynchronous to the clock in the forward mode. In reverse mode, INTA_L, INTB_L, INTC_L, and INTD_L are open drain buffers for sending interrupts to the host interrupt controller.
FBCLKIN	B4	I	**Feedback Clock Input:** It connects to one of the CLKOUT [6:0] Output Signals and provides internal clocking to PI7C9X130 PCI bus interface.
CLKIN / M66EN	T6	I	**PCI Clock Input:** PCI Clock Input Signal connects to an external clock source. The PCI Clock Outputs CLKOUT [6:0] pins are derived from CLKIN Input. **M66EN Input:** It is driven high or low to enable the internal clock generator to provide clock outputs to CLKOUT[6:0] pins.

2.4 MODE SELECT AND STRAPPING SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TM2	P16	I	**Mode Select 2:** TM2 is a strapping pin. When TM2 is strapped low for normal operations and strapped high for testing functions. See table 3-1 for mode selection and 3-2 for strapping control for details.
TM1	A3	I	**Mode Select 1:** Mode Selection Pin to select EEPROM or SM Bus. TM1=0 for EEPROM (I2C) support and TM1=1 for SM Bus support. TM1 is also a strapping pin. See table 3-1 mode selection and 3-2 for strapping control.
TM0	A2	I	**Mode Select 0:** Mode Selection Pin to select transparent or non-transparent mode. TM0=0 for transparent bridge function mode and TM0=1 for non-transparent bridge function mode. TM0 is also a strapping pin. See table 3-1 for mode selection and 3-2 for strapping control.
MSK_IN	N16	I	**Mask Input for CLKOUT:** When it is strapped to high, hot-plug is enabled. See table 3-2 for strapping control.
REVRSB	N14	I	**Forward or Reverse Bridging Pin:** REVRSB pin controls the Forward (REVRSB=0) or Reverse (REVRSB=1) Bridge Mode of PI7C9X130. This pin is also a strapping pin. See table 3-1 for mode selection.
CFN_L	P7	ID	**Bus Central Function Control Pin (Active Low):** To enable the internal arbiter, CFN_L pin should be tied low. When it's tied high, an external arbiter is required to arbitrate the bus. In external arbiter mode, REQ_L [0] is re-configured to be the secondary bus grant input, and GNT_L [0] is reconfigured to be the secondary bus request output. Also, REQ_L [5:2] and GNT_L [5:2] become GPI [3:0] and GPO [3:0] respectively if external arbiter is selected. CFN_L has a weak internal pull-down resistor. See table 3-1 for mode selection.

2.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TCK	L13	IU	**Test Clock:** TCK is the test clock to synchronize the state information and data on the PCI bus side of PI7C9X130 during boundary scan operation. At normal operation mode, this pin should be left open (NC).
TMS	M16	IU	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.
TDO	M14	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. At normal operation mode, this pin should be left open (NC).

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TDI	M15	IU	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the PCI side of PI7C9X130. At normal operation mode, this pin should be left open (NC).
TRST_L	L14	IU	**Test Reset (Active LOW):** TRST_L is the test reset to initialize the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.

2.6 MISCELLANEOUS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
GPIO [6:0]	L15, R10, P10, R7, T7, N8, P8	B	**General Purpose I/O Data Pins:** The 7 general-purpose signals are programmable as either input-only or bi-directional signals by writing the GPIO output enable control register in the configuration space. See chapter 8 for more information.
SMBCLK / SCL	B5	B	**SMBUS / EEPROM Clock Pin:** When EEPROM (I2C) interface is selected (TM1=0), this pin is an output of SCL clock and connected to EEPROM clock input. When SMBUS interface is selected (TM1=1), this pin is an input for the clock of SMBUS.
SMBDAT / SDA	A5	B/IOD	**SMBUS / EEPROM Data Pin:** Data Interface Pin to EERPOM or SMBUS. When EEPROM (I2C) interface is selected (TM1=0), this pin is a bi-directional signal. When SMBUS interface is selected (TM1=1), this pin is an open drain signal.
PME_L	C5	B	**Power Management Event Pin:** Power Management Event Signal is asserted to request a change in the device or link power state.
CLKRUN_L	C4	B	**Clock Run Pin (Active LOW):** The Clock Run signal, for mobile environment, is asserted and de-asserted to indicate the status of the PCI Clock.
PCIXCAP	A4	I	**PCI-X Capability Pin:** PI7C9X130 can be forced to PCI mode if PCIXCAP is tied to ground with a capacitor (0.01uF) in parallel. If PCIXCAP is connected to ground through a capacitor (0.01uF), PI7C9X130 will be in 133MHz PCI-X mode. If PCIXCAP is connected to ground through a resistor (10K Ohm) with a capacitor (0.01uF) in parallel, PI7C9X130 will be in 66MHz PCI-X mode.
PCIXUP	B3	O	**PCIXCAP Pull-up driver:** PI7C9X130 drives this pin for PCI-X mode detection.
DEV64	E15	I	**Control 64-bit bus width:** PI7C9X130 operates with 64-bit bus when DEV64=1. When DEV64=0, PI7C9X130 operates with 32-bit bus.
SEL100	E14	I	**Select 100MHz frequency:** When SEL100=1, PI7C9X130 expects to run at 100MHz clock. When SEL100=0, PI7C9X130 expects to run at 133MHz..
HSEN	R3	I	**Hot Swap Enable:** PI7C9X130 supports hot swap when HSEN is set to high. Tie LOW if hot swap function is not used.
HSSW	T3	I	**Hot Swap Switch:** PI7C9X130 detects HSSW input to monitor the insertion or impending extraction of a board.
LOO	N6	O	**LED On/Off:** PI7C9X130 drives LOO for LED illumination that signals the operator to extract the board.
ENUM_L	P6	OD	**ENUM_L signal:** PI7C9X130 drives ENUM_L to notify the system host that either a board has been freshly inserted or is about to be extracted.

2.7 POWER AND GROUND PINS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDA	E2, J1, J2, H3	P	**Analog Voltage Supply for PCI Express Interface:** Connect to the 1.8V Power Supply.
VDDP	G2, F3, J5, M3, N2	P	**Digital Voltage Supply for PCI Express Interface:** Connect to the 1.8V Power Supply.

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDAUX	F4, L1	P	**Auxiliary Voltage Supply for PCI Express Interface:** Connect to the 1.8V Power Supply.
VTT	G1, L5	P	**Termination Supply Voltage for PCI Express Interface:** Connect to the 1.8V Power Supply.
VDDA_PLL	D3	P	**Analog Voltage Supply for PLL at PCI Interface:** Connect to the 1.8V Power Supply.
VDDP_PLL	C2	P	**Digital Voltage Supply for PLL at PCI Interface:** Connect to the 1.8V Power Supply.
VDDC	M5, M6, M11, M12, J11, H11, E11, E10, K5, A1	P	**Core Supply Voltage:** Connect to the 1.8V Power Supply.
VDDCAUX	H5	P	**Auxiliary Core Supply Voltage:** Connect to the 1.8V Power Supply.
VD33	T1, N4, M7, M8, M9, L10, L11, M10, T16, N13, L12, K12, K11, J12, H12, G11, G12, F12, A16, D13, E12, F11, E9, E8, E7, E6, E5	P	**I/O Supply Voltage for PCI Interface:** Connect to the 3.3V Power Supply for PCI I/O Buffers.
VAUX	B2	P	**Auxiliary I/O Supply Voltage for PCI interface:** Connect to the 3.3V Power Supply.
VSS	B1, C1, C3, D4, F5, E1, G5, K3, K4, L2, N1, M4, L6, K6, L7, K7, L8, L9, K8, K9, K10, J6, J7, J8, J9, J10, H8, H9, H10, G10, F10, F9, F8, F7, F6, G9, G8, G7, G6, H7, H6	P	**Ground:** Connect to Ground.

2.8 PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VDDC	E1	VSS	J1	VDDA	N1	VSS
A2	TM0	E2	VDDA	J2	VDDA	N2	VDDP
A3	TM1	E3	TAN	J3	TCN	N3	REQ_L[4] / GPI[2]
A4	PCIXCAP	E4	TAP	J4	TCP	N4	VD33
A5	SMBDAT / SDA	E5	VD33	J5	VDDP	N5	GNT_L[2] / GPO[0]
A6	AD[30]	E6	VD33	J6	VSS	N6	LOO
A7	AD[26]	E7	VD33	J7	VSS	N7	RESET_L
A8	AD[23]	E8	VD33	J8	VSS	N8	GPIO[1]
A9	AD[19]	E9	VD33	J9	VSS	N9	CLKOUT[2]
A10	CBE[2]	E10	VDDC	J10	VSS	N10	CLKOUT[6]
A11	DEVSEL_L	E11	VDDC	J11	VDDC	N11	AD[63]
A12	AD[33]	E12	VD33	J12	VD33	N12	AD[59]
A13	AD[37]	E13	LOCK_L	J13	AD[5]	N13	VD33
A14	CBE[5]	E14	SEL100	J14	AD[6]	N14	REVRSB
A15	AD[42]	E15	DEV64	J15	AD[7]	N15	INTD_L
A16	VD33	E16	ACK64_L	J16	CBE[0]	N16	MSK_IN
B1	VSS	F1	RAN	K1	RCN	P1	PERST_L
B2	VAUX	F2	RAP	K2	RCP	P2	REQ_L[1]
B3	PCIXUP	F3	VDDP	K3	VSS	P3	REQ_L[5] / GPI[3]
B4	FBCLKIN	F4	VDDAUX	K4	VSS	P4	INTA_L
B5	SMBCLK / SCL	F5	VSS	K5	VDDC	P5	GNT_L[3] / GPO[1]
B6	AD[29]	F6	VSS	K6	VSS	P6	ENUM_L

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B7	AD[25]	F7	VSS	K7	VSS	P7	CFN_L
B8	AD[22]	F8	VSS	K8	VSS	P8	GPIO[0]
B9	AD[18]	F9	VSS	K9	VSS	P9	CLKOUT[3]
B10	FRAME_L	F10	VSS	K10	VSS	P10	GPIO[4]
B11	STOP_L	F11	VD33	K11	VD33	P11	AD[62]
B12	AD[34]	F12	VD33	K12	VD33	P12	AD[58]
B13	AD[38]	F13	CBE[1]	K13	AD[1]	P13	CBE[7]
B14	AD[40]	F14	PAR	K14	AD[2]	P14	AD[53]
B15	AD[43]	F15	SERR_L	K15	AD[3]	P15	CBE[6]
B16	AD[44]	F16	PERR_L	K16	AD[4]	P16	TM2
C1	VSS	G1	VTT	L1	VDDAUX	R1	REQ_L[0]
C2	VDDP_PLL	G2	VDDP	L2	VSS	R2	REQ_L[2] / GPI[0]
C3	VSS	G3	TBN	L3	TDN	R3	HSEN
C4	CLKRUN_L	G4	TBP	L4	TDP	R4	GNT_L[0]
C5	PME_L	G5	VSS	L5	VTT	R5	GNT_L[4] / GPO[2]
C6	AD[28]	G6	VSS	L6	VSS	R6	INTB_L
C7	AD[24]	G7	VSS	L7	VSS	R7	GPIO[3]
C8	AD[21]	G8	VSS	L8	VSS	R8	CLKOUT[0]
C9	AD[17]	G9	VSS	L9	VSS	R9	CLKOUT[4]
C10	IRDY_L	G10	VSS	L10	VD33	R10	GPIO[5]
C11	CBE[4]	G11	VD33	L11	VD33	R11	AD[61]
C12	AD[35]	G12	VD33	L12	VD33	R12	AD[57]
C13	AD[39]	G13	AD[12]	L13	TCK	R13	AD[55]
C14	AD[41]	G14	AD[13]	L14	TRST_L	R14	AD[52]
C15	AD[46]	G15	AD[14]	L15	GPIO[6]	R15	AD[49]
C16	AD[45]	G16	AD[15]	L16	AD[0]	R16	AD[48]
D1	REFCLKN	H1	RBN	M1	RDN	T1	VD33
D2	REFCLKP	H2	RBP	M2	RDP	T2	REQ_L[3] / GPI[1]
D3	VDDA_PLL	H3	VDDA	M3	VDDP	T3	HSSW
D4	VSS	H4	RREF	M4	VSS	T4	GNT_L[1]
D5	AD[31]	H5	VDDCAUX	M5	VDDC	T5	GNT_L[5] / GPO[3]
D6	AD[27]	H6	VSS	M6	VDDC	T6	CLKIN / M66EN
D7	CBE[3]	H7	VSS	M7	VD33	T7	GPIO[2]
D8	AD[20]	H8	VSS	M8	VD33	T8	CLKOUT[1]
D9	AD[16]	H9	VSS	M9	VD33	T9	CLKOUT[5]
D10	TRDY_L	H10	VSS	M10	VD33	T10	INTC_L
D11	AD[32]	H11	VDDC	M11	VDDC	T11	AD[60]
D12	AD[36]	H12	VD33	M12	VDDC	T12	AD[56]
D13	VD33	H13	AD[8]	M13	IDSEL	T13	AD[54]
D14	REQ64_L	H14	AD[9]	M14	TDO	T14	AD[51]
D15	PAR64	H15	AD[10]	M15	TDI	T15	AD[50]
D16	AD[47]	H16	AD[11]	M16	TMS	T16	VD33

3 MODE SELECTION AND PIN STRAPPING

3.1 FUNCTIONAL MODE SELECTION

If TM2 is strapped to low, PI7C9X130 uses TM1, TM0, CFN_L, and REVRSB pins to select different modes of operations. These four input signals are required to be stable during normal operation. One of the sixteen combinations of normal operation can be selected by setting the logic values for the four mode select pins. For example, if the logic values are low for all four (TM1, TM0, CFN_L, and REVRSB) pins, the normal operation will have EEPROM (I2C) support in transparent mode with internal arbiter in forward bridge mode. The designated operation with respect to the values of the TM1, TM0, CFN_L, and REVRSB pins are defined on Table 3-1:

Table 3-1 Functional Mode Selection

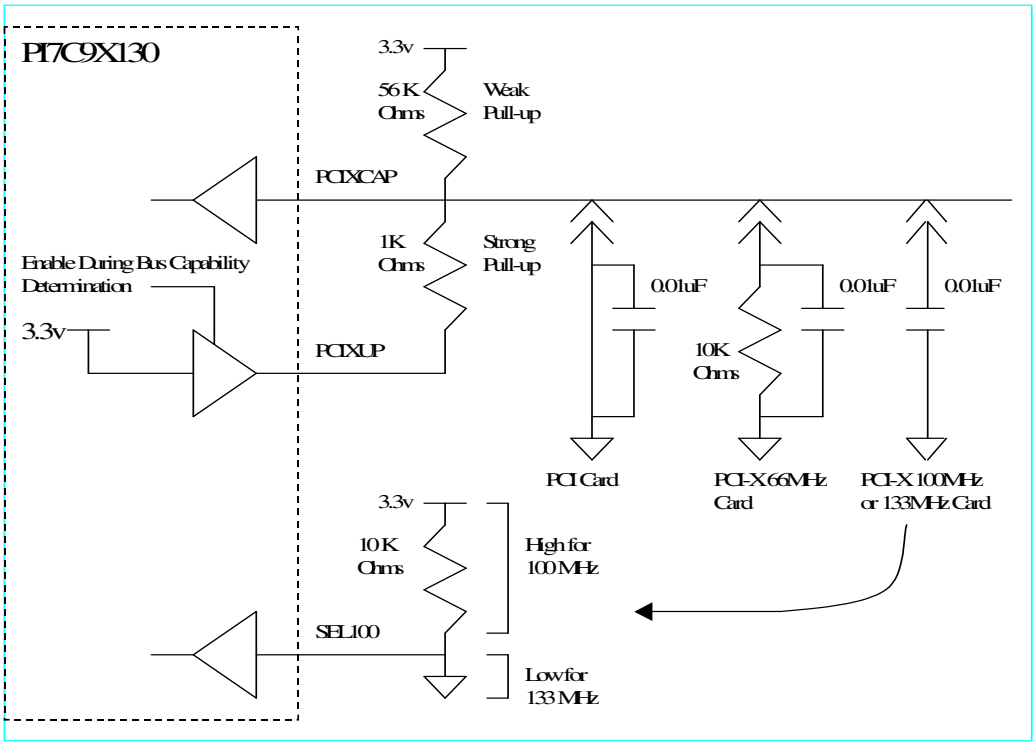
TM2 Strapped	TM1	TM0	CFN_L	REVRSB	Functional Mode
0	0	X	X	X	EEPROM (I2C) support
0	1	X	X	X	SM Bus support
0	X	0	X	X	Transparent mode
0	X	1	X	X	Non-Transparent mode
0	X	X	0	X	Internal arbiter
0	X	X	1	X	External arbiter
0	X	X	X	0	Forward bridge mode
0	X	X	X	1	Reverse bridge mode

3.2 PCI/PCI-X SELECTION

The secondary interface is capable of operating in either conventional PCI mode or in PCI-X mode. PI7C9X130 controls the mode and frequency for the secondary bus by utilizing a pull-up circuit connected to PCIXCAP. There are two pull-up resistors in the circuit as recommended by the PCI-X addendum. The first resistor is a weak pull-up (56K ohms) whose value is selected to set the voltage of PCIXCAP below its low threshold when a PCI-X 66MHz device is attached to the secondary bus. The second resistor is a strong pull-up, externally wired between PCIXCAP and PCIXUP. The value of the resistor (1K ohm) is selected to set the voltage of PCIXCAP above its high threshold when all devices on the secondary are PCI-X 66MHz capable. To detect the mode and frequency of the secondary bus, PCIXUP is initially disabled and PI7C9X130 samples the value on PCIXCAP.

If PI7C9X130 sees logic LOW on PCIXCAP, one or more devices on the secondary have either pulled the signal to ground (PCI-X 66MHz capable) or tied it to ground (only capable of conventional PCI mode). To differentiate between the two conditions, PI7C9X130 then enables PCIXUP to put the strong pull-up into the circuit node. If PCIXCAP remains at logic LOW, it must be tied to ground by one or more devices, and the bus is initialized to conventional PCI mode. If PCIXUP can be pulled up, one or more devices are capable of only PCI-X 66MHz operation so the bus is initialized to PCI-X 66MHz mode. If PI7C9X130 sees logic HIGH on PCIXCAP, then all devices on the secondary bus are capable of PCI-X 100MHz or 133MHz operation. PI7C9X130 then samples SEL100 to distinguish between the 100MHz and 133MHz clock frequencies. If PI7C9X130 sees logic HIGH on SEL100, the secondary bus is initialized to PCI-X 100MHz mode. If the value is LOW, PCI-X 133MHz is initialized. These two clock frequencies allow the flexibility to support different bus loading conditions.

Figure 3-1 PCI / PCI-X Selection



3.3 PIN STRAPPING

If TM2 is strapped to high, PI7C9X130 uses TM1, TM0, and MSK_IN as strapping pins. The strapping functions are listed in Table 3-2 to show the states of operations during the PCI Express PERST_L de-assertion transition in forward bridge mode or PCI RESET_L de-assertion transition in reverse bridge mode.

Table 3-2 Pin Strapping

TM2 Strapped	TM1 Strapped	TM0 Strapped	MSK_IN Strapped	Test Functions
1	0	0	1	PLL test
1	0	1	1	Shorten initialization test with Hot-Plug enabled
1	1	0	1	Functional loopback test
1	1	1	1	Bridge test (PRBS, IDDQ, etc.)
1	0	0	0	Reserved
1	0	1	0	Shorten initialization test with Hot-Plug disabled
1	1	0	0	Reserved
1	1	1	0	Reserved