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PI7C9X20404GP

PCI EXPRESS PACKET SWITCH

DATASHEET

REVISION 1.6

June 2009

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REVISION HISTORY

Date	Revision Number	Description
12/13/06	0.1	Initial Preliminary Datasheet
1/3/06	0.4	Proofreading an Editing
5/22/07	0.5	Revision of the registers and the description. Packaging mechanical added Corrected pin description for ATT_IND[4], TEST3, TEST4, TEST5 and TEST 6 in section 3 and 4 Corrected register description for offset F0h in section 7.2.70
7/11/07	0.6	Removed Reference Clock Output related info from 1. Features (advanced power saving), 3 Pin Description (RREF_CO, REFCLK, VDDIO), 4. Pin Assignment (RREF_CO to TEST7, REFCLK to NC, VDDIO to VDDR), 8 Clock Scheme (description), 12.2 AC Specification (VDDIO) Updated "ORDERING INFORMATION"
8/29/07	0.7	Added 12.3 AC Specifications: Transmitter and Receiver Specifications Updated 8 Clock Scheme (Table 8-1) Updated Chapter 14 Ordering Information (PI7C9X20404GPNBE) Updated Pericom Logo Added Disclaimer Added Chapter 6.2 SMBus Added SMBus related items in Chapter 1 Features Modified SMBus related pins (GPIO[5:7]) Corrected Chapter 6. EEPROM and Chapter 7. Register Description Corrected Chapter 3. Pin Description (PORTACT, TEST) and Chapter 4. Pin Assignment (B9, D3, D12, D14, E12, E14, G12, G14, H12, H14, K12, K14, L12, L13, L14, N12, N14, P2, P12, P14) Corrected Chapter 3.6 Power Pins (VDDC, VDDA, VDDCAUX to 1.1V), Chapter 3.4 Misc. Signals (TEST6 corrected, TEST7 to PWR_SAV) Updated Chapter 7.2.53 bit [15:0]
10/04/07	0.8	Updated Chapter 3.5 JTAG Signals description Updated Chapter 7.2.53 Remove VDDP, VDDAUX from Chapter 11 Power Management and Chapter 12.1 Absolute Maximum Ratings Revised Chapter 11 Power Management Updated Chapter 3 Pin Description (PERP/PERN and PETP/PETN's description, WAKEUP_L's description, VC1_EN's name and description, SLOT_IMP's description, HOTPLUG's description, SLOTCLK's description, PWR_IND's description, ATT_IND's description, MRL_PDC's description, PWR_ENA_L's description, EEPD's description, SMBDATA's description, SCAN_EN's description, PORTERR's name and description) Updated Chapter 4 Pin Assignment (VC_RS to VC1_EN, PORTACT to PORTERR) Updated 5.1 Physical Layer Circuit and Chapter 5.6 Queue Updated Disclaimer and Footer Updated Chapter 14 Ordering Information Fixed Chapter 6.1.4 Mapping EEPROM format
1/11/08	1.0	Modified Chapter 3.4 MISCELLANEOUS SIGNALS

		(GPIO[0,1,3,5]) Modified Chapter 4 PIN ASSIGNMENTS (GPIO[0,1,3,5]) Modified Chapter 6 EEPROM (0Ch) Modified Chapter 7 Registers (7.2.50 Replay Time-Out Counter, 7.2.52 Switch Operation Mode Bit[14,15,17], 7.2.53 Switch Operation Mode Bit[8:15], 7.2.64 PCI Express Capability Bit[24] , 7.2.70 Link Status Bit[28], 7.2.103 Power Budgeting Data, 7.2.104 Power Budget Capability)
1/30/08	1.1	Corrected 3.5 JTAG Boundary Scan Signal
2/20/08	1.2	Updated Chapter 3.5 Power Pins (VDDC, VDDA, VDDCAUX) Updated Chapter 1 Features (Power Dissipation) Updated Chapter 12.2 DC Specification (Power Consumption, VDDCAUX)
4/15/08	1.3	Updated Chapter 3.1 PCI Express Interface Signals (REFCLKP, REFCLKN) Corrected Chapter 12.2 DC Specifications
7/1/08	1.4	Modified Chapter 1 Features (Industrial Temperature) Corrected Chapter 7.2.27 Interrupt Pin Register Corrected Chapter 7.2.32 Power Management Data Register Bit 3 Corrected Chapter 7.2.51 Acknowledge Latency Timer Modified Chapter 12.1 Absolute Maximum Ratings (Ambient Temperature with power applied)
11/26/08	1.5	Updated Chapter 14 Ordering Information Removed “Preliminary” and “Confidential” references
6/8/09	1.6	Updated Chapter 3.2 Port Configuration Signals (SLOT_IMP, HOTPLUG, SLOTCLK) Updated Chapter 3.3 Hot Plug Signals (PWR_IND, ATT_IND) Updated Chapter 3.4 Miscellaneous Signals (PWR_SAV pin removed, EEPD) Updated Chapter 3.5 JTAG Boundary Scan Signals (TMS, TDI, TRST_L)

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1 Features

- 4-lane PCI Express Switch with 4 PCI Express ports
- Non-blocking full-wired switching capability at 16 Gbps when all 4 ports are enabled
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for packet switching
- Peer-to-peer switching between any two downstream ports
- 150 ns typical latency for packet routed through Switch without blocking
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Compliant with System Management (SM) Bus, Version 1.0
- Compliant with *PCI Express Base Specification Revision 1.1*
- Compliant with *PCI Express CEM Specification Revision 1.1*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Compliant with *PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification Revision 1.0*
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
  - Hot Plug support
  - IEEE 1149.6 JTAG interface support
- Advanced Power Saving
  - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
  - Supports L0, L0s, L1, L2, L2/$L3_{Ready}$ and L3 link power states
  - Active state power management for L0s and L1 states
  - Beacon or Wake# support in L2 state
- Device State Power Management
  - Supports D0, $D3_{Hot}$ and $D3_{Cold}$ device power states
  - 3.3V Aux Power support in $D3_{Cold}$ power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Disabled VCs' buffer is assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping for each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Supports up to 256-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Low Power Dissipation at 0.8W typical in L0 normal mode
- Industrial Temperature Range -40° to 85°C
- 148-pin LFBGA 12mm x 12mm package, 0.8 mm Ball Pitch

2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 4-lane PCIE Switch can be configured as 4-port type combinations. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs. For some systems that do not need all the 4 lanes, the unused lanes can be disabled to reduce power consumption.

In the PCI Express Architecture, the PCIE Switch forwards posted and non-posted requests and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

3 PIN DESCRIPTION

3.1 PCI EXPRESS INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
REFCLKP REFCLKN	A8 B8	I	**Reference Clock Input Pairs:** Connect to external 100MHz differential clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
PERP [3:0]	G14, L14, N12, E12	I	**PCI Express Data Serial Input Pairs:** Differential data receive signals in four ports. Port 0 (Upstream Port) is PERP[0] and PERN[0] Port 1 (Downstream Port) is PERP[1] and PERN[1] Port 2 (Downstream Port) is PERP[2] and PERN[2] Port 3 (Downstream Port) is PERP[3] and PERN[3]
PERN [3:0]	H14, K14, P12, D12	I	
PETP [3:0]	H12, K12, P14, D14	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals in four ports. Port 0 (Upstream Port) is PETP[0] and PETN[0] Port 1 (Downstream Port) is PETP[1] and PETN[1] Port 2 (Downstream Port) is PETP[2] and PETN[2] Port 3 (Downstream Port) is PETP[3] and PETN[3]
PETN [3:0]	G12, L12, N14, E14	O	
WAKEUP_L	A1	I	**Wakeup Signal (Active LOW):** When WAKEUP_L is asserted, the upstream port has to generate a Beacon that is propagated to the Root Complex/Power Management Controller. Pin has an internal pull-up.
RESET_L	D2	I	**System Reset (Active LOW):** When RESET_L is asserted, the internal states of whole chip except sticky logics are initialized.
DWNRST_L [3:1]	B3, A3, C2	O	**Downstream Device Reset (Active LOW):** It provides a reset signal to the devices connected to the downstream ports of Switch. The signal is active when either RESET_L is asserted or the device is just plugged into the Switch. DWNRST_L [x] corresponds to Portx, where x= 1,2,3.

3.2 PORT CONFIGURATION SIGNALS

NAME	PIN	TYPE	DESCRIPTION
VC1_EN	B1	I	**Virtual Channel 1 Enable:** The chip provides the capability to support virtual channel 1 (VC1), in addition to the standard virtual channel 0. When this pin is asserted high, Virtual Channel 1 is enabled, and virtual channel resource sharing is not available. When it is asserted low, the chip would allocate the additional VC1 resource to VC0, and VC1 capability is disabled. The pin has internal pull-down.
SLOT_IMP [3:1]	B4, C4, E3	I	**Slot Implemented:** It decides if the downstream port is connected to slot. SLOT_IMP [x] is correspondent to Portx, where x= 1,2,3.When SLOT_IMP [x] is high, the Portx is connected to slot. By default, downstream Port1, Port2, and Port3 are implemented with slots. The pins have internal pull-up.
HOTPLUG [3:1]	A5, B5, C5	I	**Hot Plug Capability:** It determines if the downstream port is able to support hot plug capability. HOTPLUG [x] is correspondent to Portx, where x=1,2,3. When HOTPLUG [x] is high, Portx supports hot plug operation. By default, downstream Port1, Port2, and Port3 are equipped with hot plug function. The pins have internal pull-up.
SLOTCLK	F3	I	**Slot Clock Configuration:** It determines if the all downstream components uses the same physical reference clock that the platform provides on the connector. When SLOTCLK is high, the platform reference clock is employed. By default, all downstream ports use the same physical reference clock provided by platform. The pins have internal pull-up.

3.3 HOT PLUG SIGNALS

NAME	PIN	TYPE	DESCRIPTION
PWR_IND [3:1]	N5, M5, L3	O	**Power Indicator:** Indicates the power status for each slot at downstream port. PWR_IND [x] is correspondent to Port x, where x=1,2,3. They are active-high signals. The pins have internal pull-down.
ATT_IND [3:1]	M1, N1, N2	O	**Attention Indicator:** Indicates the attention status for each slot at downstream port. ATT_IND [x] is correspondent to Port x, where x=1,2,3. They are active-high signals. ATT_IND[3:2] have internal pull-down.
ATT_BTN [3:1]	K3, K2, K1	I	**Attention Button:** When asserted high, it represents the attention button has been pressed for the slot at the downstream port. ATT_BTN [x] is correspondent to Port x, where x=1,2,3.
MRL_PDC [3:1]	N7, M7, J1	I	**Presence Detected Change:** When asserted low, it represents the device is present in the slot of downstream ports. Otherwise, it represents the absence of the device. MRL_PDC [x] is correspondent to Port x, where x=1,2,3.
PWR_ENA_L [3:1]	P2, J2, H1	O	**SLOT Power Enable (Active LOW):** Indicates the enable status of the power connecting to the associated slot. PWR_ENA [x] is correspondent to Portx, where x=1,2,3. They are active-low signals. Pins are set to "000" by default.
PWR_FLT [3:1]	N8, M8, P4	I	**SLOT Power Fault:** When asserted high, it indicates a power fault on one or more supply rails. PWR_FLT [x] is correspondent to Port x, where x=1,2,3.

3.4 MISCELLANEOUS SIGNALS

NAME	PIN	TYPE	DESCRIPTION
EECLK	P8	O	**EEPROM Clock:** Clock signal to the EEPROM interface.
EEPD	M9	I/O	**EEPROM Data: Bi-directional** serial data interface to and from the EEPROM. The pin has internal pull-up.
SMBCLK	N4	I	**SM Bus Clock:** System management Bus Clock. Pin has an internal pull-down.
SMBDATA	L2	I/O	**SM Bus Data: Bi-Directional** System Management Bus Data.
SCAN_EN	P10	I/O	**Full-Scan Enable Control:** For normal operation, SCAN_EN is an output with a value of "0". SCAN_EN becomes an input during manufacturing testing.
PORTERR [3:0]	N9, P7, P6, P5	O	**Port PHY Error Status:** These pins are used to display the PHY Error status of the ports. When PORTERR is flashing (alternating high and low signals), it indicates that a PHY error is detected. When it is low, no PHY error is detected. PORTERR [x] is correspondent to Port x, where x=0,1,2,3.
GPIO [7:0]	F1, E1, G2, G3, D1, C1, F2, E2	I/O	**General Purpose Input and Output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register. When SMBus is implemented, GPIO[7:5] act as the SMBus address pins, which set Bit 2 to 0 of the SMBus address.
TEST1	G1	I	**Test1:** This pin is for internal test purpose. Test1 should be tied to ground through a pull-down resistor.
TEST2 TEST3 TEST4 TEST5	C3 C6 B6 A6	I	**Test2/3/4/5:** These pins are for internal test purpose. Test2, Test3, Test4 and Test5 should be tied to 3.3V through a pull-up resistor.
TEST6	B11	I	**Test6:** This pin is for internal test purpose. Test6 should be connected an (475 ohm +/- 1%) external resistor to Vss.
TEST7	M6	I	**Test7:** This pin is for internal test purpose. Test7 should be tied to ground through a pull-down resistor (5.1k ohm).
NC	A10, A12, A14, B10, B12, B14, H3, L1, M2, M3, M4, N3		**Not Connected:** These pins can be just left open.

3.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN	TYPE	DESCRIPTION
TCK	M10	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	P11	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. The pin has internal pull-up. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.
TDO	N10	O	**Test Data Output:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	N11	I	**Test Data Input:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. The pin has internal pull-up. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TRST_L	M11	I	**Test Reset (Active LOW):** Active LOW signal to reset the TAP controller into an initialized state. The pin has internal pull-up. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.

3.6 POWER PINS

NAME	PIN	TYPE	DESCRIPTION
VDDC	C7, F6, F7, F9, G6, G7, G9, H6, H7, H9, J3, J6, J7, J9	P	**VDDC Supply (1.0V):** Used as digital core power pins.
VDDR	A4, A9, C12, H2, N6, P13	P	**VDDR Supply (3.3V):** Used as digital I/O power pins.
VDDA	C9, J12, J13, J14, K13	P	**VDDA Supply (1.0V):** Used as analog power pins.
VDDCAUX	D3, L13	P	**VDDCAUX Supply (1.0V):** Used as auxiliary core power pins.
VAUX	A2	P	**VAUX Supply (3.3V):** Used as auxiliary I/O power pins.
VTT	F12, M12	P	**Transmit Termination Voltage (1.5V):** Provides driver termination voltage at transmitter. Should be given the same consideration as VDDCAUX.
VSS	A7, A11, A13, B2, B7, B9, B13, C8, C10, C11, C13, C14, D13, E13, F8, F13, F14, G8, G13, H8, H13, J8, M13, M14, N13, P1, P3, P9	P	**VSS Ground:** Used as ground pins.

4 PIN ASSIGNMENTS

4.1 PIN LIST of 148-PIN LFBGA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	WAKEUP_L	C10	VSS	H1	PWR_ENA_L[1]	M6	TEST7
A2	VAUX	C11	VSS	H2	VDDR	M7	MRL_PDC[2]
A3	DWNRST_L[2]	C12	VDDR	H3	NC	M8	PWR_FLT[2]
A4	VDDR	C13	VSS	H6	VDDC	M9	EEPD
A5	HOTPLUG[3]	C14	VSS	H7	VDDC	M10	TCK
A6	TEST5	D1	GPIO[3]	H8	VSS	M11	TRST_L
A7	VSS	D2	RESET_L	H9	VDDC	M12	VTT
A8	REFCLKP	D3	VDDCAUX	H12	PETP[3]	M13	VSS
A9	VDDR	D12	PERN[0]	H13	VSS	M14	VSS
A10	NC	D13	VSS	H14	PERN[3]	N1	ATT_IND[2]
A11	VSS	D14	PETP[0]	J1	MRL_PDC[1]	N2	ATT_IND[1]
A12	NC	E1	GPIO[6]	J2	PWR_ENA_L[2]	N3	NC
A13	VSS	E2	GPIO[0]	J3	VDDC	N4	SMBCLK
A14	NC	E3	SLOT_IMP[1]	J6	VDDC	N5	PWR_IND[3]
B1	VC1_EN	E12	PERP[0]	J7	VDDC	N6	VDDR
B2	VSS	E13	VSS	J8	VSS	N7	MRL_PDC[3]
B3	DWNRST_L[3]	E14	PETN[0]	J9	VDDC	N8	PWR_FLT[3]
B4	SLOT_IMP[3]	F1	GPIO[7]	J12	VDDA	N9	PORTERR[3]
B5	HOTPLUG[2]	F2	GPIO[1]	J13	VDDA	N10	TDO
B6	TEST4	F3	SLOTCLK	J14	VDDA	N11	TDI
B7	VSS	F6	VDDC	K1	ATT_BTN[1]	N12	PERP[1]
B8	REFCLKN	F7	VDDC	K2	ATT_BTN[2]	N13	VSS
B9	VSS	F8	VSS	K3	ATT_BTN[3]	N14	PETN[1]
B10	NC	F9	VDDC	K12	PETP[2]	P1	VSS
B11	TEST6	F12	VTT	K13	VDDA	P2	PWR_ENA_L[3]
B12	NC	F13	VSS	K14	PERN[2]	P3	VSS
B13	VSS	F14	VSS	L1	NC	P4	PWR_FLT[1]
B14	NC	G1	TEST1	L2	SMBDATA	P5	PORTERR[0]
C1	GPIO[2]	G2	GPIO[5]	L3	PWR_IND[1]	P6	PORTERR[1]
C2	DWNRST_L[1]	G3	GPIO[4]	L12	PETN[2]	P7	PORTERR[2]
C3	TEST2	G6	VDDC	L13	VDDCAUX	P8	EECLK
C4	SLOT_IMP[2]	G7	VDDC	L14	PERP[2]	P9	VSS
C5	HOTPLUG[1]	G8	VSS	M1	ATT_IND[3]	P10	SCAN_EN
C6	TEST3	G9	VDDC	M2	NC	P11	TMS
C7	VDDC	G12	PETN[3]	M3	NC	P12	PERN[1]
C8	VSS	G13	VSS	M4	NC	P13	VDDR
C9	VDDA	G14	PERP[3]	M5	PWR_IND[2]	P14	PETP[1]

5 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

5.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the **P**HY **I**nterface for **P**CI **E**xpress Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. In addition, a pair of PRBS generator and checker is included for PHY built-in self test. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the different application needs, the driving current and equalization of each transmitting channels can be adjusted using EEPROM individually. The driver current of each channel is set to 20mA in default mode. To change the current value, the user can program the EEPROM for nominal value (HIDRV, LODRV) or actual value (DTX [3:0]), which is a scaled multiple of Inom. The following tables illustrate the possible transmitted current values the chip provides.

Table 5-1 Nominal Driver Current Values (Inom)

HIDRV	LODRV	NOMINAL DRIVER CURENT
0	0	20 mA
0	1	10 mA
1	0	28 mA
1	1	Reserved

Table 5-2 Ratio of Actual Current and Nominal Current

DTX [3:0]	ACTUAL CURRENT / NOMINAL CURRENT
0000	1.00
0001	1.05
0010	1.10
0011	1.15
0100	1.20
0101	1.25
0110	1.30

[1] Multiple lanes could share the PLL.

DTX [3:0]	ACTUAL CURRENT / NOMINAL CURRENT
0111	1.35
1000	0.60
1001	0.65
1010	0.70
1011	0.75
1100	0.80
1101	0.85
1110	0.90
1111	0.95

The equalization function of transmitting channels can optimize the driver current for different back-plane lengths and materials. The table shown below lists the combinations of de-emphasized driver current ($I_{TX} - I_{EQ}$) to non-de-emphasized driver current (I_{TX}) for different values of DEQ [3:0].

Table 5-3 De-emphasis Level versus DEQ [3:0]

DEQ [3:0]	$(I_{TX} - I_{EQ}) / I_{TX}$	De-emphasis (dB)
0000	1.00	0.00
0001	0.96	-0.35
0010	0.92	-0.72
0011	0.88	-1.11
0100	0.84	-1.51
0101	0.80	-1.94
0110	0.76	-2.38
0111	0.72	-2.85
1000	0.68	-3.35
1001	0.64	-3.88
1010	0.60	-4.44
1011	0.56	-5.04
1100	0.52	-5.68
1101	0.48	-6.38
1110	0.44	-7.13
1111	0.40	-7.96

By default, the DEQ is set to "1000" conform to the PCI Express 1.0a specification, which calls for a de-emphasis level of between –3 dB and –4 dB.

In order to improve the data stream integrity across the channels, the receiver of each port of the Switch includes a reception equalizer to mitigate the effects of ISI. The reception equalizer is implemented as a selectable high-pass filter at the input node, and it is capable of removing as much as 0.4UI of ISI related jitter. The following table shows a simple guideline for selecting the appropriate value to adapt with different lengths or connector numbers in various applications.

Table 5-4 Rx Equalizer Settings (RXEQCTL)

RXEQCTL [1]	RXEQCTL [0]	Rx Eq Setting	Input Jitter	Channel Length
0	0	Max Rx Eq	> 0.25 UI	> 20" and two or more connectors
0	1	Min Rx Eq	Between 0.1 UI and 0.25 UI	Between 8" and 20" and up to two connectors
1	X		< 0.1 UI	8" or less, up to one connector

5.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes deskew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

5.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

5.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet can not be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

5.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.

5.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1) has its own corresponding packet header and data queue. When only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

5.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

5.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

5.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

5.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there is no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

5.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

5.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 5-4 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

Table 5-4 Summary of PCI Express Ordering Rules

Row Pass Column	Posted Request	Read Request	Non-posted Write Request	Read Completion	Non-posted Write Completion
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older Bridges that do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue.

5.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which input traffic to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At upstream port, in addition to the traffic from inter-port, the intra-port packet such as configurations completion would also join the arbitration loop to get the service in Virtual Channel 0.

5.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC. They are respectively Strict Priority, Round Robin or Weighted Round Robin.

5.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this switch, each port has separate queues for different traffic types and the credits are on the fly sent to data link layer, which compares the current available credits with the monitored one and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent from link entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. It would broadcast them to all the other ingress ports for gating the packet transmission.

5.11 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They are to construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packet when the local resource (i.e. configuration register) is accessed and regenerate the message that terminated at receiver to RC if acts as an upstream port.

6 EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS

The EEPROM interface consists of two pins: EECLK (EEPROM clock output) and EEPD (EEPROM bi-directional serial data). The Switch may control an ISSI IS24C04 or compatible parts using into 512x8 bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PRST# is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies a 7-bit EEPROM word address. The Switch does not control the EEPROM address input. It can only access the EEPROM with address input set to 0.

The System Management Bus interface consists of two pins: SMBCLK (System Management Bus Clock input) and SMBDATA (System Management Bus Data input/ output).

6.1 EEPROM INTERFACE

6.1.1 AUTO MODE EERPOM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

6.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [3] offset DCh (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '0' which indicates that the autoload initialization sequence is complete.

6.1.3 EEPROM SPACE ADDRESS MAP

15 – 8	7 – 0	BYTE OFFSET
EEPROM Signature (1516h)		00h
Vendor ID		02h
Device ID		04h
Extended VC Count / Link Capability / Switch Mode Operation / Interrupt pin for Port 1 ~ 3		06h
Subsystem Vender ID		08h
Subsystem ID		0Ah
Max_Payload_Size Support / ASPM Support / Role_Base Error Reporting / RefClk ppm Difference		0Ch
Reserved		0Eh
PM Data for Port 0	PM Capability for Port 0	10h
PM Data for Port 1	PM Capability for Port 1	12h
PM Data for Port 2	PM Capability for Port 2	14h
PM Data for Port 3	PM Capability for Port 3	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch

15 – 8	7 – 0	BYTE OFFSET
Reserved		1Eh
TC/VC Map for Port 0 (VC0)	Slot Clock / LPVC Count / Port Num, Port 0	20h
TC/VC Map for Port 1(VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 1	22h
TC/VC Map for Port 2 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 2	24h
TC/VC Map for Port 3 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 3	26h
Reserved		28h
Reserved		2Ah
Reserved		2Ch
Reserved		2Eh
Reserved		30h
Slot Capability 0 for Port 1		32h
Slot Capability 0 for Port 2		34h
Slot Capability 0 for Port 3		36h
Reserved		38h
Reserved		3Ah
Reserved		3Ch
Reserved		3Eh
Reserved		40h
Slot Capability 1 for Port 1		42h
Slot Capability 1 for Port 2		44h
Slot Capability 1 for Port 3		46h
Reserved		48h
Reserved		4Ah
Reserved		4Ch
Reserved		4Eh
TC/VC Map for Port 0 (VC1)	Maximum Time Slot for Port 0	50h
TC/VC Map for Port 1 (VC1)	Maximum Time Slot for Port 1	52h
TC/VC Map for Port 2 (VC1)	Maximum Time Slot for Port 2	54h
TC/VC Map for Port 3 (VC1)	Maximum Time Slot for Port 3	56h
Reserved		58h
Reserved		5Ah
Reserved		5Ch
Reserved		5Eh
Power Budgeting Capability Register for Port 0		60h
Power Budgeting Capability Register for Port 1		62h
Power Budgeting Capability Register for Port 2		64h
Power Budgeting Capability Register for Port 3		66h
Reserved		68h
Reserved		6Ah
Reserved		6Ch
Reserved		6Eh
Replay Time-out Counter for Port 0		70h
Replay Time-out Counter for Port 1		72h
Replay Time-out Counter for Port 2		74h
Replay Time-out Counter for Port 3		76h
Reserved		78h
Reserved		7Ah
Reserved		7Ch
Reserved		7Eh
Acknowledge Latency Timer for Port 0		80h
Acknowledge Latency Timer for Port 1		82h
Acknowledge Latency Timer for Port 2		84h
Acknowledge Latency Timer for Port 3		86h
Reserved		88h
Reserved		8Ah
Reserved		8Ch
Reserved		8Eh
PHY Parameter for Port 0		90h
PHY Parameter for Port 1		92h

15 – 8	7 – 0	BYTE OFFSET
PHY Parameter for Port 2		94h
PHY Parameter for Port 3		96h
Reserved		98h
Reserved		9Ah
Reserved		9Ch
Reserved		9Eh
Reserved	PM Control Para/Rx Polarity for Port 0	A0h
Reserved	PM Control Para/Rx Polarity for Port 1	A2h
Reserved	PM Control Para/Rx Polarity for Port 2	A4h
Reserved	PM Control Para/Rx Polarity for Port 3	A6h

6.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

ADDRESS	PCI CFG OFFSET	DESCRIPTION
00h		**EEPROM signature** – 1516h
02h	00h ~ 01h	**Vendor ID**
04h	02h ~ 03h	**Device ID**
06h	144h (Port 0~3) 144h: Bit [0]	**Extended VC Count for Port 0 ~ 3** ▪ Bit [0]: It represents the supported VC count other than the default VC
	ECh (Port 0~3) ECh: Bit [14:12] ECh: Bit [17:15]	**Link Capability for Port 0 ~ 3** ▪ Bit [3:1]: It represents L0s Exit Latency for all ports ▪ Bit [6:4]: It represents L1 Exit Latency for all ports
	B4h (Port 0~3) B4h:Bit [5] Bit [6] Bit [0] Bit [2:1] Bit [3] Bit [4]	**Switch Mode Operation for Port 0** ▪ Bit [8]: no ordering on packets for different egress port mode ▪ Bit [9]: no ordering on different tag of completion mode ▪ Bit [10]: Store and Forward ▪ Bit [12:11]: Cut-through Threshold ▪ Bit [13] : Port arbitrator Mode ▪ Bit [14]: Credit Update Mode
	3Ch (Port 1~3) 3Ch: Bit [8]]	**Interrupt pin for Port 1 ~ 3** ▪ Bit [15]: Set when INTA is requested for interrupt resource
08h	BCh: Bit [15:0]	**Subsystem Vender ID**
0Ah	BCh: Bit [31:16]	**Subsystem ID**
0Ch	E4h(Port 0~3) E4h: Bit 0	**Max_Payload_Size Support for Port 0 ~ 3** ▪ Bit [0]: Indicated the maximum payload size that the device can support for the TLP
	ECh(Port 0~3) ECh: Bit[11:10]	**ASPM Support for Port 0 ~ 3** ▪ Bit [2:1] : Indicate the level of ASPM supported on the PCIe link
	E4h(Port 0~3) E4h: Bit[15]	**Role_Base Error Reporting for Port 0 ~ 3** ▪ Bit [3] : Indicate implement the role-base error reporting
	B0h(port 0~3) B0h : Bit [14]	**MSI Capability Disable for Port 0~3** ▪ Bit [4] : Disable MSI capability
	B0h(port 0~3) B0h : Bit [15]	**AER Capability Disable for Port 0~3** ▪ Bit [5] : Disable AER capability
	B4h(port 0~3) B4h : Bit [15]	**Compliance Pattern Parity Control Disable for Port 0~3** ▪ Bit [6] : Disable compliance pattern parity
	B0h(port 0~3) B0h : Bit [13]	**Power Management Capability Disable for Port 0~3** ▪ Bit [7] : Disable Power Management Capability
	A8h(Port 0~3)	**RefClk ppm Difference for Port 0 ~ 3**

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	A8h: Bit [14:13]	▪ Bit [9:8]: It represents RefClk ppm difference between the two ends in one link; 00: 0 ppm, 01: 100 ppm, 10: 200 ppm, 11: 300 ppm
10h	84h (Port 0) 84h: Bit [3] 80h (Port 0) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 0** ▪ Bit [0]: No_Soft_Reset. **Power Management Capability for Port 0** ▪ Bit [3:1]: AUX Current. ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
11h	84h (Port 0) 84h: Bit [31:24]	**Power Management Data for Port 0** ▪ Bit [15:8]: read only as Data register
12h	84h (Port 1) 84h: Bit [3] 80h (Port 1) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 1** ▪ Bit [0]: No_Soft_Reset. **Power Management Capability for Port 1** ▪ Bit [3:1]: AUX Current. ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
13h	84h (Port 1) 84h: Bit [31:24]	**Power Management Data for Port 1** ▪ Bit [15:8] – read only as Data register
14h	84h (Port 2) 84h: Bit [3] 80h (Port 2) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 2** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 2** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
15h	84h (Port 2) 84h: Bit [31:24]	**Power Management Data for Port 2** ▪ Bit [15:8] – read only as Data register
16h	84h (Port 3) 84h: Bit [3] 80h (Port 3) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 3** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 3** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
17h	84h (Port 3) 84h: Bit [31:24]	**Power Management Data for Port 3** ▪ Bit [15:8] – read only as Data register
20h	F0h (Port 0) F0h: Bit [28] 80h (Port 0) 80h: Bit[21] 144h (Port 0) 144h: Bit [4] ECh (Port 0) ECh: Bit [25:24]	**Slot Clock Configuration for Port 0** ▪ Bit [1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 0** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 0** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 0 **Port Number for Port 0** ▪ Bit [5:4]: It represents the logic port numbering for physical port 0