Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PI7C9X442SL

PCI EXPRESS TO USB 2.0 SWIDGE

DATASHEET

REVISION 3

January 2018

A Product Line of Diodes Incorporated

1545 Barber Lane Milpitas, CA 95035
Telephone: 408-232-9100
FAX: 408-434-1040
Internet: http://www.diodes.com

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the
failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com

REVISION HISTORY

Date	Revision Number	Description
5/27/09	0.2	Preliminary datasheet
10/20/09	0.3	Added Section 6 EEPROM Interface and System Management Bus Added Section 7 Register Description Updated Table 11-3 DC Electrical Characteristics
6/11/10	0.4	Updated Section 6.1.3 EEPROM Space Address Map and 6.1.4 Mapping EEPROM Contents to Configuration Registers (Offset – C0h, C2h, C4h Physical Layer Control 3) Updated Section 7.2 PCI Express Configuration Registers (Offset – C0h, C4h, C8h) Added Section 14 Recommended Components
6/23/10	0.5	Updated Section 3 Pin Definition and Section 4 Pin Assignments (VDDCAUX to ADDC, VAUX to VDDR) Updated Figure 12-1 Package outline drawing
8/27/10	0.6	Updated Section 1 Features (Industrial Temperature Range) Updated Section 3.3 USB Interface Signals (OCI and POE pins) Updated Section 3.5 Miscellaneous Signals (NC pins) Updated Section 13 Ordering Information (Industrial Temperature Range) Updated Table 11-1 (Ambient Temperature with power applied)
11/18/10	0.7	Updated Section 3.3 USB Interface Signals (PME_L pin) Updated Section 3.5 Miscellaneous Signals (MAIN_DETECT, GPIO and SMBCLK pins) Corrected Section 4.1 Pin List (Pin 30, 31, 32) Updated Section 6.1.4 Mapping EEPROM Contents to Configuration Registers (24h, 3Eh) Updated Section 7.3.17 Serial Bus Release Number Register, 7.3.18 Miscellaneous Register
12/23/10	0.8	Updated 7.3.10 Base Address Register 0, 7.3.11 Base Address Register 0, 7.3.17 Serial Bus Release Number Register, 7.3.18 Frame Length Adjustment Register, 7.3.19 Port Wake Capability Register, 7.3.22 Power Management Data Register, 7.3.27 Message Signaled Interrupt Capability ID Register, 7.3.29 Message Control Register, 7.3.30 Message Address Register, 7.3.31 Message Data Register, 7.3.40 Device Control Register, 7.3.42 Link Capabilities Register, 7.3.43 Link Control Register
4/29/11	1.0	Updated Table 9-3 JTAG boundary scan register definition Updated 7.3.24 Power Management Data Register (bit 15) Production PI7X9X442SL datasheet revision 1.0 released
6/10/11	1.1	Updated Section 8.2 USB Interface Updated Section 10.1 Express Power States Updated Section 11.3 DC Specification
7/15/11	1.2	Update Section 7.2.46, 7.2.53. 7.2.55. 7.2.57, 7.2.58 and 7.3.40.
11/7/11	1.3	Added Table 8.2 Input Clock Requirements for USB Interface
11/23/11	1.4	Added Table 11-4 DC electrical characteristics for Digital I/O Updated Table 11-7 USB Interface Characteristics
02/13/11	1.5	Updated 3.5 Miscellaneous Signals (SLOTCLK) Updated 5.1.1.3 Receiver Equalization Updated 5.1.1.6 Driver Amplitude Updated 7.2.53 Physical Layer Control 0 - Offset B4h (Upstream Port) Updated 7.2.55 Physical Layer Control 0 - Offset B4h (Downstream Port)
08/13/12	1.6	Updated 1 Features (Power Dissipation) Updated 3.5 Miscellaneous Signals (GPIO) Updated 11.2 Power Consumption
05/06/13	1.7	Updated 2. General Description (peer-to-peer feature)
09/25/13	1.8	Updated 3.6 Power Pins (Added pin 129 to VSS) Updated 4.1 Pin Assignments (Added pin 129)
01/09/15	1.9	Updated 12 Package Information
01/05/16	2.0	Updated 12 Package Information
01/17/17	2.1	Updated Table 11-4 DC Electrical Characteristics for Digital I/O Updated Logo Updated Section 11.1 Absolute Maximum Ratings Added Section 11.2 Operating Ambient Temperature Updated Figure 12.1 Package Outline Drawing
03/09/17	2.2	Updated 3.4 Jtag Boundary Scan Signals

Date	Revision Number	Description
		Updated Figure 12-1 Package Outline Drawing Updated Section 11.1 Absolute Maximum Ratings Remove Section 14 Recommended Components
01/11/18	3	Revision numbering system changed to whole number Updated Section 13 Ordering Information Added 12-2 Part Marking

TABLE OF CONTENTS

TABLE OF FIGURES

LIST OF TABLES

1 Features

General Features

- PCI Express to four USB 2.0 and two PCI Express downstream ports
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Low Power Dissipation at 448 mW typical in L0 normal mode
- Industrial Temperature Range -40°C to 85°C
- 128-pin LQFP 14mm x 14mm package

Industrial Compliance

- Compliant with PCI Express Base Specification Revision 1.1
- Compliant with PCI Express CEM Specification Revision 1.1
- Compliant with PCI-to-PCI Bridge Architecture Specification Revision 1.2
- Compliant with Advanced Configuration Power Interface (ACPI) Specification
- Compliant with Universal Serial Bus Specification Revision 2.0 (data rate 1.5/12/480 Mbps)
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 1.0
- Compliant with System Management (SM) Bus, Version 1.0

PCI Express Swidge

- One x1 PCIe 1.1 upstream port and two x1 PCIe 1.1 downstream ports
- Supports "Cut-Through" (default) as well as "Store and Forward" mode
- 150 ns typical latency for packets routed through Swidge without blocking
- Non-blocking full-wired switching capability at 16 Gbps provided for all 3 PCI Express ports and all 4 USB 2.0 ports
- Advanced Power Saving
    - Empty downstream ports are set to idle state to minimize power consumption
    - Link Power Management
    - Supports L0, L0s, L1, L2, L2/L3Ready and L3 link power state
    - Active state power management for L0s and L1 state
    - PME# support in L2 state
    - Device State Power Management
    - Supports D0, D3Hot and D3Cold device power state
    - 3.3V Aux Power support in D3Cold power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-Based Weighted RR
- Supports up to 256-byte maximum payload size
- Programmable driver current and de-emphasis level at each PCIe port
- Reliability, Availability and Serviceability

USB Host Controller

- USB Root Hub with 4 downstream facing ports shared by OHCI and EHCI host controllers
- All USB downstream facing ports are able to handle high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) transactions
- PCI Express to USB bridging through PCI Express multi-functional core of PI7C9X442SL
- Two OHCI host controllers for full-speed and low-speed and one EHCI host controller for high-speed
- Programmable PHY parameters for each USB port
- Operational registers of the USB Host Controller are directly mapped to PCI memory space

2 GENERAL DESCRIPTION

PI7C9X442SL PCI Express-to-USB 2.0 Swidge is a multi-functional device that combines the functionalities of PCI Express (PCIe) Packet Switch and PCIe-to-USB2.0 Bridge. The high-performance interconnect architecture of PI7C9X442SL is capable of fanning out from one PCIe x1 upstream port to two x1 downstream and four USB 2.0 ports. The device allows simultaneous access to multiple PCIe and USB devices from system host processor, and therefore expands the connectivity domain of the system. The high-speed and low-latency switch architecture offers 16 Gbps aggregated, full-duplex switching capacity for four integrated high-speed channels, one of which is used to bridge into four USB links. The device can operate at either store-and-forward or cut-through mode and support eight Traffic Classes (TCs) and one Virtual Channel (VC) with flexible and efficient resource management. The USB ports of the device can support all the available speeds including High-Speed (HS), Full-Speed (FS) and Low-Speed (LS). The PCIe-to-USB2.0 bridge function of the device is implemented by two types of host controllers, the Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OHCI). There are one EHCI controller and two OHCI controllers residing in PI7C9X442SL. The EHCI controller handles High-Speed USB transaction while the OHCI controllers handle Full-Speed or Low-Speed USB transaction.

From the perspective of system model, the PCIe switch forwards posted, non-posted request and completion packets in downstream or upstream direction concurrently as if a virtual PCI bridge is in operation at each port. By visualizing the port as a virtual bridge, the switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI bridges, where one upstream-port bridge sits upon all downstream-port bridges over a virtual PCI bus. In addition, three USB controllers are attached to one of the PCI Express downstream ports. During enumeration, each PCIe port is given a unique bus number, device number and function number that are logically formed as a destination ID. The USB host controllers are viewed as a multi-functional device by the bootstrapping procedures. The EHCI controller is assigned function #2 and the two OHCI controllers are assigned function #0 and #1, and all the controllers are assigned the same device number. The memory-map and IO address ranges are exclusively allocated to each port and USB host controller. After the software enumeration is completed, the transaction packets are routed to the dedicated PCIe port or USB host controller based on the embedded contents of address or destination ID.

For the PCIe switching function, the traffic from two PCIe downstream ports and one PCIe upstream port are exchanged in the direction of either upstream or downstream. For the PCIe-to-USB bridging function, the four USB ports are first served in a host-centric manner by EHCI or OHCI host controllers, which then interface with the PCIe port to transfer packets to/from the upstream port through switch fabric. At High-Speed mode, all the USB ports are handled by ECHI controller with function #2. At Full-Speed and Low-Speed modes, USB port #1 and port #2 are handled by OHCI controller with function #0 and USB port #3 and port #4 are handled by OHCI controller with function #1. The Root Hub resides between the USB ports and host controllers and handles connection sessions from the host controller cores to USB ports.

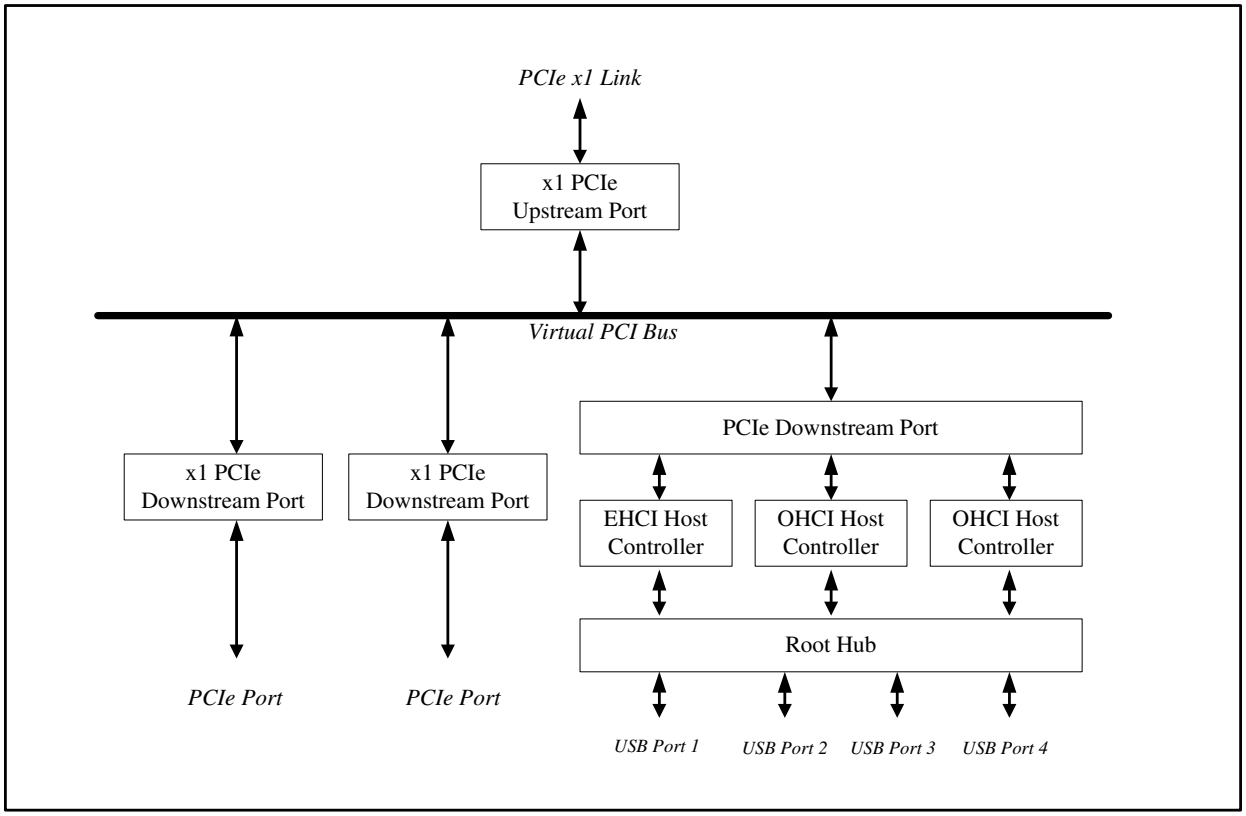

Figure 2-1 PI7C9X442SL Topology

3 PIN DEFINITION

3.1 SIGNAL TYPES

TYPE OF SIGNAL	DESCRIPTION
I	Input
O	Output
P	Power

"_L" in signal name indicates Active LOW signal

3.2 PCI EXPRESS INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
REFCLKP REFCLKN	51, 52	I	**Reference Clock Input Pairs:** Connect to external 100MHz differential clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
PERP [2:0]	63, 43, 37	I	**PCI Express Data Serial Input Pairs:** Differential data receive signals in three ports. Port 0 (Upstream Port): PERP[0] and PERN[0] Port 1 (Downstream Port): PERP[1] and PERN[1] Port 2 (Downstream Port): PERP[2] and PERN[2]
PERN [2:0]	62, 44, 38	I	
PETP [2:0]	59, 47, 41	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals in three ports. Port 0 (Upstream Port): PETP[0] and PETN[0] Port 1 (Downstream Port): PETP[1] and PETN[1] Port 2 (Downstream Port): PETP[2] and PETN[2]
PETN [2:0]	58, 48, 42	O	
PERST_L	104	I	**System Reset (Active LOW):** When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized.
DWNRST_L [2:1]	108, 107	O	**Downstream Device Reset (Active LOW):** It provides a reset signal to the devices connected to the downstream ports of the device. The signal is active when either PERST_L is asserted or the device has just been plugged into the Switch. DWNRST_L [x] corresponds to Portx, where x= 1,2.
REXT	57	I	**External Reference Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry.
REXT_GND	56	I	**External Reference Resistor Ground:** Connect to an external resistor to REXT.

3.3 USB INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
DP [4:1]	85, 93, 117, 124	I/O	**USB D+ Signal:** USB D+ analog signal covering HS/FS/LS. DP [x] is correspondent to Portx, where x=1,2,3,4.
DM [4:1]	84, 92, 116, 123	I/O	**USB D- Signal:** USB D- analog signal covering HS/FS/LS. DP [x] is correspondent to Portx, where x=1,2,3,4.
OCI [4:1]	7, 6, 5, 4	I	**Over Current Input (Active LOW):** These signals are asserted low to indicate that an over-current condition has occurred. OCI [x] is correspondent to Portx, where x=1,2,3,4.
POE [4:1]	13, 12, 11, 10	O	**Power Output Enable (Active LOW):** Power supply control output for USB Root Hub Port. When these signals are asserted low, they enable an external power switch to turn on the power supply. POE [x] is correspondent to Portx, where x=1,2,3,4.

NAME	PIN	TYPE	DESCRIPTION
RREF[4:1]	87, 95, 119, 126	I/O	**External Resistor Connection for Current Reference:** This analog signal is the connection to the external resistor. It sets the reference current. No external capacitor should be connected. The recommended value for the resistor is 6.04 kohm and accuracy of +/- 1%.
XI	102	I	**Crystal Oscillator Input:** A 12MHz crystal oscillator is required.
XO	103	O	**Crystal Oscillator Output**
PME_L	113	O	**Power Management Event (Low Active):** This signal is asserted whenever the USB power state is resumed to Operational State from Suspend State.
LEG_EMU_EN	20	O	**OHCI Legacy Emulation Enable:** This signal indicates that Legacy emulation support is enabled for the OHCI controller, and the application can read or write to I/O ports 60h/64h when I/O access for the OHCI controller is enabled. See section 5.2.1.1 for details of the Legacy Mode.
SMI_O	14	O	**System Management Interrupt:** This signal is used to indicate that an interrupt condition has occurred. The signal is used only when OHCI Legacy support is enabled. See section 5.2.1.1 for details of the Legacy Mode.
IO_HIT_I	3	I	**Application I/O Hit:** This signal indicates a PCI I/O cycle strobe. See section 5.2.1.1 for details of the Legacy Mode.
IRQ1_I	16	I	**External Interrupt 1:** This external keyboard controller interrupt 1 causes an emulation interrupt. See section 5.2.1.1 for details of the Legacy Mode.
IRQ1_O	18	O	**OHCI Legacy IRQ1:** This signal is asserted when an emulation interrupt condition exists and OutputFull, IRQEn, and AuxOutputFull are asserted. See section 5.2.1.1 for details of the Legacy Mode.
IRQ12_I	17	I	**External Interrupt 12:** This external keyboard controller interrupt 12 causes an emulation interrupt. See section 5.2.1.1 for details of the Legacy Mode.
IRQ12_O	19	O	**OHCI Legacy IRQ12:** This signal is asserted when an emulation interrupt condition exists, OutputFull and IRQEn are asserted, and AuxOutputFull is de-asserted. See section 5.2.1.1 for details of the Legacy Mode.

3.4 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN	TYPE	DESCRIPTION
TCK	26	I	**Test Clock:** TCK is the test clock to synchronize the state information and data during boundary scan operation. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	27	I	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.
TDO	25	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	28	I	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the Test Access Port. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TRST_L	29	I	**Test Reset (Active LOW):** TRST_L is the test reset to initialize the Test Access Port (TAP) controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.

3.5 MISCELLANEOUS SIGNALS

NAME	PIN	TYPE	DESCRIPTION
EECLK	99	O	**EEPROM Clock:** Clock signal to the EEPROM interface.
EEPD	98	I/O	**EEPROM Data:** Bi-directional serial data interface to and from the EEPROM. The pin is set to 1 by default.
SMBCLK	21	I	**SMBus Clock:** System management Bus Clock.
SMBDATA	64	I/O	**SMBus Data:** Bi-Directional System Management Bus Data.
SCAN_EN	15	I/O	**Full-Scan Enable Control:** For normal operation, SCAN_EN is an output with a value of "0". SCAN_EN becomes an input during manufacturing testing.
PRSNT [2:1]	78, 2	I	**Present:** When asserted low, it represents the device is present in the slot of downstream ports. Otherwise, it represents the absence of the device. PRSNT [x] is correspondent to Port x, where x=1,2.
SLOTCLK	66	I	**Slot Clock Configuration:** It determines if the downstream component uses the same physical reference clock that the platform provides on the connector. When SLOTCLK is high, the platform reference clock is employed. By default, all downstream ports use the same physical reference clock provided by platform.
SLOT_IMP[2:1]	80, 79	I	**Slot Implemented:** These signals are asserted to indicate that the downstream ports are connected to slots. SLOT_IMP[x] corresponds to Portx, where x= 1,2. When SLOT_IMP[x] is asserted, the Portx is connected to slot. By default, downstream ports are implemented with slots, and SLOT_IMP[2:1] are asserted.
GPIO[7:0]	76, 75, 74, 73, 72, 71, 70, 69	I/O	**General Purpose input and output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.
MAIN_DETECT	24	I	**Main Power Detect:** MAIN_DETECT should be tied to the Aux Power of the system through a 4.7K ohm pull-up resistor if the USB remote wakeup function is to be supported. Otherwise, this signal should be tied to the Main Power of the system through a 4.7K ohm pull-up resistor.
TEST1/3/4/5	1, 65, 77, 114	I	**Test Pins:** For testing purposes only. TEST1 and TEST4 should be tied to ground, and TEST3 and TEST5 should be tied to high for normal operation. The suggested value for the pull-up and pull-down resistor is 5.1K.
NC	30, 31, 32, 55, 88		**Not Connected:** These pins can be left floating.

3.6 POWER PINS

NAME	PIN	TYPE	DESCRIPTION
VDDC	22, 35, 81, 100, 109, 111	P	**VDDC Supply (1.0V):** Used as digital core power pins.
VDDR	8, 33, 67, 105, 112	P	**VDDR Supply (3.3V):** Used as digital I/O power pins.
VDDA	83, 90, 91, 97, 115, 121, 122, 128	P	**VDDA Supply (3.3V):** Used as USB analog power pins.
AVDD	40, 46, 49, 60,	P	**AVDD Supply (1.0V):** Used as PCI Express analog power pins.
AVDDH	54	P	**AVDDH Supply (3.3V):** Used as PCI Express analog high voltage power pins.
VSS	9, 23, 34, 36, 39, 45, 50, 53, 61, 68, 82, 86, 89, 94, 96, 101, 106, 110, 118, 120, 125, 127, 129	P	**VSS Ground:** Used as ground pins. **GND:** The central thermal pad underneath the package should be connected to ground.

4 PIN ASSIGNMENTS

4.1 PIN LIST of 128-PIN LQFP

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	TEST1	33	VDDR	65	TEST3	97	VDDA
2	PRSNT[1]	34	VSS	66	SLOTCLK	98	EEPD
3	IO_HIT_I	35	VDDC	67	VDDR	99	EECLK
4	OCI[1]	36	VSS	68	VSS	100	VDDC
5	OCI[2]	37	PERP[0]	69	GPIO[0]	101	VSS
6	OCI[3]	38	PERN[0]	70	GPIO[1]	102	XI
7	OCI[4]	39	VSS	71	GPIO[2]	103	XO
8	VDDR	40	AVDD	72	GPIO[3]	104	PERST_L
9	VSS	41	PETP[0]	73	GPIO[4]	105	VDDR
10	POE[1]	42	PETN[0]	74	GPIO[5]	106	VSS
11	POE[2]	43	PERP[1]	75	GPIO[6]	107	DWNRST_L[1]
12	POE[3]	44	PERN[1]	76	GPIO[7]	108	DWNRST_L[2]
13	POE[4]	45	VSS	77	TEST4	109	VDDC
14	SMI_O	46	AVDD	78	PRSNT[2]	110	VSS
15	SCAN_EN	47	PETP[1]	79	SLOT_IMP[1]	111	VDDC
16	IRQ1_I	48	PETN[1]	80	SLOT_IMP[2]	112	VDDR
17	IRQ12_I	49	AVDD	81	VDDC	113	PME_L
18	IRQ1_O	50	VSS	82	VSS	114	TEST5
19	IRQ12_O	51	REFCLKP	83	VDDA	115	VDDA
20	LEG_EMU_EN	52	REFCLKN	84	DM[4]	116	DM[2]
21	SMBCLK	53	VSS	85	DP[4]	117	DP[2]
22	VDDC	54	AVDDH	86	VSS	118	VSS
23	VSS	55	NC	87	RREF[4]	119	RREF[2]
24	MAIN_DETECT	56	REXT_GND	88	NC	120	VSS
25	TDO	57	REXT	89	VSS	121	VDDA
26	TCK	58	PETN[2]	90	VDDA	122	VDDA
27	TMS	59	PETP[2]	91	VDDA	123	DM[1]
28	TDI	60	AVDD	92	DM[3]	124	DP[1]
29	TRST_L	61	VSS	93	DP[3]	125	VSS
30	NC	62	PERN[2]	94	VSS	126	RREF[1]
31	NC	63	PERP[2]	95	RREF[3]	127	VSS
32	NC	64	SMBDATA	96	VSS	128	VDDA
						129	E_PAD

5 FUNCTIONAL DESCRIPTION

The multi-functional Swidge (PCI Express Packet Switch/PCI Express-to-USB Bridge) device contains multiple virtual PCI-to-PCI Bridges (VPPB) connected by a virtual PCI bus and USB Host Controllers (OHCI and EHCI) connected to the secondary PCI bus at one of VPPBs. Each one of the VPPBs encompasses complete PCIe architecture with the physical, data link, and transaction layers, except the one connected to the USB host controllers. One VPPB represents a single PCIe Port, which handles the transmission and reception of PCIe packets. The USB Host Controller is able to handle operational registers and descriptor link list, which provide a communication channel for Host Controller Driver (HCD) to initiate USB packet transactions to and from USB devices.

The operation of the PCIe packet switch function performs in the following steps. The packets entering the Switch via one of the VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer.

The operation of the PCIe to USB bridging functions are depicted as follows. The HCD first prepares the data structure of the USB commands or data. Then, the host controllers are notified to fetch the commands or data, which are eventually converted from PCIe into USB packet format. Depending on the direction of transfer, the host controller moves and converts the packet to/from USB devices. When the transfer is complete, an interrupt message will notify the HCD to process the data stored in the system memory the descriptor points to.

5.1 PCI EXPRESS PACKET SWITCH FUNCTIONALITIES

5.1.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the **P**HY **I**nterface for **P**CI **E**xpress Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. In addition, a pair of PRBS generator and checker is included for PHY built-in self test. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

[1] Multiple lanes could share the PLL.

5.1.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the Physical Layer Control Register 2 (offset BCh, bit[6:4]) as listed in Table 5-1.

Table 5-1 Receiver Detection Threshold Settings

Receiver Detection Threshold	Threshold
000	1.0 us
001	2.0 us
010	4.0 us (Recommended)
011	5.0 us
100	7.0 us
101	Reserved
110	Reserved
111	Reserved

5.1.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the Physical Layer Control Register 2 (Offset BCh, bit[22:21]) as listed in Table 5-2, and can be configured on a per-port basis via EEPROM settings.

Table 5-2 Receiver Signal Detect Threshold

Receiver Signal Detect	Min (mV ppd)	Max (mV ppd)
00	50	150
01 (Recommended)	65	175
10	75	200
11	120	240

5.1.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the Physical Layer Control Register 2 (Offset BCh, bit[25:22]). There are 16 possible settings. It is recommended that customers determine the optimal equalization settings based on their environment to and their application.

5.1.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the Physical Layer Control Register 2 (offset BCh, Bit[30]) is used for the selection of full swing signaling or half swing signaling.

Table 5-3 Transmitter Swing Settings

Transmitter Swing	Mode	De-emphasis
0	Full Voltage Swing	Implemented
1	Half Voltage Swing	Not implemented

5.1.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the Physical Layer Control Register 0 (offset B4h) and one of the Drive De-Emphasis Base Level fields in the Physical Layer Control Register 1 (offset B8h) are active for configuration of the amplitude and de-emphasis.

In addition, optional offset values can be added to the drive amplitude and drive de-emphasis on a per-port basis via EEPROM settings (EEPROM offset 70h, bit[3:0]). The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.

The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 5-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

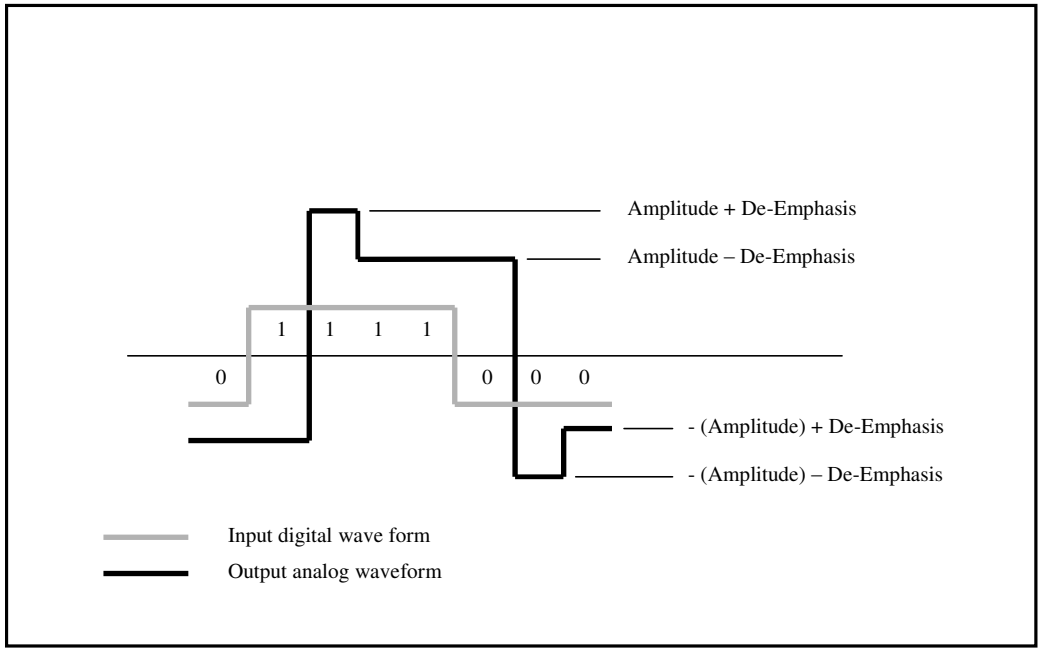

Figure 5-1 Driver Output Waveform

5.1.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the Physical Control Register 0 (offset B4h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-4 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 5-5

Table 5-4 Drive Amplitude Base Level Registers

Active Register	De-Emphasis Condition	Swing Condition
Drive Amplitude Level (3P5 Nom)	-3.5 db	Full

Table 5-5 Drive Amplitude Base Level Settings

Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)
00000	0	00111	175	01110	350
00001	25	01000	200	01111	375
00010	50	01001	225	10000	400
00011	75	01010	250	10001	425
00100	100	01011	275	10010	450
00101	125	01100	300	10011	475
00110	150	01101	325	Others	Reserved

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.

5.1.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the Physical Control Register 1 (Offset B8h, bit[20:16]) listed in Table 5-6 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 5-7

Table 5-6 Drive De-Emphasis Base Level Register

Register	De-Emphasis Condition
Drive De-Emphasis Level	-3.5 db

Table 5-7 Drive De-Emphasis Base Level Settings

Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)
00000	0.0	01011	68.75	10110	137.5
00001	6.25	01100	75.0	10111	143.75
00010	12.5	01101	81.25	11000	150.0
00011	18.75	01110	87.5	11001	156.25
00100	25.0	01111	93.75	11010	162.5
00101	31.25	10000	100.0	11011	168.75
00110	37.5	10001	106.25	11100	175.0
00111	43.75	10010	112.5	11101	181.25
01000	50.0	10011	118.75	11110	187.5
01001	56.25	10100	125.0	11111	194.75
01010	62.5	10101	131.25	-	-

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.

5.1.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the Physical Layer Control Register 2 (Offset BCh, bit[3:0]).

5.1.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes deskew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

5.1.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping, and it validates the correctness of the transaction type and format. If the TLP is found to contain illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

5.1.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet can not be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

5.1.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that all the traffic classes are mapped to VC0, since only VC0 is available on the Switch. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the VC0 queues.

5.1.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD.

5.1.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers.

5.1.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue.

5.1.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data.

5.1.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there is no 4-DW completion headers.

5.1.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue.

5.1.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 5-4 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels.

Table 5-8 Summary of PCI Express Ordering Rules

Row Pass Column	Posted Request	Read Request	Non-posted Write Request	Read Completion	Non-posted Write Completion
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older Bridges that do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue.

5.1.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which input traffic to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC

channel. Each port has port arbitration circuitries for traffic handling in VC0. At upstream port, in addition to the traffic from inter-port, the intra-port packet such as configurations completion would also join the arbitration loop to get the service in Virtual Channel 0.

5.1.9 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this switch, each port has separate queues for different traffic types and the credits are on the fly sent to data link layer, which compares the current available credits with the monitored one and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent from link entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. It would broadcast them to all the other ingress ports for gating the packet transmission.

5.1.10 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They are to construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packet when the local resource (i.e. configuration register) is accessed and regenerate the message that terminated at receiver to RC if acts as an upstream port.