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PI7C9X7954

PCI Express® Quad UART

Datasheet
Revision 2
October 2017

A Product Line of
Diodes Incorporated

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REVISION HISTORY

Date	Revision Number	Description
10/31/07	0.1	Preliminary Datasheet Fixed the diagrams Corrected Section 4.2 Pin Description (RREF, GPIO[7]) Updated Section 6 PCI Express Registers(6.2.42 [3], 6.2.36 UART Driver Setting, 6.2.41 GPIO Control Register) Revised Section 7.1 Registers in I/O Mode Updated Section 11 Ordering Info
12/20/2007	0.2	Updated Section 4 Pin Assignment (description for shared pins added, MODE_SEL changed to DRIVER_SEL) Updated Section 6 PCI Express Register Description Updated Section 7 UART Register Description Updated Section 8 EEPROM Interface
04/22/08	0.3	Updated Section 1 Features (Clock prescaler, Data frame size, Power Dissipation) Corrected Section 3 General Description Updated Section 4 Pin Assignment (description for shared pins added, MODE_SEL changed to DRIVER_SEL, VAUX changed to VDDCAUX, WAKEUP_L, CLKINP, CLKINN) Added 5.2.4 Mode Selection, 5.2.5 450/550 Mode, 5.2.6 Enhanced 550 Mode, 5.2.7 Enhanced 950 Mode Corrected 5.2.8 Transmit and Receive FIFOs, 5.2.9 Automated Flow Control Modified 5.2.12 Baud Rate Generation Updated Section 6 PCI Express Register Description (6.2.36, 6.2.42) Updated Format (6.2.20, 6.2.36, 6.2.54, 6.2.55, 6.2.57) Updated Section 7 UART Register Description (7.1.6 LCR Bit[5:0], 7.1.7 MCR Bit[5] and Bit[7], 7.1.9 MSR Bit[3:0], 7.2.6 LCR Bit[5:0], 7.2.7 MCR Bit[5] and Bit[7], 7.2.9 MSR Bit[3:0], 7.2.11 DLL, 7.2.12 DLH, 7.2.13 EFR, 7.2.18 ACR Bit[7:2], 7.2.23 CPRM) Updated Chapter 8.3 EEPROM Space Address Map And Description (00h, 0Ah, 40h) Added Section 9 Electrical Specification Corrected Section 9.2 DC Specification Updated Section 9.3 AC Specification Added Section 10 Clock Scheme
08/13/08	0.4	Updated Section 1 Features (added Industrial Temperature Range) Updated 9.1 Absolute Maximum Ratings: Ambient Temperature with power applied
11/25/08	1.0	Updated 7.1.13 Sample Clock Register and 7.2.27 Sample Clock Register Updated Chapter 12 Ordering Information Removed “Preliminary” and “Confidential” references
03/06/09	1.1	Corrected Figure 3-1 PI7C9X7954 Block Diagram (SYN_UART_CLK removed) Corrected Section 4.2.1 UART Interface (SYNCLK_IN_EN and SYN_UART_CLK removed) Corrected Figure 5-2 Internal Loopback in PI7C7954 Corrected Figure 5-3 Crystal Oscillator as the Clock Source (14.7456 MHz) Corrected Section 7.1.7 Modem Control Register (Bit[5]), 7.1.10 Special Function Register (Bit[4]), 7.2.7 Modem Control Register (Bit[5]), 7.2.10 Special Function Register (Bit[4]), 7.2.29 Receive FIFO Data Registers, 7.2.30 Transmit FIFO Data Register, 7.2.31
04/21/09	1.2	Updated Section 4 Pin Description
09/24/09	1.3	Updated Figure 5-3 Crystal Oscillator as the Clock Source Updated Section 6.2.24 Message Signaled Interrupt (MSI) Next Item Pointer 8Ch Added Section 6.2.25 Message Address Register – Offset 90h Added Section 6.2.26 Message Upper Address Register – Offset 94h Added Section 6.2.27 Message Data Register – Offset 98h
06/04/14	1.4	Updated Section 4.1 Pin List (SR_DO and SR_DI) Updated Section 4.2.5 EEPROM Interface (SR_DO and SR_DI) Created for IC Revision B Updated Section 12 Ordering Information Added Section 6.2.25 Message Control Register – OFFSET 8Ch
01/09/15	1.5	Updated Section 11 Package Information
05/11/15	1.6	Updated Table 5-2 Baud Rate Generator Setting Updated Section 7.2.23 Clock Prescale Register – Offset 14h
08/30/17	1.7	Updated Section 4.1.PIN LIST OF 128-PIN LQFP Updated Section 4.2.1 UART Interface Updated Table 9.1 Absolute Maximum Ratings Updated Table 9.2 DC Electrical Characteristics Updated Section 12 Ordering Information
10/06/17	2	Revision numbering system changed to whole number

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- x1 PCI Express link host interface
- Four high performance 950-class UARTs
- Compliant with PCI Express Base Specification 1.1
- Compliant with PCI Express CEM Specification 1.1
- Compliant with PCI Power Management 1.2
- Fully 16C550 software compatible UARTs
- 128-byte FIFO for each transmitter and receiver
- Baud rate up to 15 Mbps in asynchronous mode
- Flexible clock prescaler from 4 to 46
- Automated in-band flow control using programmable Xon/Xoff in both directions
- Automated out-of-band flow control using CTS#/RTS# and/or DSR#/DTR#
- Arbitrary trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-of-band flow control
- Global Interrupt Status and readable FIFO levels to facilitate implementation of efficient device drivers
- Detection of bad data in the receiver FIFO
- Data framing size including 5, 6, 7, 8 and 9 bits
- Hardware reconfiguration through Microwire compatible EEPROM
- Operations via I/O or memory mapping
- Dual power operation (1.8V for PCIe I/O and core, 3.3V for UART I/O)
- Power dissipation: 0.8 W typical in normal mode
- Industrial Temperature Range -40^{o} to 85^{o}
- 128-pin LQFP, Pb-free and 100% Green

2. APPLICATIONS

- Remote Access Servers
- Network / Storage Management
- Factory Automation and Process Control
- Instrumentation
- Multi-port RS-232/ RS-422/ RS-485 Cards
- Point-of-Sale Systems (PoS)
- Industrial PC (IPC)
- Industrial Control
- Gaming Machines
- Building Automation
- Embedded Systems

3. GENERAL DESCRIPTION

The PI7C9X7954 is a PCI Express Quad UART (Universal Asynchronous Receiver-Transmitters) I/O Bridge. It is specifically designed to meet the latest system requirements of high performance and lead (Pb) -free. The bridge can be used in a wide range of applications such as Remote Access Servers, Automation, Process Control, Instrumentation, POS, ATM and Multi-port RS232/ RS422/ RS485 Cards. The PI7C9X7954 provides one x1 PCIe (dual simplex 2.5 Gbps) uplink port, and it is fully compliant with PCI express 1.1 and PCI power management 1.2 specifications. The bridge supports four high performance UARTs, each of which supports Baud rate up to 15 Mbps in asynchronous mode. The UARTs support in-band and out-band auto flow control, arbitrary trigger level, I/O mapping and memory mapping. The PI7C9X7954 is fully software compatible with 16C550 type device drivers and can be configured to fit the requirements of RS232, RS422 and RS485 applications. The EEPROM interface is provided for system implementation convenience. Some registers can be pre-programmed via hardware pin settings to facilitate system initialization. For programming flexibility, all of the default configuration registers can be overwritten by EEPROM data, such as sub-vendor and sub-system ID.

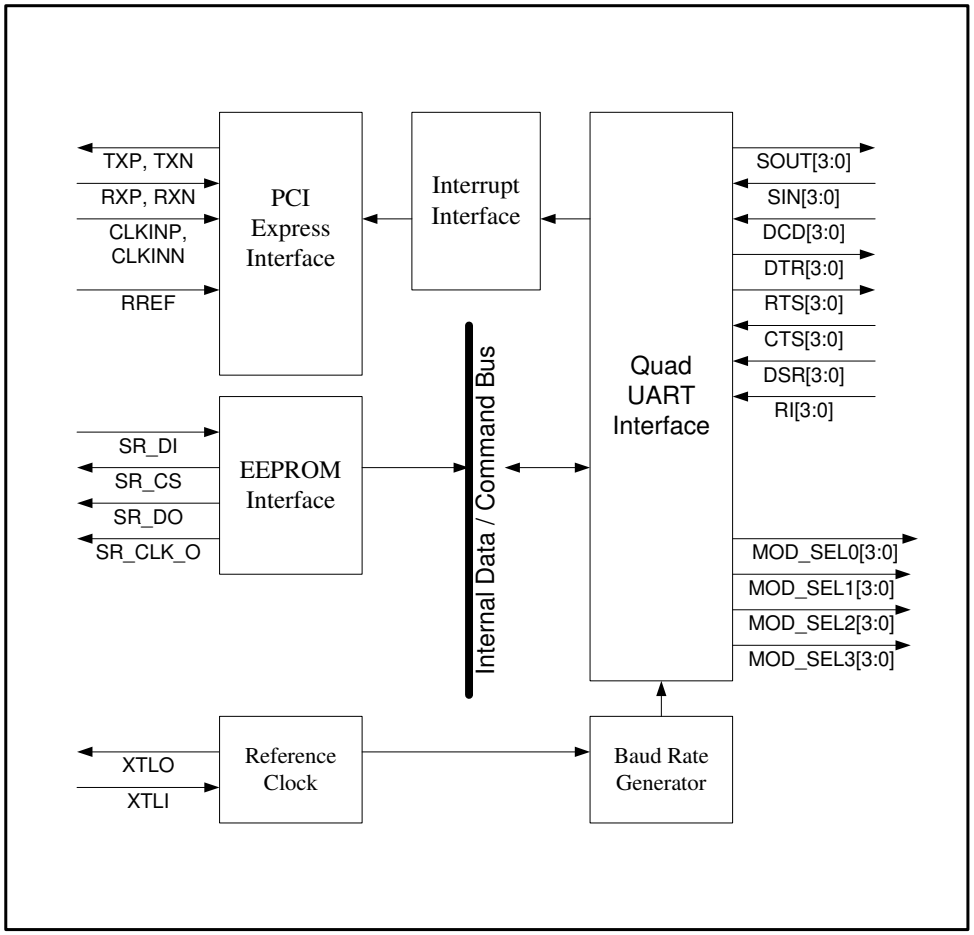

Figure 3-1 PI7C9X7954 Block Diagram

4. PIN ASSIGNMENT

4.1. PIN LIST OF 128-PIN LQFP

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VDDR	33	VDDC	65	DRIVER_SEL3[0]	97	NC
2	VDDR	34	VDDCAUX	66	DRIVER_SEL3[1]	98	VDDC
3	VSS	35	VSS	67	DRIVER_SEL3[2]	99	VDDC
4	VSS	36	PERST_L	68	DRIVER_SEL3[3]	100	VSS
5	SCAN_EN	37	TEST	69	VDDC	101	VSS
6	XTLI	38	GPIO[0]/DEQ[1]	70	VSS	102	NC
7	XTLO	39	GPIO[1]/DEQ[2]	71	SOUT[0]	103	NC
8	SR_CLK_O	40	VDDR	72	RTS[0]/EEPROM_BYPASS	104	NC
9	SR_DI	41	VDDR	73	DTR[0]/TEST2	105	NC
10	SR_DO	42	VSS	74	SIN[0]	106	JTAG_TDI
11	SR_CS	43	GPIO[2]/DEQ[3]	75	CTS[0]	107	JTAG_TMS
12	VDDC	44	GPIO[3]/TXTERMADJ[0]	76	DSR[0]	108	JTAG_TCK
13	VSS	45	GPIO[4]/TXTERMADJ[1]	77	RI[0]	109	JTAG_TDO
14	WAKEUP_L	46	GPIO[5]/RXTERMADJ[0]	78	DCD[0]	110	JTAG_TRST_L
15	VSS	47	GPIO[6]/RXTERMADJ[1]	79	SOUT[1]/DEBUG_PIN	111	NC
16	CLKINP	48	GPIO[7]/SR_ORG	80	RTS[1]/UART_TEST_MODE	112	NC
17	VDDA	49	DRIVER_SEL0[0]/HI_DRV	81	DTR[1]	113	NC
18	CLKINN	50	DRIVER_SEL0[1]/PHY_TM	82	SIN[1]	114	NC
19	VSS	51	DRIVER_SEL0[2]/LO_DRV	83	CTS[1]	115	VDDR
20	VDDC	52	DRIVER_SEL0[3]/DTX[0]	84	DSR[1]	116	VDDR
21	VTT	53	VDDC	85	RI[1]	117	VSS
22	TXN	54	VSS	86	DCD[1]	118	VSS
23	TXP	55	DRIVER_SEL1[0]/DTX[1]	87	SOUT[2]	119	SOUT[3]
24	VSS	56	DRIVER_SEL1[1]/DTX[2]	88	RTS[2]	120	RTS[3]
25	VDDCAUX	57	DRIVER_SEL1[2]/DTX[3]	89	DTR[2]	121	DTR[3]
26	RXP	58	DRIVER_SEL1[3]/DEQ[0]	90	SIN[2]	122	SIN[3]
27	VSS	59	DRIVER_SEL2[0]	91	CTS[2]	123	CTS[3]
28	RXN	60	DRIVER_SEL2[1]	92	DSR[2]	124	DSR[3]
29	RREF	61	DRIVER_SEL2[2]	93	RI[2]	125	RI[3]
30	VDDA	62	DRIVER_SEL2[3]	94	DCD[2]	126	DCD[3]
31	VSS	63	VDDR	95	VDDR	127	VDDC
32	VDDA	64	VSS	96	VSS	128	VDDC

Table 4-1 Pin-List of 128-Pin LQFP

4.2. PIN DESCRIPTION

4.2.1. UART INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
119, 87, *79, 71	SOUT [3:0]	O	**UART Serial Data Outputs:** The output pins transmit serial data packets with start and end bits. SOUT[0] and SOUT[1] are output signals with weak internal pull-down resistors. **DEBUG_PIN:** During system initialization, SOUT[1] acts as the DEBUG_IN pin, and it is used to internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped.
122, 90, 82, 74	SIN [3:0]	I	**UART Serial Data Inputs:** The input pins receive serial data packets with start and end bits. The pins are idle high.
126, 94, 86, 78	DCD [3:0]	I	**Modem Data-Carrier-Detect Input and General Purpose Input (Active Low)**
121, 89, 81, *73	DTR [3:0]	O	**Modem Data-Terminal-Ready Output (Active LOW):** If automated DTR# flow control is enabled, the DTR# pin is asserted and deasserted if the receiver FIFO reaches or falls below the programmed thresholds, respectively. DTR[0] and DTR[1] are output signals with weak internal pull-down resistors. **TEST2:** During system initialization, DTR[0] acts as the TEST pin, and it is used for internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped.
120, 88, *80, *72	RTS [3:0]	O	**Modem Request-To-Send Output (Active LOW):** If automated RTS# flow control is enabled, the RTS# pin is deasserted and reasserted whenever the receiver FIFO reaches or falls below the programmed thresholds, respectively. RTS[0] and RTS[1] are output signals with weak internal pull-down resistors. **UART_TEST_MODE:** During system initialization, RTS[1] acts as the UART_TEST_MODE pin, and it is used for internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped. **EEPROM Bypass:** During system initialization, RTS[0] acts as the EEPROM Bypass pin, and it is used to bypass EEPROM pre-loading. The pin is active-high. When it is asserted at start-up, the EEPROM pre-loading is bypassed, and no configuration data is loaded from the EEPRPOM. Otherwise, configuration data is loaded from the EEPROM.
123, 91, 83, 75	CTS [3:0]	I	**Modem Clear-To-Send Input (Active LOW):** If automated CTS# flow control is enabled, upon deassertion of the CTS# pin, the transmitter will complete the current character and enter the idle mode until the CTS# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the CTS# pin.
124, 92, 84, 76	DSR [3:0]	I	**Modem Data-Set-Ready Input (Active LOW):** If automated DSR# flow control is enabled, upon deassertion of the DSR# pin, the transmitter will complete the current character and enter the idle mode until the DSR# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the DSR# pin.
125, 93, 85, 77	RI [3:0]	I	**Modem Ring-Indicator Input (Active LOW)**
7	XTLO	O	**Crystal Oscillator Output**
6	XTLI	I	**Crystal Oscillator Input Or External Clock Pin:** The maximum frequency supported by this device is 60MHz.

PIN NO.	NAME	TYPE	DESCRIPTION
*52, *51, *50, *49	DRIVER_SEL0 [3:0]	O	**DRIVER_SEL0:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 0. DRIVER_SEL0 [3:0] are output signals with weak internal pull-down resistors. **Driver Current Level Control (DTX[0]):** During system initialization, DRIVER_SEL0[3] acts as the DTX[0] pin, and it is used to control the driver current level. By default, it is set to '0' without pin strapped. **Low Driver Control (LO_DRV):** During system initialization, DRIVER_SEL0[2] acts as the LO_DRV pin, and it is used to decrease the nominal value of the PCI Express lane's driver current level. By default, it is set to '0' without pin strapped. **PHY_TM:** During system initialization, DRIVER_SEL0[1] acts as the PHY_TM pin, and it is used for internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped. **High Driver Control (HI_DRV):** During system initialization, DRIVER_SEL0[0] acts as the HI_DRV pin, and it is used to increase the nominal value of the PCI Express lane's driver current level. By default, it is set '0' without pin strapped.
*58, *57, *56, *55	DRIVER_SEL1 [3:0]	O	**DRIVER_SEL1:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 1. DRIVER_SEL1 [3:0] are output signals with weak internal pull-down resistors. **Driver Equalization Level Control (DEQ[0]):** During system initialization, DRIVER_SEL1[3] acts as the DEQ[0] pin, and it is used to control the driver current level. By default, it is set to '0' without pin strapped. **Driver Current Level Control (DTX[3:1]):** During system initialization, DRIVER_SEL1[2:0] acts as the DTX[3:1] pins, and they are used to control the driver current level. By default, they are set to '000' without pin strapped.
62, 61, 60, 59	DRIVER_SEL2 [3:0]	O	**DRIVER_SEL2:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 2. DRIVER_SEL2[3] is an output signal with a weak internal pull-up resistor, and other DRIVER_SEL2 signals are output signals with internal pull-down resistors.
68, 67, 66, 65	DRIVER_SEL3 [3:0]	O	**DRIVER_SEL3:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 3. DRIVER_SEL3 [3:0] are output signals with weak internal pull-up resistors.

4.2.2. PCI EXPRESS INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
23, 22	TXP, TXN	O	**PCI Express Serial Output Signal:** Differential PCI Express output signals.
26, 28	RXP, RXN	I	**PCI Express Serial Input Signal:** Differential PCI Express input signals.
16, 18	CLKINP, CLKINN	I	**Reference Input Clock:** Connects to external 100MHz differential clock The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
29	RREF	I	**Reference Resistor:** To accurately set internal bias references, a precision resistor must be connected between **Rref** and **Vss**. The resistor should have a nominal value of 2.1 KΩ and accuracy of +/- 1%

4.2.3. SYSTEM INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
36	PEREST_L	I	**System Reset Input**
*48, *47, *46, *45, *44, *43, *39, *38	GPIO [7:0]	I/O	**General-Purpose Bi-Direction Signals / SR_ORG:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register. GPIO[2] is a bi-directional signal with a weak internal pull-up resistor, and other GPIO pins are bi-directional signals with weak internal pull-down resistors. **EEPROM Organization Pin (SR_ORG):** During system initialization, GPIO[7] acts as the SR_ORG pin, and it is used to select the organization structure of the EEPROM. The pin is active-high. When it is asserted at start-up, the EEPROM configuration data is organized in 16-bit structure. Otherwise, 8-bit structure is used. **Receiver Termination Adjustment (RXTERMADJ[1:0]):** During system initialization, GPIO[6:5] acts as the RXTERMADJ[1:0] pins, and they are used to adjust the receive termination resistor value. By default, they are set to '00' without pin strapped. **Transmit Termination Adjustment (TXTERMADJ[1:0]):** During system initialization, GPIO[4:3] acts as the TXTERMADJ[1:0] pins, and they are used to adjust the transmit termination resistor value. By default, they are set to "00" without pin strapped. **Driver Equalization Level Control (DEQ[3:1]):** During system initialization, GPIO[2:0] acts as the DEQ[3:1] pins, and they are used to control the driver current level. By default, they are set to '100' without pin strapped.
14	WAKEUP_L	O	**Wakeup Signal (Active LOW):** When the Ring Indicator is received on UART channel 0 in L2 state, the WAKEUP_L is asserted. WAKEUP_L is an output signal with a weak internal pull-down resistor.

4.2.4. TEST SIGNALS

PIN NO.	NAME	TYPE	DESCRIPTION
106	JTG_TDI	I	**Test Data Input:** When SCAN_EN is high, the pin is used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. JTG_TDI is an input signal with a weak internal pull-up resistor.
109	JTG_TDO	O	**Test Data Output:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream
107	JTG_TMS	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. JTG_TMS is an input signal with a weak internal pull-up resistor.
108	JTG_TCK	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan.
110	JTG_TRST_L	I	**Test Reset:** Active LOW signal to reset the TAP controller into an initialized state. JTG_TRST_L is an input signal with a weak internal pull-up resistor.
5	SCAN_EN	I	**Scan Test Enable Pin:** SCAN_EN is an input signal with a weak internal pull-up resistor.
37	TEST	I	This input signal should be tied to ground during normal operation.
97, 102, 103, 104, 105, 111, 112, 113, 114	NC		These pins can be left floating.

4.2.5. EEPROM INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
11	SR_CS	O	**EEPROM Chip Select:** SR_CS is an output signal with a weak internal pull-up resistor.
10	SR_DO	O	**EEPROM Data Output:** Serial data output interface to the EEPROM. SR_DO is an output signal with a weak internal pull-up resistor.
9	SR_DI	I	**EEPROM Data Input:** Serial data input interface to the EEPROM. SR_DI is an input signal with a weak internal pull-up resistor.
8	SR_CLK_O	O	**EEPROM Clock Output.**

4.2.6. POWER PINS

PIN NO.	NAME	TYPE	DESCRIPTION
12, 20, 33, 53, 69, 98, 99, 127, 128	VDDC	P	**1.8 V Power Pin:** Used as digital core power pins.
17, 30, 32,	VDDA	P	**1.8 V Power Pin:** Used as analog core power pins.
1, 2, 40, 41, 63, 95, 115, 116	VDDR	P	**3.3 V Power Pin:** Used as digital I/O power pins.
25, 34	VDDCAUX	P	**1.8 V Power Pin:** Used as auxiliary power pins.
21	VTT	P	**1.8V Termination Voltage:** Provides driver termination voltage at transmitter. Should be given the same consideration as VDDCAUX.
3, 4, 13, 15, 19, 24, 27, 31, 35, 42, 54, 64, 70, 96, 100, 101, 117, 118	VSS	P	**Ground Pin:** Used as ground pins.

5. FUNCTIONAL DESCRIPTION

The PI7C9X7954 is an integrated solution of four high-performance 16C550 UARTs with one x1 PCI Express host interface. The PCI Express host interface is compliant with the PCI Express Base Specification 1.1, PCI Express CEM Specification 1.1, and PCI Power Management 1.2. In addition, the chip is compliant with the Advanced Configuration Power Interface (ACPI) Specification and the PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification Revision 1.0. The x1 PCI Express host interface supports up to 2.5 Gbps bandwidth and complete PCI Express configuration register set. The PCI Express interface allows direct access to the configuration and status registers of the UART channels.

The UARTs in the PI7C9X7954 support the complete register set of the 16C550-type devices. The UARTs support Baud Rates up to 15 Mbps in asynchronous mode. Each UART channel has 128-byte deep transmit and receive FIFOs. The high-speed FIFOs reduce CPU utilization and improve data throughput. In addition, the UARTs support enhanced features including automated in-band flow control using programmable Xon/ Xoff in both directions, automated out-band flow control using CTS#/ RTS# and/or DRS#/ DTR#, and arbitrary transmit and receive trigger levels.

5.1. CONFIGURATION SPACE

The PI7C9X7954 has two sets of registers to allow various configuration and status monitoring functions. The PCI Express Configuration Space Registers enable the plug-and-play and auto-configuration when the device is connected to the PCI Express system bus. The UART configuration and internal registers enable the general UART operation functions, status control and monitoring.

5.1.1. PCI Express Configuration Space

The PI7C9X7954 is recognized as a PCI Express endpoint, which is mapped into the configuration space as a single logical device. Each endpoint in the system, including the PI7C9X7954, is part of a Hierarchy Domains originated by the Root Complex, which is a tree with a Root Port at its head in the configuration space. The device configuration registers are implemented for the user to access the functionalities provided by the PCI Express specification. The specification utilizes a flat memory-mapped configuration space to access device configuration registers.

All PCI Express endpoints facilitate a PCI-compatible configuration space to maintain compatibility with PCI software configuration mechanism. PCI Local Bus Specification, Revision 3.0 allocates 256 bytes per device function. PCI Express Base Specification 1.1 extends the configuration space to 4096 bytes to allow enhanced features. The first 256 bytes of the PCI Express Configuration Space are PCI 3.0 compatible region, and the rest of the 4096 bytes are PCI Express Configuration Space. The user can access the PCI 3.0 compatible region either by conventional PCI 3.0 configuration addresses or by the PCI Express memory-mapping addresses. These two types of accesses to the PCI 3.0 compatible region have identical results. The enhanced features in the PCI Express configuration space can only be accessed by PCI Express memory-mapping accesses.

5.1.2. UART Configuration Space

Through the UART registers, the user can control and monitor various functionalities of the UARTs on the PI7C9X7954 including FIFOs, interrupt status, line status, modem status and sample clock. Each of the UART's transmit and receive data FIFOs can be conveniently accessed by reading and writing the registers in the UART configuration space. These registers allow flexible programming capability and versatile device operations of the PI7C9X7954. Each UART is accessed through an 8-byte I/O blocks. The addresses of the UART blocks are offset by the base address referred by the Base Address Register (BAR). The value of the base address is loaded from the I/O or Memory Base Address defined in the PCI Express configuration

space.

The PI7C9X7954 also supports enhanced features such as Xon/Xoff, automatic flow control, Baud Rate prescaling and various status monitoring. These enhanced features are available through the memory address offset by the BAR in the PCI Express configuration space.

The basic features available in the registers in I/O mode are also available in the registers in memory-mapping mode. Accesses to these registers are equivalent in these two modes.

The UARTs on the PI7C9X7954 supports operations in 16C450, 16C550 and 16C950 modes. These modes of operation are selected by writing the SFR, FCR and EFR registers. The PI7C9X7954 is backward compatible with these modes of operation.

5.2. DEVICE OPERATION

The PI7C9X7954 is configured by the Root Complex in the bootstrap process during system start-up. The Root Complex performs bus scans and recognizes the device by reading vendor and device IDs. Upon successful device identification, the system then loads device-specific driver software and allocates I/O, memory and interrupt resources. The driver software allows the user to access the functions of the device by reading and writing the UART registers. The PCI Express interface incorporates convenient device operation and high system performance.

5.2.1. Configuration Access

The PI7C9X7954 accepts type 0 configuration read and write accesses defined in the PCI Express Base1.1 Specification. The first 256 bytes of the PCI Express configuration are compatible with PCI 3.0.

5.2.2. I/O Reads/Writes

The PCI Express interface of the PI7C9X7954 decodes incoming transaction packets. If the address is within the region assigned by the I/O Base Address Registers, the transaction is recognized as an I/O Read or Write.

5.2.3. Memory Reads/Writes

Similar to the I/O Read/Write, if the address of the transaction packet is within the memory range, a Memory Read/Write occurs.

5.2.4. Mode Selection

All of the internal UART channels in the I/O Bridge support the 16C450, 16C550, Enhanced 16C550, and Enhanced 950 UART Modes. The mode of the UART operation is selected by toggling the Special Function Register (SFR[5]) and Enhanced Function Register (EFR[4]). The FIFO depth of each mode and the mode selection is tabulated in the table below.

Table 5-1 Mode Selection

UART Mode	SFR[5]	EFR[4]	FIFO Size
450/550	X	0	1/16
Enhanced 550	0	1	128
Enhanced 950	1	1	128

5.2.5. 450/550 Mode

The 450 Mode is inherently supported when 550 Mode is selected. When in the 450 Mode, the FIFOs are in the "Byte Mode", which refers to the one-byte buffer in the Transmit Holding Register and the Receive Holding Register in each of the UART channels. When in the 550 Mode, the UARTs support an increased FIFO depth of 16.

When EFR[4] is set to "0", the SFR[5] is ignored, and the 450/550 Mode is selected.

5.2.6. Enhanced 550 Mode

Setting the SFR[5] to "0" and EFR[4] to "1" enables the Enhanced 550 Mode. The Enhanced 550 Mode further increases FIFO depth to 128.

5.2.7. Enhanced 950 Mode

128-deep FIFOs are supported in the Enhanced 950 Mode. When the Enhanced 950 Mode is enabled, the UART channels support additional features:

- Sleep mode
- Special character detection
- Automatic in-band flow control
- Automatic flow control using selectable arbitrary thresholds
- Readable status for automatic in-band and out-of-band flow control
- Flexible clock prescaler
- Programmable sample clock
- DSR/DTR automatic flow control

5.2.8. Transmit and Receive FIFOs

Each channel of the UARTs consists of 128 bytes of transmit FIFOs and 128 bytes of receive FIFOs, namely the Transmit Holding Registers (THR) and the Receive Holding Registers (RHR). The FIFOs provide storage space for the data before they can be transmitted or processed. The THR and RHR operate simultaneously to transmit and read data.

The transmitter reads data from the THR into the Transmit Shift Register (TSR) and removes the data from top of the THR. It then converts the data into serial format with start and stop bits and parity bits if required. If the transmitter completes transmitting the data in the TSR and the THR is empty, the transmitter is in the idle state. The data that arrive most recently are written to the bottom of the THR. If the THR is full, and the user attempts to write data to the THR, a data overrun occurs and the data is lost.

The receiver writes data to the bottom of the RHR when it finishes receiving and decoding the data bits. If the RHR is full when the receiver attempts to write data to it, a data overrun occurs. Any read operation to an empty RHR is invalid.

The empty and full status of the THR and RHR can be determined by reading the empty and full flags in the Line Status Register (LSR). When the transmitter and receiver are ready to transfer data to and from the FIFOs, interrupts are raised to signal this condition. Additionally, the user can use the Receive FIFO Data Counter (RFDC) and Transmit FIFO Data Counter (TFDC) registers to determine the number of items in each FIFO.

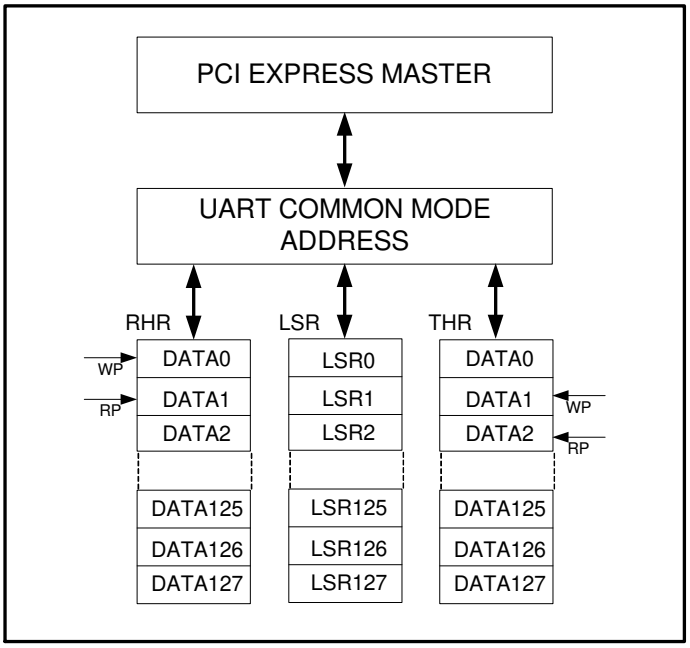

Figure 5-1 Transmit and Receive FIFOs

5.2.9. Automated Flow Control

The device uses automatic in-band flow control to prevent data-overrun to the local receive FIFO and remote receive FIFO. This feature works in conjunction with the special character detection. When an XOFF condition is detected, the UART transmitter will suspend any further data transmission after the current character transmission is completed. The transmitter will resume data-transmission as soon as an XON condition is detected. The automatic in-band feature is enabled by the Enhanced Function Register (EFR). EFR[1:0] enables the in-band receive flow control, and EFR[3:2] enables the in-band transmit flow control.

The out-of-band flow control utilizes RTS# and CTS# pins to suspend and resume the data transmission and to prevent data-overrun. An asserted CTS# pin signals the UART to suspend transmission due to a full remote receive FIFO. Upon detecting an asserted CTS# pin, the UART will complete the current character transmission and enters idle mode until the CTS# pin is deasserted.

The UART deasserts RTS# to signal the remote transmitter that the local receive FIFO reaches the programmed upper trigger level. When the local receive FIFO falls below the programmed lower trigger level, the RTS# is reasserted. The automatic out-of-band flow control is enabled by EFR[7:6].

5.2.10. Internal Loopback

The internal loopback capability of the UARTs is enabled by setting Modem Control Register bit-4 (MCR[4]) to 1. When the feature is enabled, the data from the output of the transmit shift register are looped back to the input of the receive shift register. This feature provides the users a way to perform system diagnostics by allowing the UART to receive the same data it is sending.

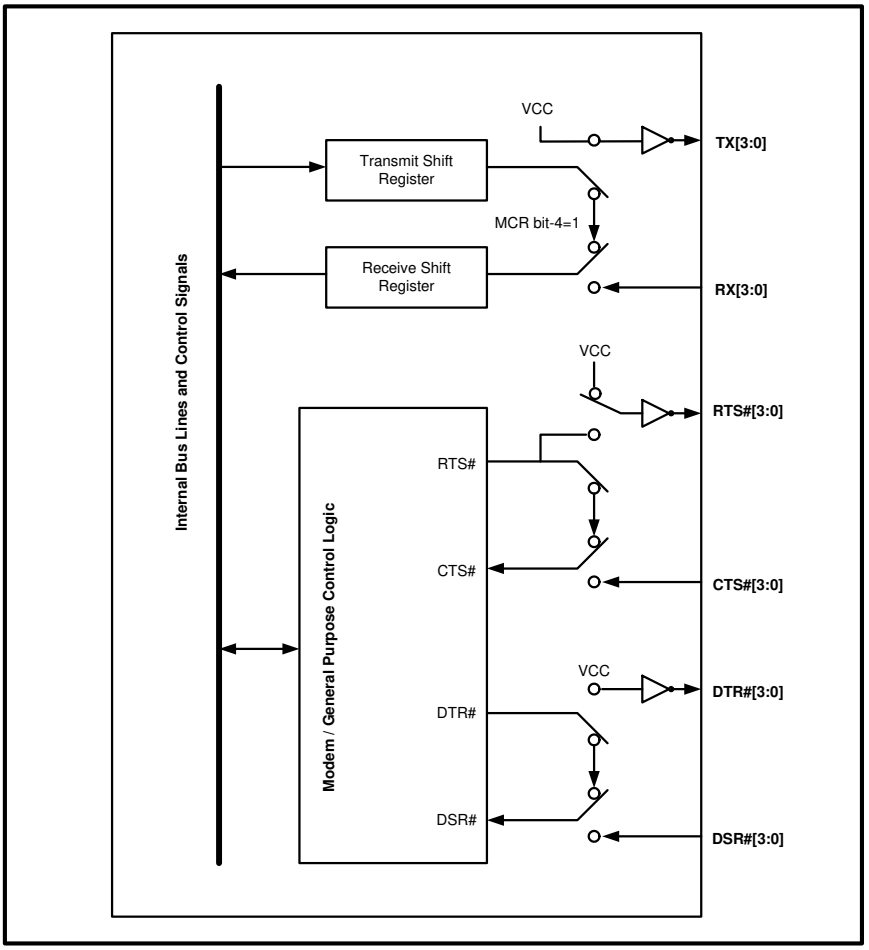

Figure 5-2 Internal Loopback in PI7C9X7954

5.2.11. Crystal Oscillator

The PI7C9X7954 uses a crystal oscillator or an external clock source to provide system clock to the Baud Rate Generator. When a clock source is used, the clock signal should be connected to the XTLI pin, and a 2K pull-up resistor should be connected to the XTLO pin.

When a crystal oscillator is used, the XTLI is the input and XTLO is the output, and the crystal should be connected in parallel with two capacitors.

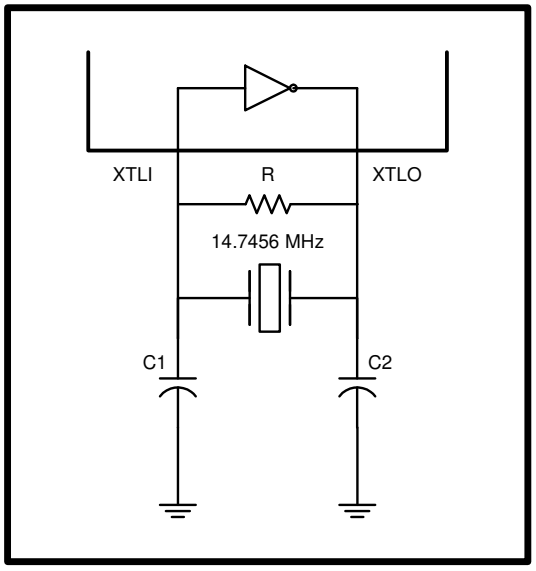

Figure 5-3 Crystal Oscillator as the Clock Source

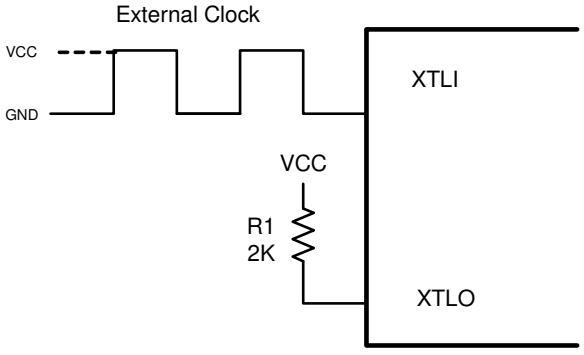

Figure 5-4 External Clock Source as the Clock Source

5.2.12. Baud Rate Generation

The built-in Baud Rate Generator (BRG) allows a wide range of input frequency and flexible Baud Rate generation. To obtain the desired Baud Rate, the user can set the Sample Clock Register (SCR), Divisor Latch Low Register (DLL), Divisor Latch High Register (DLH) and Clock Prescale Registers (CPRM and CPRN). The Baud Rate is generated according to the following equation:

$$BaudRate = \frac{InputFrequency}{Divisor * \Pr escaler}$$

The parameters in the equation above can be programmed by setting the "SCR", "DLL", "DLH", "CPRM" and "CPRN" registers according to the table below.

Table 5-2 Baud Rate Generator Setting

Setting	Description
Divisor	DLL + (256 * DLH)
Prescaler	$2^M * (SampleClock + N)$
SampleClock	$16 - SCR$, (SCR = '0h' to 'Ch')
M	CPRM, (CPRM = '01h' to '02h')
N	CPRN, (CPRN = '0h' to '7h')

To ensure the proper operation of the Baud Rate Generator, users should avoid setting the value '0' to Sample Clock, Divisor and Prescaler.

The following table lists some of the commonly used Baud Rates and the register settings that generate a specific Baud Rate. The examples assume an Input Clock frequency of 14.7456 Mhz. The SCR register is set to '0h', and the CPRM and CPRN registers are set to '1h' and '0h' respectively. In these examples, the Baud Rates can be generated by different combination of the DLH and DLL register values.

Table 5-3 Sample Baud Rate Setting

Baud Rate	DLH	DLL
1,200	3h	00h
2,400	1h	80h
4,800	0h	C0h
9,600	0h	60h
19,200	0h	30h
28,800	0h	20h
38,400	0h	18h
57,600	0h	10h
115,200	0h	08h
921,600	0h	01h

5.2.13. Power Management

The PI7C9X7954 supports the D0, D1, D2 and D3 power states. The device is compliant with PCI Power Management Specification Revision 1.2.

6. PCI EXPRESS REGISTER DESCRIPTION

6.1. REGISTER TYPES

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
WO	Write Only
RW	Read / Write
RWC	Read / Write 1 to Clear
RWCS	Sticky - Read Only / Write 1 to Clear
RWS	Sticky - Read / Write

6.2. CONFIGURATION REGISTERS

The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Master Latency Timer	Cache Line Size	0Ch
Base Address Register 0				10h
Base Address Register 1				14h
Reserved				18h~28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Capability Pointer				34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – 7Fh
Power Management Capabilities		Next ID = 8C	Capability ID = 01	80h
PM Data	PPB Support	Power Management Data		84h
Message Control Register		Next ID =9C	Capability ID = 05	8Ch
Message Address Register				90h
Message Upper Address Register				94h
Message Data Register				98h
VPD Register		Next ID = A4	Capability ID = 03	9Ch
VPD Data Register				A0h
Vendor Define Register(28h)		Next ID = E0	Capability ID = 09	A4h
XPIP CSR0				A8h
XPIP CSR1				Ach
ACK Latency Timer		Replay Time-out counter		B0h
UART Driver Selection				B4h
Power Management Control Parameter				B8h
Debug Register				BCh – C4h
PHY Parameter				C8h
Reserved				CCh – D4h
GPIO Data and Control				D8h
EEPROM Data		EEPROM Control		DCh
PCI Express Capability Register		Next ID = 00h	Capability ID = 10	E0h
Device Capability				E4h
Device Status		Device Control		E8h
Link Capability				ECh
Link Status		Link Control		F0h
Reserved				F4h - FCh

Other than the PCI 2.3 compatible configuration space header, the I/O bridge also implements PCI express extended configuration space header, which includes advanced error reporting registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Next Capability Offset = 000h	Capability Version	PCI Express Extended Capability ID = 001h		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register				11Ch~128h

6.2.1. VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.

6.2.2. DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this I/O bridge as the PI7C9X7954. The default value may be changed by auto-loading from EEPROM. Reset to 7954h.

6.2.3. COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. Reset to 0b.
1	Memory Space Enable	RW	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to response to memory Space accesses. Reset to 0b.
2	Bus Master Enable	RO	It is not implemented. Hardwired to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	Controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error Status bit when an error is detected. Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0b.