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3V Bus LVDS 1-to-6 Clock Buffer/Bus Transceiver

Features

- Master/Slave clock selection in a backplane application
- 160 MHz operation (typical)
- 100ps duty cycle distortion (typical)
- 50ps channel to channel skew (typical)
- 3.3V power supply design
- Glitch-free power on at CLKI/O pins
- Low Power design (16mA @ 3.3V static)
- Accepts small swing (300mV typical) differential signal levels
- Industrial temperature operating range (–40°C to +85°C)
- Available in 24-pin TSSOP Packaging (L)

General Description

PI90LVB16 is a six-channel LVTTL clock distribution driver with 50 picosecond channel-to-channel skew. It translates one BLVDS (Bus Low-Voltage Differential Signaling) input signal into six LVTTL-compatible output signals for distribution to adjacent chips on the same board. The PI90LVB16 accepts BLVDS (300mV typical) differential input levels, and translates them to 3V CMOS output levels.

The 160MHz PI90LVB16 can be the master clock, driving inputs of other clock I/O pins in a multipoint environment. It can also drive the BLVDS backplane with a separate channel acting as a return/source LVTTL clock source. The master/slave clock selection of the driving source is controlled by the $CrdCLK_{IN}$ and the $\overline{DE}$ pins. An output enable pin $\overline{OE}$, when high, forces all CLK_{OUT} pins high.

A backplane clock distribution network must be able to drive many transmission line stubs. The Bus LVDS feature of the PI90LVB16 is ideal for driving data transfers in large, high-performance backplane system applications. The device can be used as a source synchronous driver to distribute clock signals within data and telecommunications systems.

Driver Mode Truth Table

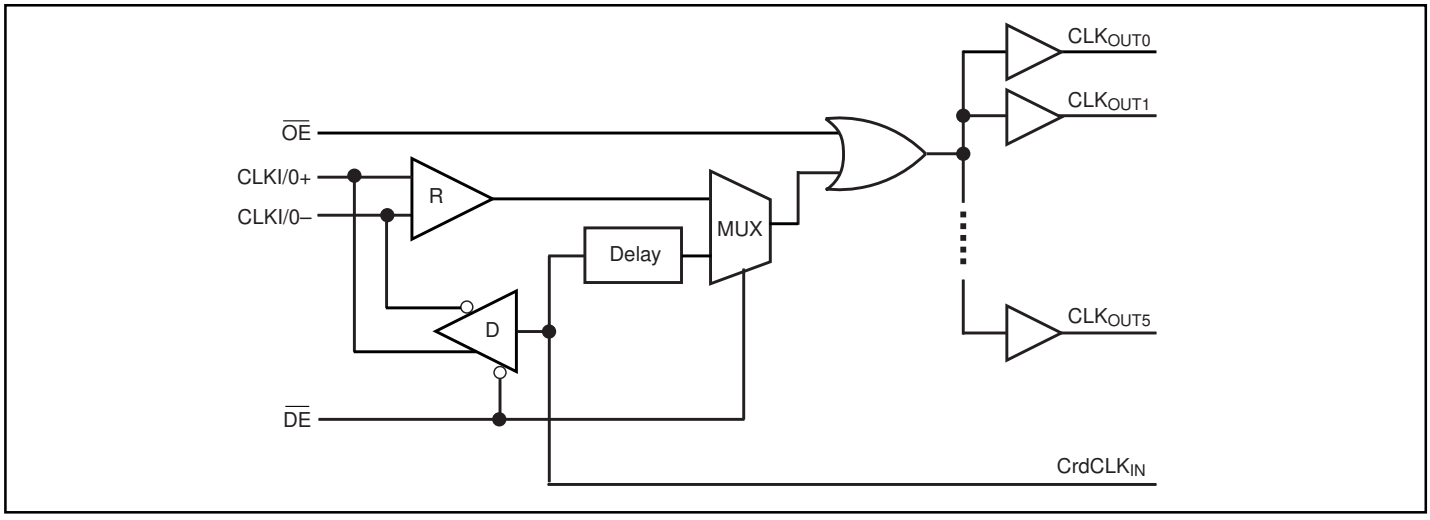
Input			Output		
$\overline{OE}$	$\overline{DE}$	$CrdCLK_{IN}$	CLKI/O+	CLKI/O–	CLK_{OUT}
L	L	L	L	H	L
L	L	H	H	L	H
H	L	L	L	H	H
H	L	H	H	L	H
H	H	X	Z	Z	H

Receive Mode Truth Table

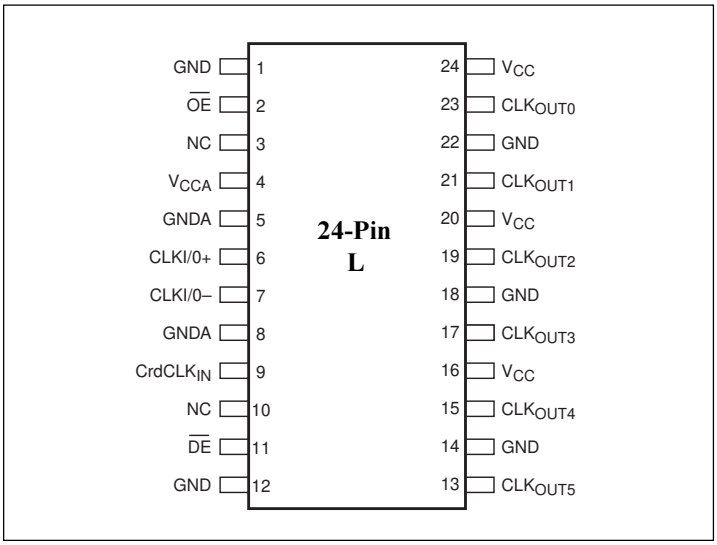
Input				Output
$\overline{OE}$	$\overline{DE}$	$CrdCLK_{IN}$	(CLKI/O+)–(CLKI/O–)	CLK_{OUT}
H	H	X	X	H
L	H	X	VID ≥ 0.07V	H
L	H	X	VID ≤ –0.07V	L

L = Low Logic State; H = High Logic State; X = Irrelevant
Z = High Impedance

Function Diagram



Connection Diagram



TSSOP Package Pin Description

Pin Name	Pin #	Type	Description
CLKI/O+	6	I/O	True (Positive) side of the differential clock input.
CLKI/O–	7	I/O	Complementary (Negative) side of the differential clock input.
$\overline{OE}$	2	I	$\overline{OE}$; this pin is active Low. When High, this pin forces all CLK_{OUT} pin High. When Low, CLK_{OUT} pins logic state is determined by either the CrdCLKIN or VID at the CLKI/O pins with respect to the logic level at the $\overline{DE}$ pin. This pin has a weak pullup device to V_{CC}. If $\overline{OE}$ is floating, then all CLK_{OUT} pins will be High.
$\overline{DE}$	11	I	$\overline{DE}$; this pin is active Low. When Low, this pin enables the $CardCLK_{IN}$ signal to the CLKI/O pins and CLK_{OUT}. When High the Driver is 3-State, the CLKI/O pins are inputs and determine the state of the CLK_{OUT} pins. This pin has a weak pullup device to V_{CC}. If $\overline{DE}$ is floating, then all CLKI/O pins are 3-State.
CLK_{OUT}	13,15,17,19,21,23	O	Six Buffered clock (CMOS) outputs.
$CrdCLK_{IN}$	9	I	Input clock from Card (CMOS level or TTL level).
V_{CC}	16,20,24	Power	V_{CC}; Analog V_{CCA} (Internally separate from V_{CC}, connect externally or use separate power supplies). No special power sequencing required. Either V_{CCA} or V_{CC} can be applied first, or simultaneously apply both power supplies.
GND	1,12,14,18,22	Ground	GND
V_{CCA}	4	Power	Analog V_{CCA} (Internally separate from V_{CC}, connect externally or use separate power supplies). No special power sequencing required. Either V_{CCA} or V_{CC} can be applied first, or simultaneously apply both power supplies.
GNDA	5,8	Ground	Analog Ground (Internally separate from Ground must be connected externally.
NC	3,10		No Connects.

Absolute Maximum Ratings(1)

Supply Voltage Range, V_{CC}	–0.3V to +4V
Enable Input Voltage (DE, OE, CrdCLK$_{IN}$)	–0.3V to +4V
Voltage (CLK$_{OUT}$)	–0.3V to (V_{CC} + 0.3V)
Voltage (CLKI/O±)	–0.3V to (V_{CC} + 0.3V)
Driver Short Circuit Current	momentary
Receiver Short Circuit Current	momentary
Maximum Package Power Dissipation at +25°C	
TSSOP Package	1500mW
Derate TSSOP Package	8.2mW/°C above +25°C
θ_{JA}	95°C/W
θ_{JC}	30°C/W
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering, 4s)	260°C
ESD Ratings: HBM(2)	9kV
CLK$_{OUT(0–5)}$	≥2kV
CDM(2)	>1000V
Machine Model(2)	>200V

Recommended Operating Conditions

	Min.	Typ.	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
CrdCLK$_{IN}$, $\overline{DE}$, $\overline{OE}$ Input Voltage	0		V_{CC}	V
Operating Free Air Temperature (T_A)	–40	24	+85	°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specificed[3,4]

Symbol	Parameter	Conditions	Pin	Min.	Typ.	Max.	Units
V_{TH}	Input Threshold High		CLKI/O+, CLKI/O–		25	75	mV
V_{TL}	Input Threshold Low			–70	–35		
VCMR	Common Mode Voltage Range[5]	VID = 250mV peak-to-peak		$\lvert V_{ID} \rvert /2$		2.8 – $\lvert V_{ID} \rvert /2$	V
I_{IN}	Input Current	V_{IN} = OV to V_{CC}, $\overline{DE}$ = V_{CC}, $\overline{OE}$ = V_{CC}, Other Input = 1.2V ±50mV		–10	±5	+10	µA
V_{OH1R}	Output High Voltage	VID =250mV, I_{OH} = –1.0mA	CLK_{OUT}	V_{CC} –0.2	2.9		V
V_{OH2R}	Output High Voltage	VID =250mV, I_{OH} = –6mA		V_{CC} –0.6	2.5		
V_{OL1R}	Output Low Voltage	I_{OL} =1.0mA, VID = –250mV			0.04	0.1	
V_{OL2R}	Output Low Voltage	I_{OL} =6mA, VID = –250mV		0	0.22	0.4	
I_{ODHR}	CLK_{OUT} Dynamic Output Current[6]	VID = +250mV, V_{OUT} = V_{CC}–1V		–16	–24	–34	mA
I_{ODLR}		VID = –250mV, V_{OUT} = 1V		14	25	37.5	
V_{IH}	Input High Voltage		$\overline{DE}$, $\overline{OE}$, $CrdCLK_{IN}$	2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V	$\overline{OE}$, $\overline{DE}$	–6	4	6	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V		–20	11	+20	
I_{INCRD}	Input Current	V_{IN} = 0V to V_{CC}, $\overline{OE}$ = V_{CC}	$CrdCLK_{IN}$	–5		5	
V_{CL}	Input Voltage Clamp	I_{OUT} = –1.5mA	$\overline{OE}$, $\overline{DE}$, $CrdCLK_{IN}$	–0.8			V
I_{CC}	No Load Supply Current Outputs Enabled, No VID Applied	$\overline{OE}$ = $\overline{DE}$ = 0V, $CrdCLK_{IN}$ = V_{CC} or GND, CLKI/O(±) = Open CLK_{OUT} (0:5) = Open Circuit	V_{CC}			10	mA
I_{CC1}	No Load Supply Current Outputs Enabled, VID over Common Voltage Range	$\overline{OE}$ = GND, $\overline{DE}$ = V_{CC}, $CrdCLK_{IN}$ = V_{CC} or GND, VID = 250mV (0.125V VCM 2.275V) CLK_{OUT}(0:5) = Open Circuit				6	
I_{CCD}	Driver Loaded Supply Current	$\overline{DE}$ = $\overline{OE}$ = 0V, $CrdCLK_{IN}$ = V_{CC} or GND, R_L = 37.5Ω between CLKI/O+ and CLKI/O–, CLK_{OUT} (0:5) = Open Circuit		16		21	

DC Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specificed[3,4]

Symbol	Parameter	Conditions	Pin	Min.	Typ.	Max.	Units
V_{OD}	Driver Output Differential Voltage	R_L = 37.5Ω, Figure 5 $\overline{DE}$ = 0V	CLKI/O+, CLKI/O–	250	350	450	mV
ΔV_{OD}	Driver V_{OD} Magnitude Change				2	20	
V_{OS}	Driver Offset Voltage			1.1	1.25	1.5	V
ΔV_{OS}	Driver Offset Voltage Multitude Change				1	20	mV
V_{OHD}	Driver Output High				1.4	1.8	V
V_{OLD}	Driver Output Low			0.8	1.05		
I_{OS1D}	Driver Differential Short Circuit Current[6]	CrdCLK$_{IN}$ = V_{CC} or GND, VOD = 0V, (outputs shorted together), $\overline{DE}$ = 0V			±13	±17	mA
I_{OS2D}	Driver Differential Short Circuit Current to V_{CC}[6]	CrdCLK$_{IN}$ = GND, $\overline{DE}$ = 0V, CLKI/O+ = V_{CC}			11	17	
I_{OS3D}		CrdCLK$_{IN}$ = V_{CC}, $\overline{DE}$ = 0V, CLKI/O– = V_{CC}			10	17	
I_{OS4D}	Driver Differential Short Circuit Current to GND[6]	CrdCLK$_{IN}$ = V_{CC}, $\overline{DE}$ = 0V, CLKI/O+ = 0V			–15	–17	
I_{OS5D}		CrdCLK$_{IN}$ = GND, $\overline{DE}$ = 0V, CLKI/O– = 0V			–15	–17	
I_{OFF}	Power Off Leakage Current	V_{CC} = 0V or Open, $V_{APPLIED}$ = 3.6V				±20	µA

Switching Characteristics

Differential Receiver Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specificed[7,8]

Symbol	Parameter	Conditions	Min.	Typ.[1]	Max.	Units
t_{PHLDR}	Differential Propagation Delay High to Low. $CLK_{I/O}$ to CLK_{OUT}	C_L = 15pF VID = 250mV Figures 1 & 2	1.3	2.6	3.8	ns
t_{PLHDR}	Differential Propagation Delay Low to High. $CLK_{I/O}$ to CLK_{OUT}		1.3	2.6	3.8	
t_{SK1R}	Duty Cycle Distortion[10] pulse skew, |tPLH – tPHL|			5	400	ps
t_{SK2R}	Channel-to-Channel Skew; Same Edge[11]			5	80	
t_{SK3R}	Part-to-Part Skew[12]				TBD	ns
t_{TLHR}	Transition Time Low-to-High[9], (20% to 80%)		1.0	1.4	2.4	
t_{THLR}	Transition Time High-to-Low[9], (80% to 20%)		1.0	1.3	2.4	
t_{PLHOER}	Propagation Delay Low-to-High ($\overline{OE}$ to CLK_{OUT})	C_L = 15pF Figures 3 & 4	1.0	2.1	3.2	
t_{PHLOER}	Propagation Delay High-to-Low ($\overline{OE}$ to CLK_{OUT})		1.0	2.1	3.2	
f_{MAX}	Maximum Operating Frequency[15]		100	160		MHz

Switching Characteristics

Differential Driver Timing Requuirements

(Over supply voltage and operating temperature ranges, unless otherwise specificed[7,8]

Symbol	Parameter	Conditions	Min.	Typ.[1]	Max.	Units
t_{PHLDD}	Differential Propagation Delay High to Low. CrdCLK$_{IN}$ to CLKI/O	C_L = 15pF R_L = 37.5Ω Figures 6 & 7	1.0	1.5	2.2	ns
t_{PLHDD}	Differential Propagation Delay Low to High. CrdCLK$_{IN}$ to CLKI/O		1.0	1.3	2.2	
t_{PHLCrd}	CrdCLK$_{IN}$ to CLK$_{OUT}$ Propagation Delay High to Low	C_L = 15pF Figures 8 & 9	2.0	2.8	4.5	
t_{PLHCrd}	CrdCLK$_{IN}$ to CLK$_{OUT}$ Propagation Delay Low to High		2.0	2.8	4.5	
t_{SK1D}	Differential Skew $\lvert t_{PLH} - t_{PHL} \rvert$[13]	C_L = 15pF Figures 6 & 7			600	ps
t_{SK2D}	Differential Part-to-Part Skew[14]				TBD	ns
t_{TLHD}	Differential Transition Time[9], (20% to 80%)		0.2	0.35	0.65	
t_{THLD}	Differential Transition Time[9], (80% to 20%)		0.2	0.35	0.65	
t_{PHZD}	Transition Time Low to 3-State. $\overline{DE}$ to CLKI/O	V_{IN} = 0V to V_{CC} C_L = 15pF R_L = 37.5Ω Figures 10 & 11			2.6	
t_{PLZD}	Transition Time Low to 3-State. $\overline{DE}$ to CLKI/O				2.6	
t_{PZHD}	Transition Time 3-State-to-High. $\overline{DE}$ to CLKI/O				4.3	
t_{PZLD}	Transition Time 3-State-to-Low. $\overline{DE}$ to CLKI/O				3.6	
f_{MAX}	Maximum Operating Frequency[15]		100	160		MHz

Notes:

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. These ratings are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
2. ESD Rating: ESD qualification is performed per the following: HBM (1.5kΩ, 100pF), Machine Model (250V, 0Ω), IEC 1000-4-2. All V_{CC} pins connected together, all ground pins connected together.
3. Current into device pins are defined as positive. Current out of device pins defined as negative. All voltages are referenced to ground except VID, VOD, VTH, and VTL
4. All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
5. The VCMR range is reduced for larger VID. Example: If VID=400 mV, then VCMR is 02V to 2.2VAVID up to $\lvert V_{CC}$-0V$\rvert$ may be applied between the CLKI/O+ and CLKI/O– inputs, with the Common Mode set to V_{CC}/2.
6. Only one output should be momentarily shorted at a time. Do not exceed package power dissipation rating.
7. C_L includes probe and fixture capacitance.
8. Generator waveform for all tests unless otherwise specified: f = 25 MHz, Zo = 50Ω, t_r = 1ns, t_f = 1ns (10%–90%). To ensure fastest propagation delay and minimum skew, clock input edge rates should not be slower than 1ns/V; control signals not slower than 3ns/V. In general, the faster the input edge rate, the better the AC performance,
9. All device output transition times are based on characterization measurements and are guaranteed by design.
10. t_{SKIR} is the difference in receiver propagation delay $\lvert t_{PLH}$-$t_{PHL} \rvert$ of one device, and is the duty cycle distortion of the output at any given temperature and V_{CC}. The propagation delay specification is a device-to-device worst case over process, voltage and temperature.
11. t_{SK2R} is the difference in receiver propagation delay between channels in the same device of any outputs switching in the same direction. This parameter is guaranteed by design and characterization.
12. t_{SK3R} part-to-part skew, is the difference in receiver propagation delay between devices of any outputs switching in the same direction. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SK3R} is defined as Max-Min differential propagation delay. This parameter is guaranteed by design and characterization.
13. t_{SK1D} is the difference in driver propagation delay $\lvert t_{PLH}$-$t_{PHL} \rvert$and is the duty cycle distortion of the CLKI/O outputs.
14. t_{SK2D} part-to-part skew, is the difference in driver propagation delay between devices of any outputs switching in the same direction. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SK2D} is defined as Max-Min differential propagation delay.
15. Generator input conditions: $t_r t_f$ < 1ns, 50% duty cycle, differential (1.10V to 1.35V pk-pk). Output Criteria: 60%/40% duty cycle, V_{OL}(max) 0.4V, V_{OH}(min) 2.7V, Load - 7pF (stray plus probes).

Parameter Measurement Information

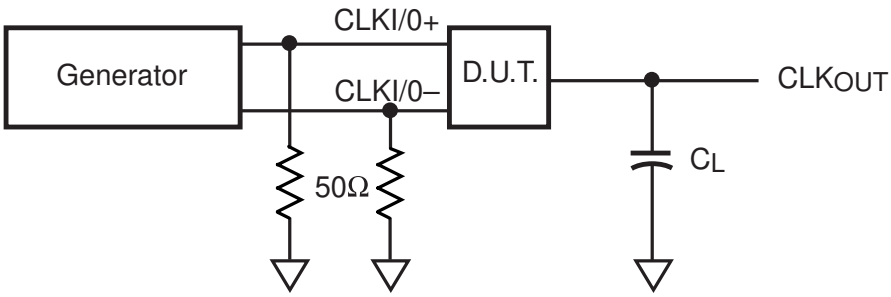
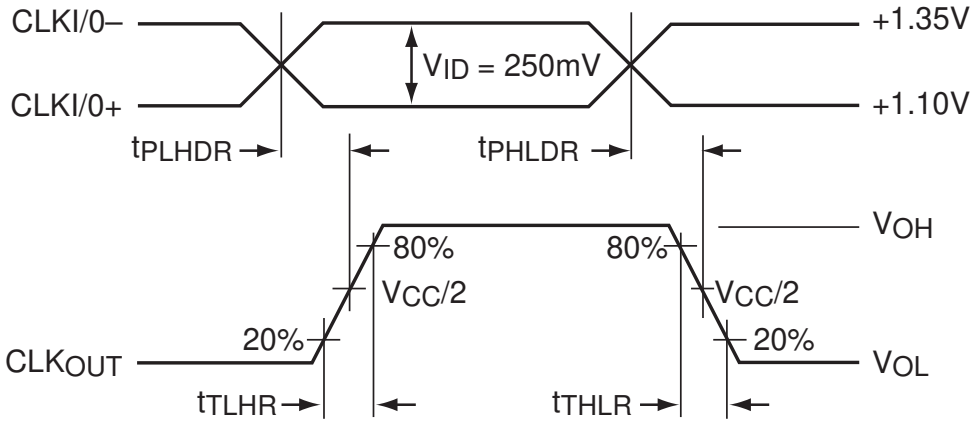


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit



Generator waveform for all test unless otherwise specificed: f = 25MHz, 50% Duty Cycle, Z0 = 50Ω, t_{THL} = 1ns

Figure 2. Receiver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information

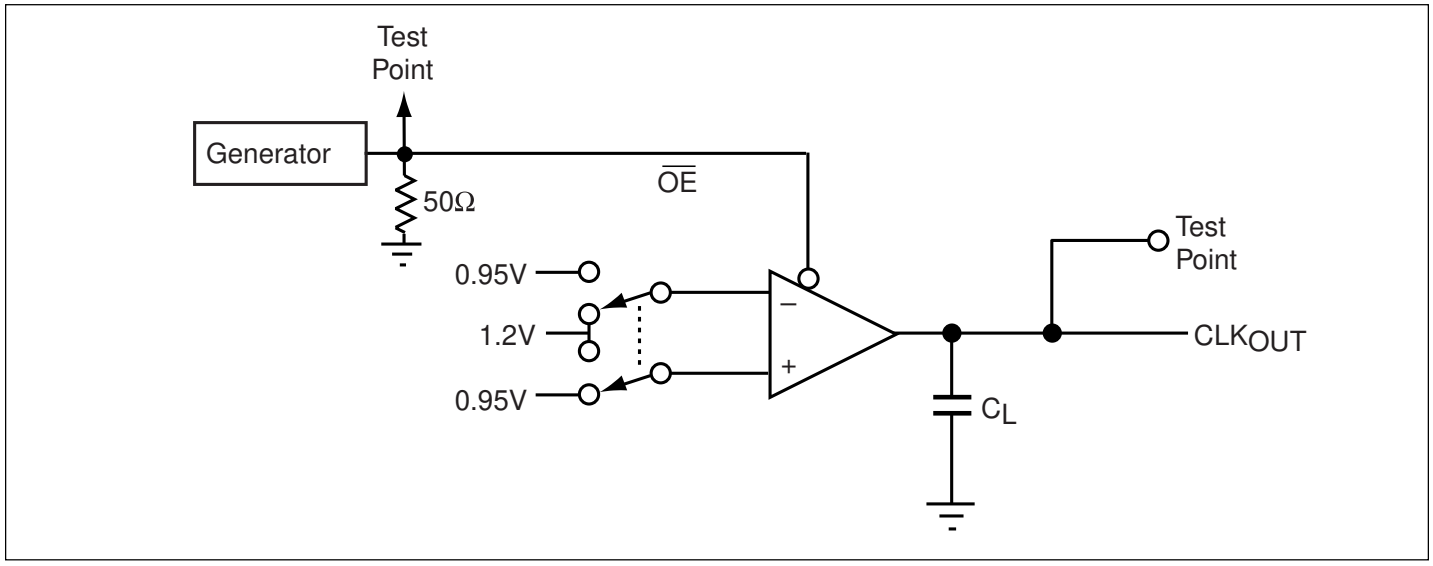


Figure 3. Output Enable ($\overline{OE}$) Test Circuit

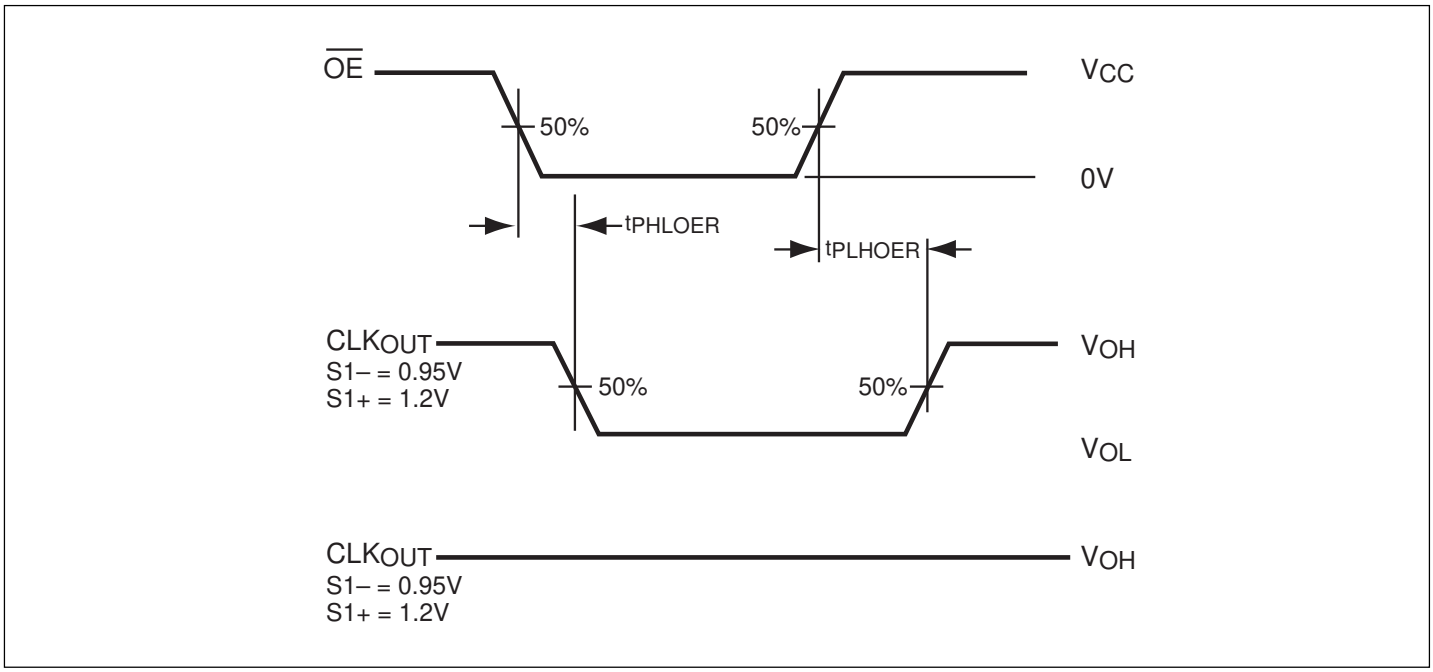


Figure 4. Output Enable ($\overline{OE}$) Delay Waveforms

Parameter Measurement Information

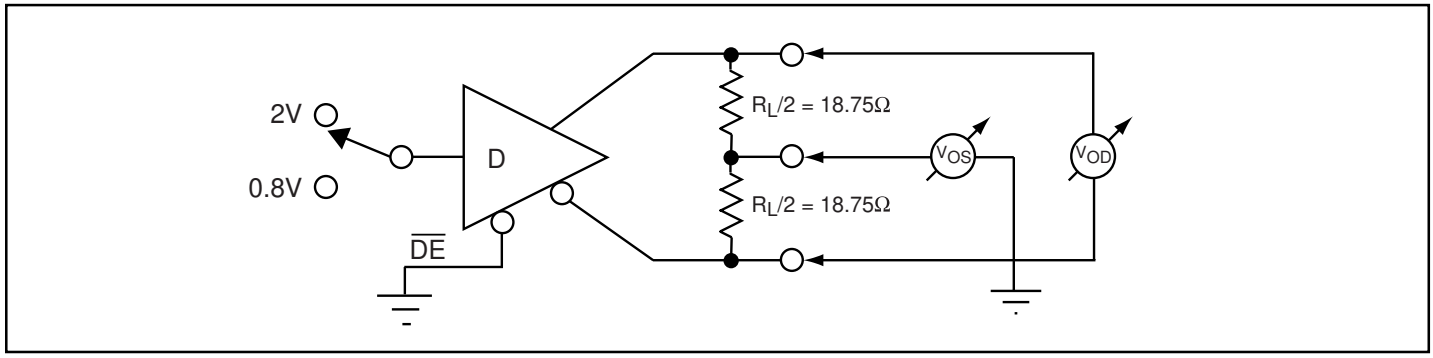


Figure 5. Differential Driver DC Test

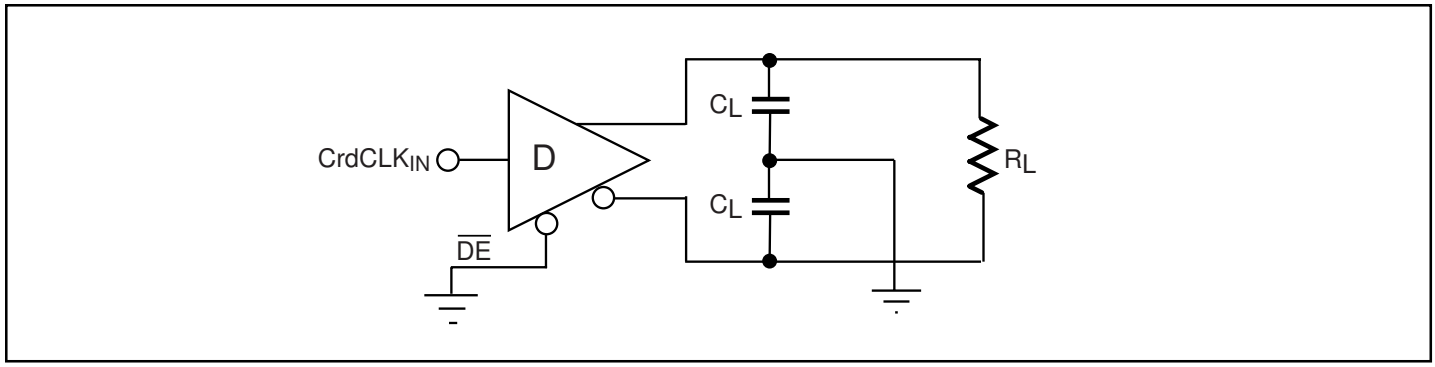


Figure 6. Driver Propagation Delay Test Circuit

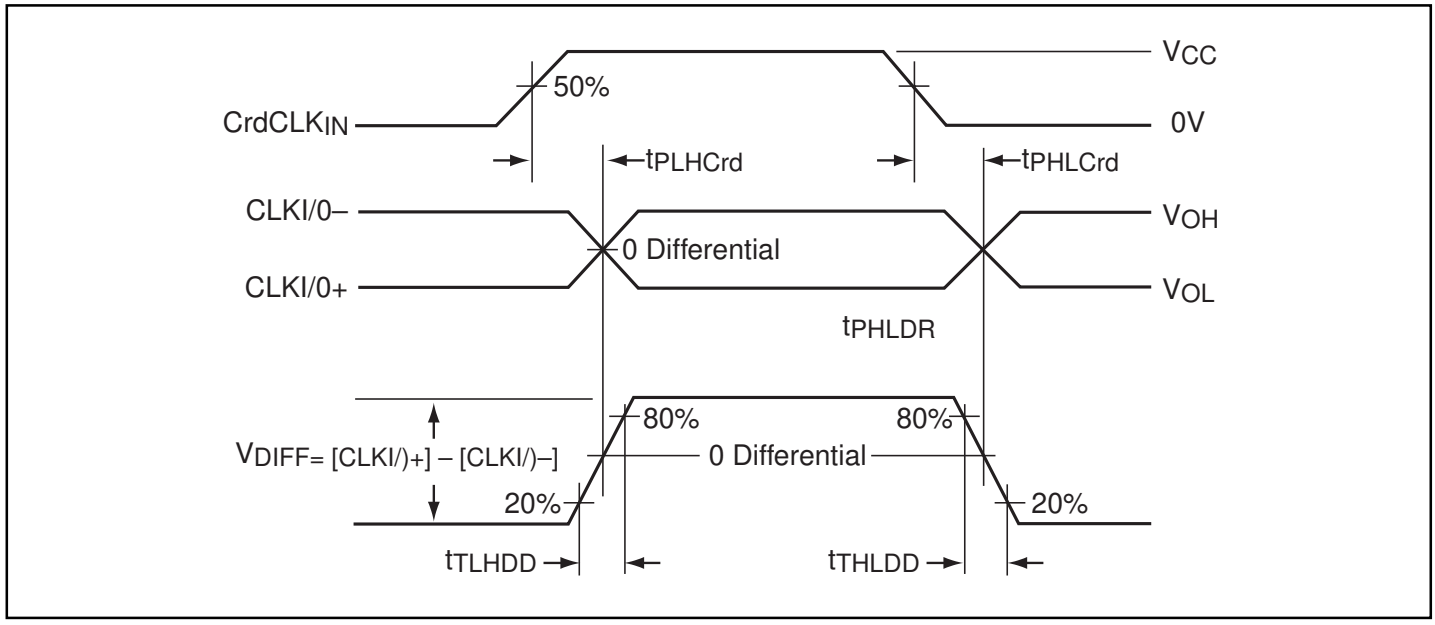


Figure 7. Driver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information

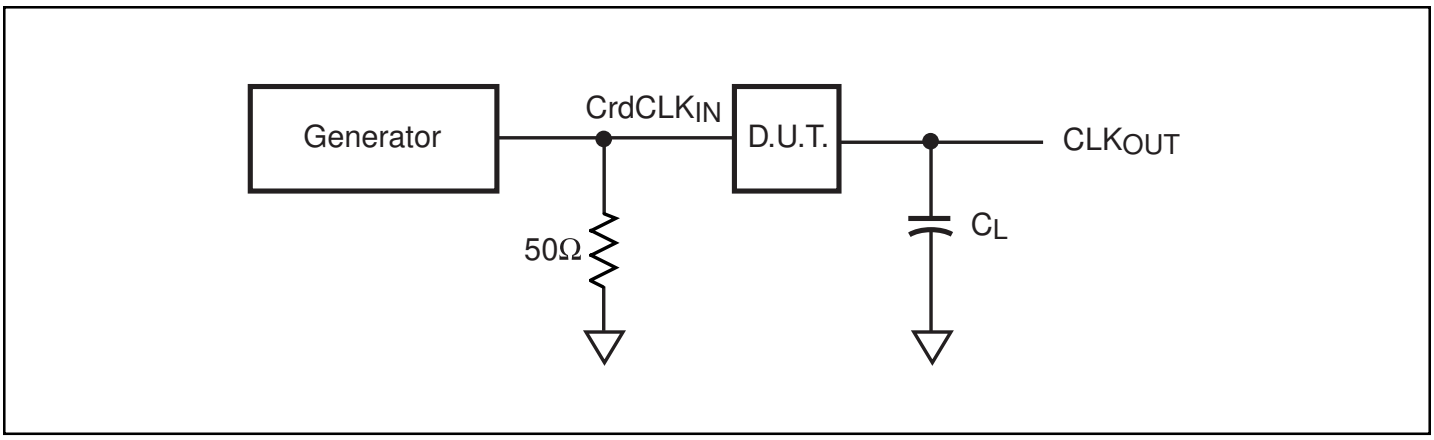


Figure 8. $CrdCLK_{IN}$ Propagation Delay Time Test Circuit

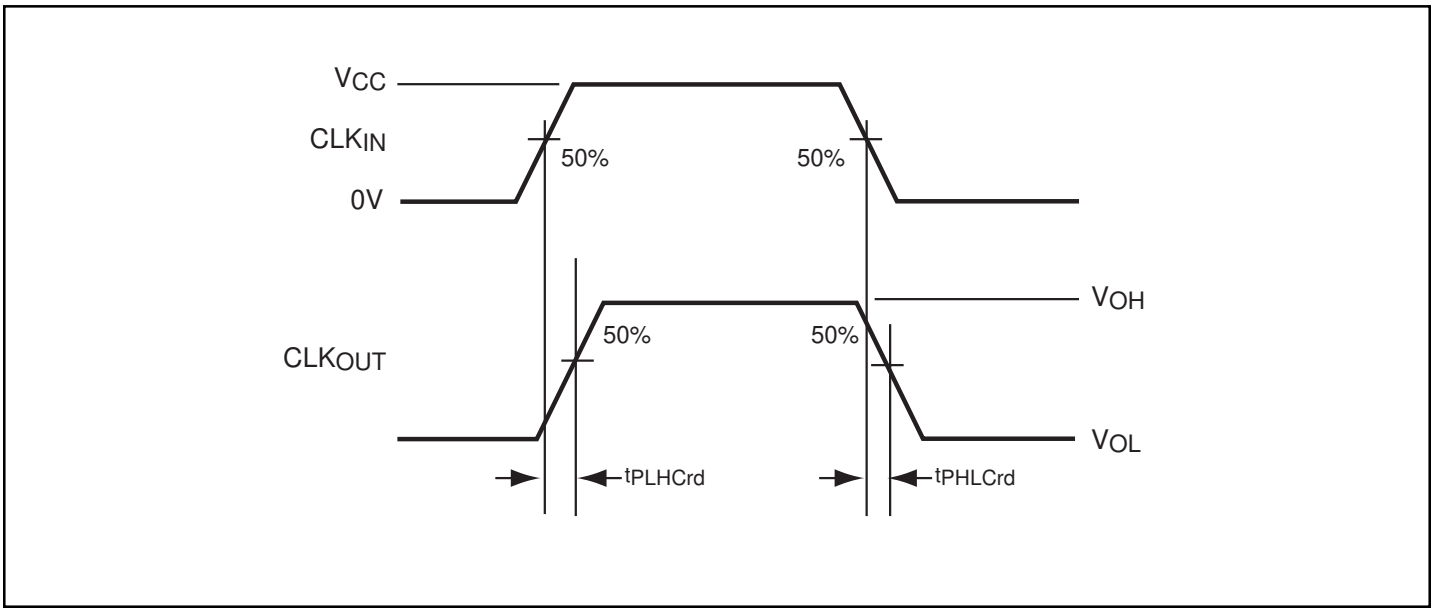


Figure 9. $CrdCLK_{IN}$ Propagation Delay Time Waveforms

Parameter Measurement Information

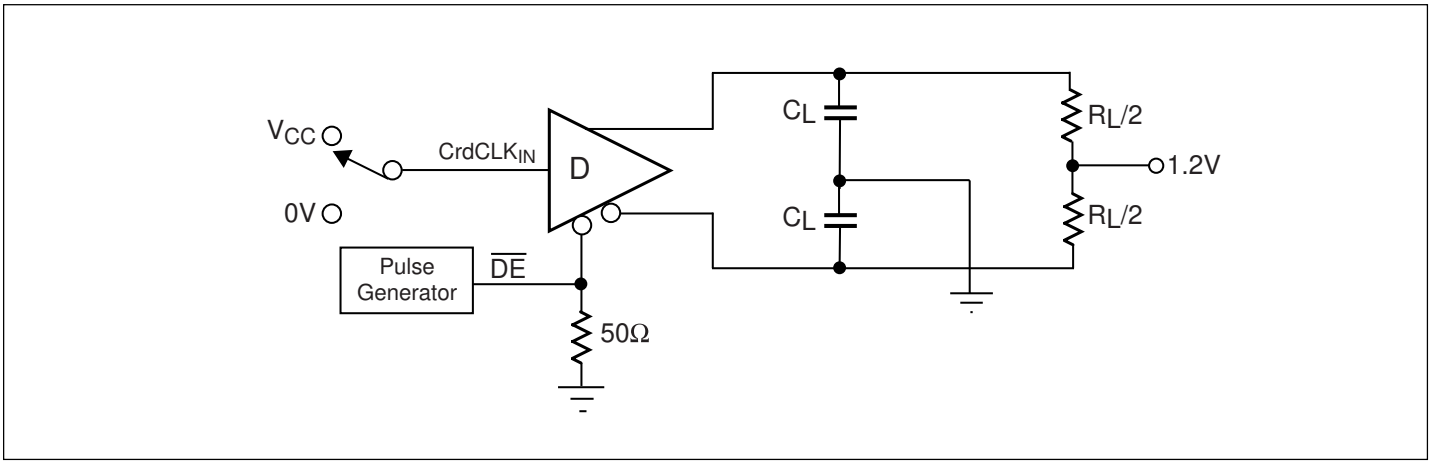


Figure 10. Driver 3-State Test Circuit

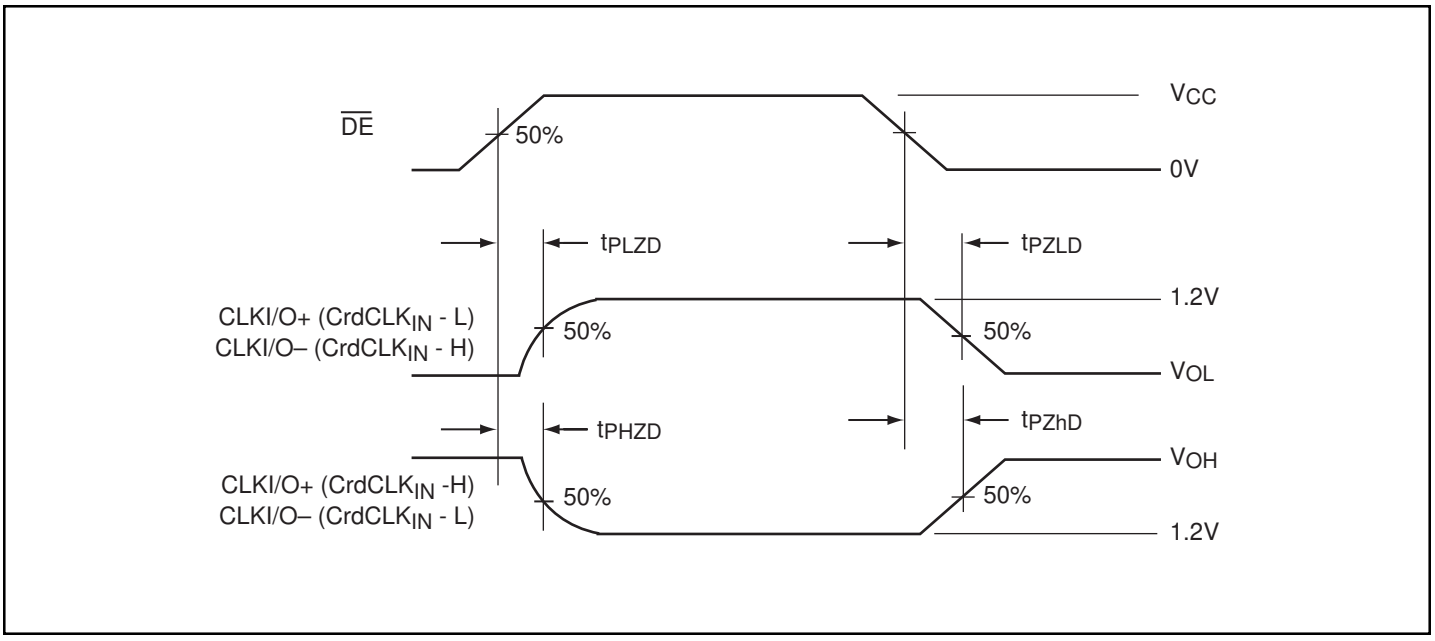
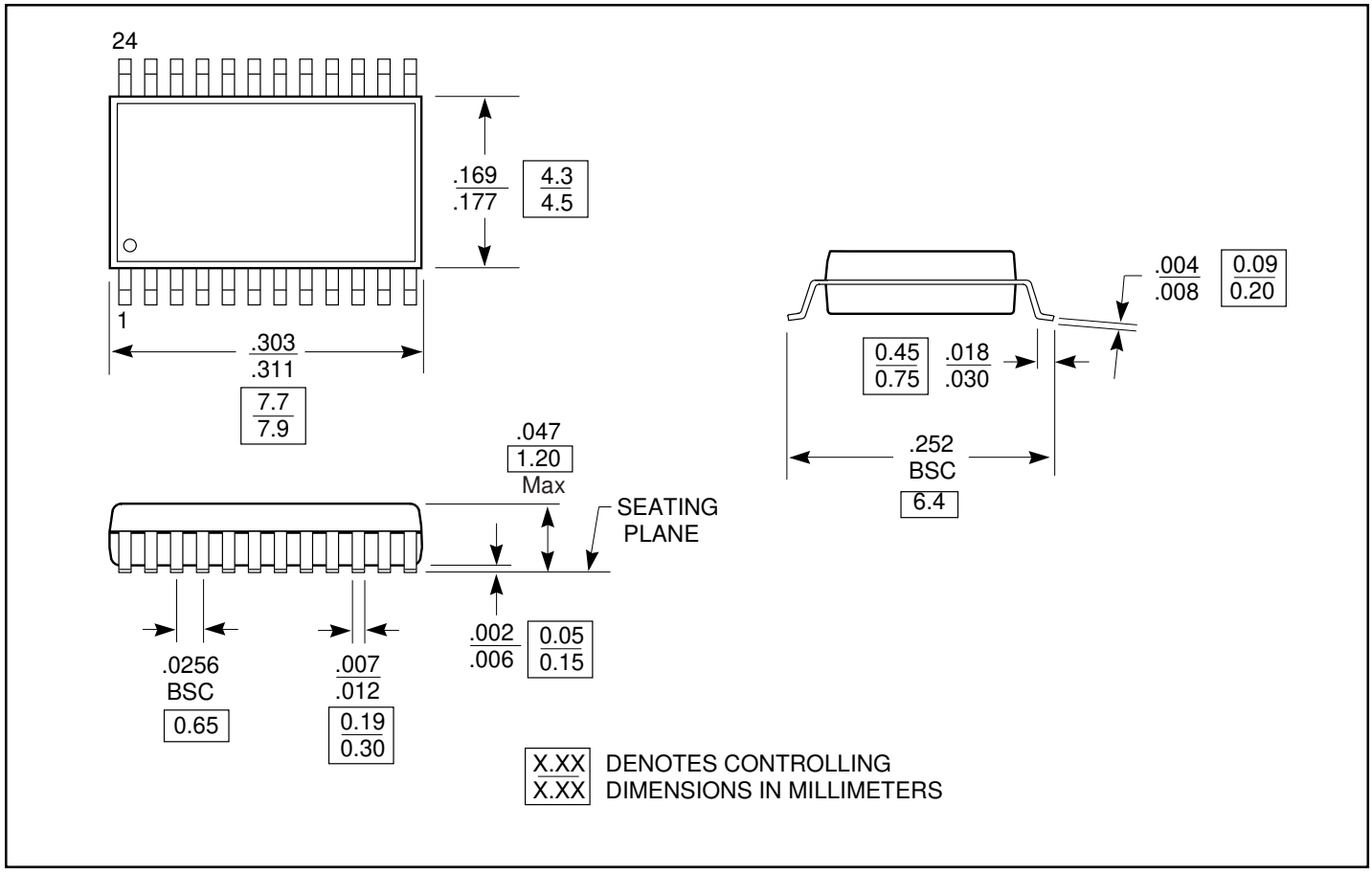


Figure 11. Driver 3-State Waveforms

24-Pin TSSOP (L) Package



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI90LVB16L	L24	24-pin TSSOP	–40°C to 85°C