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PIC10(L)F320/322

6/8-Pin Flash-Based, 8-Bit Microcontrollers

High-Performance RISC CPU

- Only 35 Instructions to Learn:
  - All single-cycle instructions, except branches
- Operating Speed:
  - DC – 16 MHz clock input
  - DC – 250 ns instruction cycle
- Eight-level Deep Hardware Stack
- Interrupt Capability
- Processor Self-Write/Read access to Program Memory
- Pinout Compatible to other 6-Pin PIC10FXXX Microcontrollers

Memory

- Up to 512 Words of Flash Program Memory
- 64 Bytes Data Memory
- High-Endurance Flash Data Memory (HEF)
  - 128B of nonvolatile data storage
  - 100K erase/write cycles

Special Microcontroller Features

- Low-Power 16 MHz Internal Oscillator:
  - Software selectable frequency range from 16 MHz to 31 kHz
  - Factory calibrated to ± 1%, typical
- Wide Operating Range:
  - 1.8V to 3.6V (PIC10LF320/322)
  - 2.3V to 5.5V (PIC10F320/322)
- Power-On Reset (POR)
- Power-up Timer (PWRT)
- Brown-Out Reset (BOR)
- Ultra Low-Power Sleep Regulator
- Extended Watchdog Timer (WDT)
- Programmable Code Protection
- Power-Saving Sleep mode
- Selectable Oscillator Options (EC mode or Internal Oscillator)
- In-Circuit Serial Programming™ (ICSP™) (via Two Pins)
- In-Circuit Debugger Support
- Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V (‘F’ variant only) Output Levels
- Integrated Temperature Indicator
- 40-year Flash Data Retention

eXtreme Low-Power (XLP) Features (PIC10LF320/322)

- Sleep Current:
  - 20 nA @ 1.8V, typical
- Operating Current:
  - 25 μA @ 1 MHz, 1.8V, typical
- Watchdog Timer Current:
  - 500 nA @ 1.8V, typical

Peripheral Features

- Four I/O Pins:
  - One input-only pin
  - High current sink/source for LED drivers
  - Individually selectable weak pull-ups
  - Interrupt-on-Change
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two PWM modules:
  - 10-bit PWM, max. frequency 16 kHz
  - Combined to single 2-phase output
- A/D Converter:
  - 8-bit resolution with 3 channels
- Configurable Logic Cell (CLC):
  - 8 selectable input source signals
  - Two inputs per module
  - Software selectable logic functions including: AND/OR/XOR/D Flop/D Latch/SR/JK
  - External or internal inputs/outputs
  - Operation while in Sleep
- Numerically Controlled Oscillator (NCO):
  - 20-bit accumulator
  - 16-bit increment
  - Linear frequency control
  - High-speed clock input
  - Selectable Output modes
    - Fixed Duty Cycle (FDC)
    - Pulse Frequency (PF) mode
- Complementary Waveform Generator (CWG):
  - Selectable falling and rising edge dead-band control
  - Polarity control
  - Two auto-shutdown sources
  - Multiple input sources: PWM, CLC, NCO

PIC10(L)F320/322 Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High Endurance Flash (bytes)	I/O's(2)	8-Bit ADC (ch)	Timers (8-Bit)	PWM	Complementary Wave Generator (CWG)	Configurable Logic Cell (CLC)	Fixed Voltage Reference (FVR)	Numerically Controlled Oscillator (NCO)	Debug(1)	XLP
PIC10(L)F320	(1)	256	64	128	4	3	2	2	1	1	1	1	H	Y
PIC10(L)F322	(1)	512	64	128	4	3	2	2	1	1	1	1	H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Available using Debug Header; E - Emulation, Available using Emulation Header.

2: One pin is input-only.

Data Sheet Index:

1: DS40001585 PIC10(L)F320/322 Data Sheet, 6/8 Pin High Performance, Flash Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

FIGURE 1: 6-PIN DIAGRAM, PIC10(L)F320/322

SOT-23

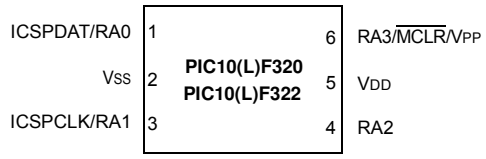

FIGURE 2: 8-PIN DIAGRAM, PIC10(L)F320/322

PDIP, DFN

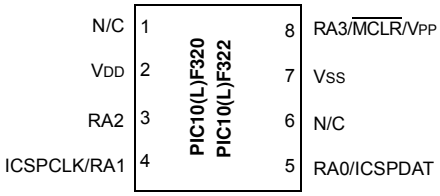

TABLE 1: 6 AND 8-PIN ALLOCATION TABLE, PIC10(L)F320/322

I/O	6-Pin	8-Pin	Analog	Timer	PWM	Interrupts	Pull-ups	CWG	NCO	CLC	Basic	ICSP
RA0	1	5	AN0	—	PWM1	IOC0	Y	CWG1A	—	CLC1IN0	—	ICSPDAT
RA1	3	4	AN1	—	PWM2	IOC1	Y	CWG1B	NCO1CLK	CLC1	CLKIN	ICSPCLK
RA2	4	3	AN2	T0CKI	—	INT/IOC2	Y	$\overline{\text{CWG1FLT}}$	NCO1	CLC1IN1	CLKR	
RA3	6	8	—	—	—	IOC3	Y	—	—	—	$\overline{\text{MCLR}}$	VPP
N/C	—	1	—	—	—	—	—	—	—	—	—	—
N/C	—	6	—	—	—	—	—	—	—	—	—	—
VDD	5	2	—	—	—	—	—	—	—	—	VDD	—
VSS	2	7	—	—	—	—	—	—	—	—	VSS	—

Table of Contents

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1.0 DEVICE OVERVIEW

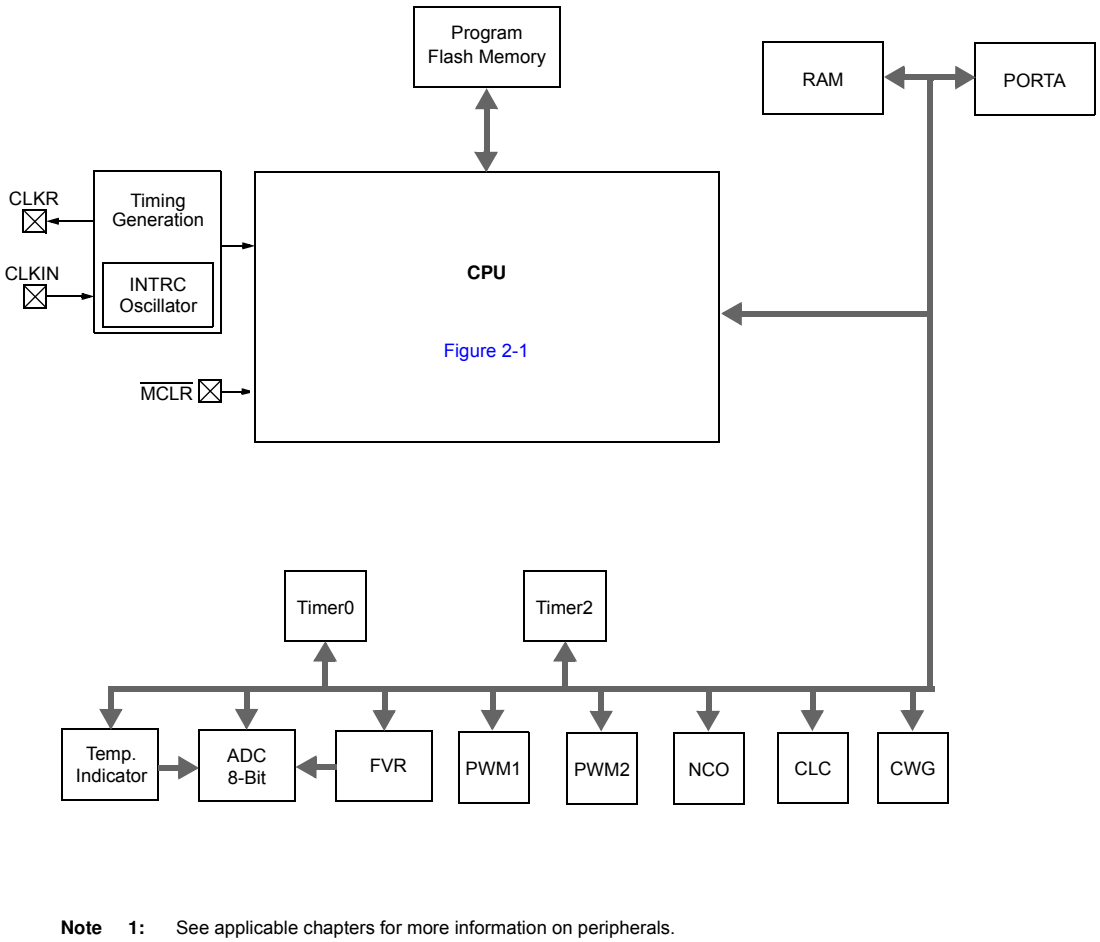
The PIC10(L)F320/322 are described within this data sheet. They are available in 6/8-pin packages. Figure 1-1 shows a block diagram of the PIC10(L)F320/322 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC10(L)F320	PIC10(L)F322
Analog-to-Digital Converter (ADC)		●	●
Configurable Logic Cell (CLC)		●	●
Complementary Wave Generator (CWG)		●	●
Fixed Voltage Reference (FVR)		●	●
Numerically Controlled Oscillator (NCO)		●	●
Temperature Indicator		●	●
PWM Modules			
	PWM1	●	●
	PWM2	●	●
Timers			
	Timer0	●	●
	Timer2	●	●

FIGURE 1-1: PIC10(L)F320/322 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC10(L)F320/322 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/PWM1/CLC1IN0/CWG1A/ AN0/ICSPDAT	RA0	TTL	CMOS	General purpose I/O with IOC and WPU.
	PWM1	—	CMOS	PWM output.
	CLC1IN0	ST	—	CLC input.
	CWG1A	—	CMOS	CWG primary output.
	AN0	AN	—	A/D Channel input.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/PWM2/CLC1/CWG1B/AN1/ CLKIN/ICSPCLK/NCO1CLK	RA1	TTL	CMOS	General purpose I/O with IOC and WPU.
	PWM2	—	CMOS	PWM output.
	CLC1	—	CMOS	CLC output.
	CWG1B	—	CMOS	CWG complementary output.
	AN1	AN	—	A/D Channel input.
	CLKIN	ST	—	External Clock input (EC mode).
	ICSPCLK	ST	—	ICSP™ Programming Clock.
	NCO1CLK	ST	—	Numerical Controlled Oscillator external clock input.
RA2/INT/T0CKI/NCO1/CLC1IN1/ CLKR/AN2/$\overline{\text{CWG1FLT}}$	RA2	TTL	CMOS	General purpose I/O with IOC and WPU.
	INT	ST	—	External interrupt.
	T0CKI	ST	—	Timer0 clock input.
	NCO1	—	CMOS	Numerically Controlled Oscillator output.
	CLC1IN1	ST	—	CLC input.
	CLKR	—	CMOS	Clock Reference output.
	AN2	AN	—	A/D Channel input.
	$\overline{\text{CWG1FLT}}$	ST	—	Complementary Waveform Generator Fault 1 source input.
RA3/$\overline{\text{MCLR}}$/V_{PP}	RA3	TTL	—	General purpose input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	V_{PP}	HV	—	Programming voltage.
V_{DD}	V_{DD}	Power	—	Positive supply.
V_{SS}	V_{SS}	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output
TTL = CMOS input with TTL levels ST = CMOS input with Schmitt Trigger levels
HV = High Voltage

2.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Word
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

2.1 Program Memory Organization

The mid-range core has a 13-bit program counter capable of addressing 8K x 14 program memory space. This device family only implements up to 512 words of the 8K program memory space. Table 2-1 shows the memory sizes implemented for the PIC10(L)F320/322 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 2-1, and 2-2).

TABLE 2-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC10(L)F320	256	00FFh	0080h-00FFh
PIC10(L)F322	512	01FFh	0180h-01FFh

Note 1: High-endurance Flash applies to low byte of each address in the range.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR PIC10(L)F320

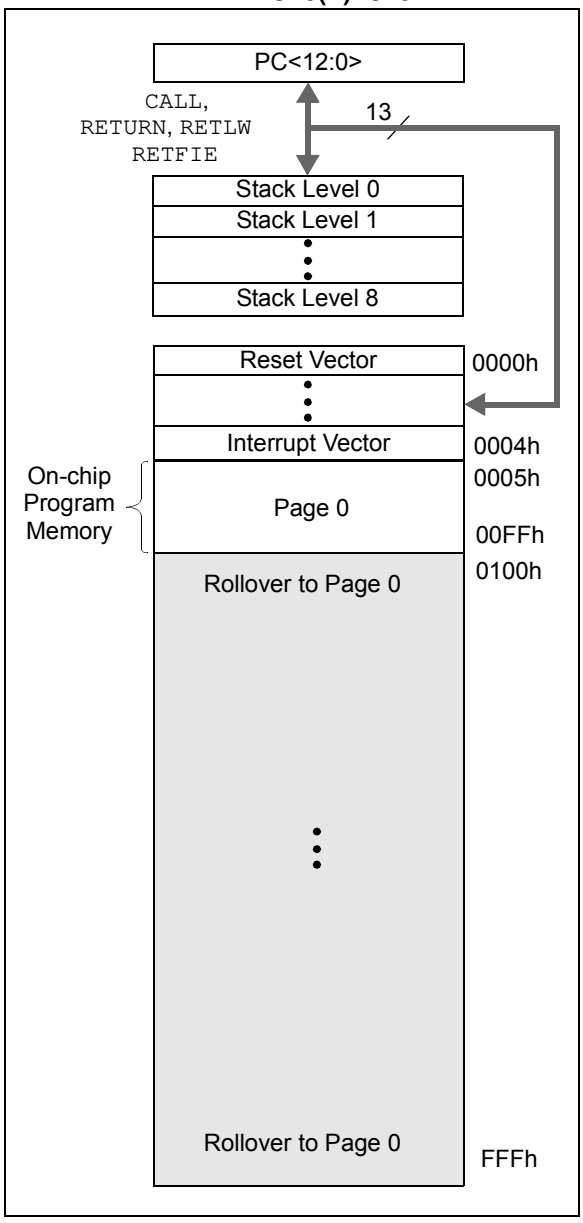
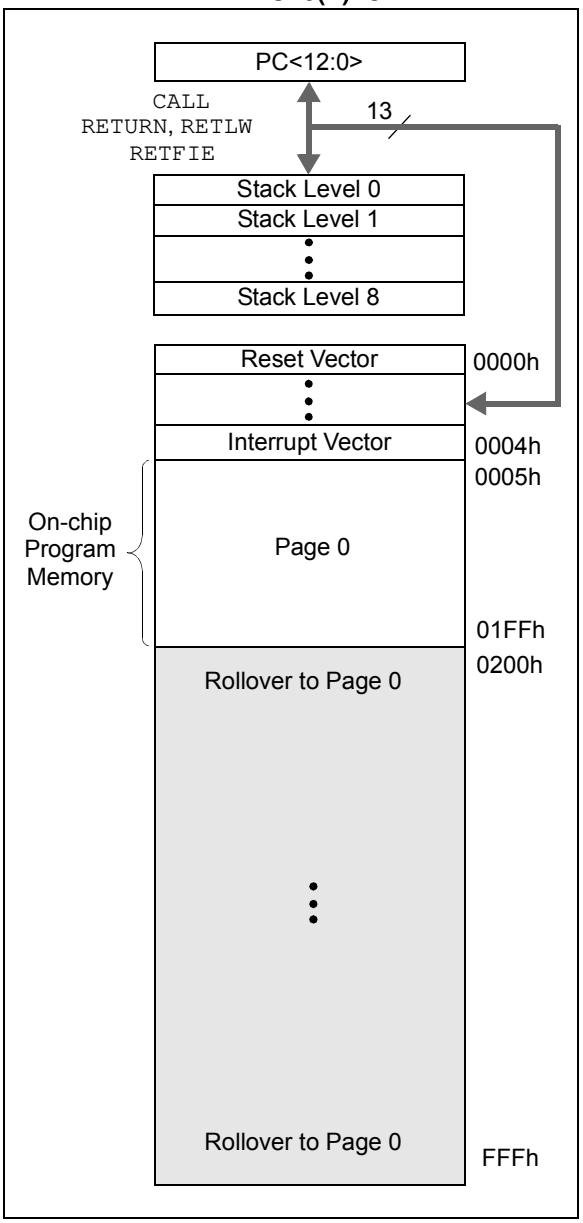


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR PIC10(L)F322



2.2 Data Memory Organization

The data memory is in one bank, which contains the General Purpose Registers (GPR) and the Special Function Registers (SFR). The RP<1:0> bits of the STATUS register are the bank select bits.

RP1	RP0	
0	0	→ Bank 0 is selected

The bank extends up to 7Fh (128 bytes). The lower locations of the bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as Static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC10(L)F320/322. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-3). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (see **Section 23.0 "Instruction Set Summary"**).

Note 1:	Bits IRP and RP1 of the STATUS register are not used by the PIC10(L)F320 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
2:	The C and DC bits operate as a $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R-1/q	R-1/q	R/W-x/u	R/W-x/u	R/W-x/u
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **IRP:** Reserved(2)

bit 6-5 **RP<1:0>:** Reserved(2)

bit 4 **$\overline{TO}$:** Time-out bit
- 1 = After power-up, CLRWDT instruction or SLEEP instruction
- 0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
- 1 = After power-up or by the CLRWDT instruction
- 0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
- 1 = The result of an arithmetic or logic operation is zero
- 0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
- 1 = A carry-out from the 4th low-order bit of the result occurred
- 0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
- 1 = A carry-out from the Most Significant bit of the result occurred
- 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low-order bit of the source register.

2: Maintain as '0'.

2.2.3 DEVICE MEMORY MAPS

The memory maps for PIC10(L)F320/322 are as shown in Table 2-2.

TABLE 2-2: PIC10(L)F320/322 MEMORY MAP (BANK 0)

INDF(*)	00h	PMADRL	20h	General Purpose Registers 32 Bytes	40h	General Purpose Registers 32 Bytes	60h
TMR0	01h	PMADRH	21h				
PCL	02h	PMDATL	22h				
STATUS	03h	PMDATH	23h				
FSR	04h	PMCON1	24h				
PORTA	05h	PMCON2	25h				
TRISA	06h	CLKRCON	26h				
LATA	07h	NCO1ACCL	27h				
ANSELA	08h	NCO1ACCH	28h				
WPUA	09h	NCO1ACCU	29h				
PCLATH	0Ah	NCO1INCL	2Ah				
INTCON	0Bh	NCO1INCH	2Bh				
PIR1	0Ch	Reserved	2Ch				
PIE1	0Dh	NCO1CON	2Dh				
OPTION_REG	0Eh	NCO1CLK	2Eh				
PCON	0Fh	Reserved	2Fh				
OSCCON	10h	WDTCON	30h				
TMR2	11h	CLC1CON	31h				
PR2	12h	CLC1SEL1	32h				
T2CON	13h	CLC1SEL2	33h				
PWM1DCL	14h	CLC1POL	34h				
PWM1DCH	15h	CLC1GLS0	35h				
PWM1CON	16h	CLC1GLS1	36h				
PWM2DCL	17h	CLC1GLS2	37h				
PWM2DCH	18h	CLC1GLS3	38h				
PWM2CON	19h	CWG1CON0	39h				
IOCAP	1Ah	CWG1CON1	3Ah				
IOCAN	1Bh	CWG1CON2	3Bh				
IOCAF	1Ch	CWG1DBR	3Ch				
FVRCON	1Dh	CWG1DBF	3Dh				
ADRES	1Eh	VREGCON	3Eh				
ADCON	1Fh	BORCON	3Fh		5Fh		7Fh

Legend: = Unimplemented data memory locations, read as '0'.

* = Not a physical register.

TABLE 2-3: SPECIAL FUNCTION REGISTER SUMMARY (BANK 0)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	TRISA	—	—	—	—	—(1)	TRISA2	TRISA1	TRISA0	---- 1111	---- 1111
07h	LATA	—	—	—	—	—	LATA2	LATA1	LATA0	---- -xxx	---- -uuu
08h	ANSELA	—	—	—	—	—	ANSA2	ANSA1	ANSA0	---- -111	---- -111
09h	WPUA	—	—	—	—	WPUA3	WPUA2	WPUA1	WPUA0	---- 1111	---- 1111
0Ah	PCLATH	—	—	—	—	—	—	—	PCLH0	---- ---0	---- ---0
0Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 000u
0Ch	PIR1	—	ADIF	—	NCO1IF	CLC1IF	—	TMR2IF	—	-0-0 0-0-	-0-0 0-0-
0Dh	PIE1	—	ADIE	—	NCO1IE	CLC1IE	—	TMR2IE	—	-0-0 0-0-	-0-0 0-0-
0Eh	OPTION_REG	$\overline{WPUEN}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>			1111 1111	uuuu uuuu
0Fh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
10h	OSCCON	—	IRCF<2:0>			HFIOFR	—	LFIOFR	HFIOFS	-110 0-00	-110 0-00
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
12h	PR2	Timer2 Period Register								1111 1111	1111 1111
13h	T2CON	—	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
14h	PWM1DCL	PWM1DCL<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
15h	PWM1DCH	PWM1DCH<7:0>								xxxx xxxx	uuuu uuuu
16h	PWM1CON	PWM1EN	PWM1OE	PWM1OUT	PWM1POL	—	—	—	—	0000 ----	0000 ----
17h	PWM2DCL	PWM2DCL<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
18h	PWM2DCH	PWM2DCH<7:0>								xxxx xxxx	uuuu uuuu
19h	PWM2CON	PWM2EN	PWM2OE	PWM2OUT	PWM2POL	—	—	—	—	0000 ----	0000 ----
1Ah	IOCAP	—	—	—	—	IOCAP3	IOCAP2	IOCAP1	IOCAP0	---- 0000	---- 0000
1Bh	IOCAN	—	—	—	—	IOCAN3	IOCAN2	IOCAN1	IOCAN0	---- 0000	---- 0000
1Ch	IOCAF	—	—	—	—	IOCAF3	IOCAF2	IOCAF1	IOCAF0	---- 0000	---- 0000
1Dh	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	—	—	ADFVR<1:0>		0x00 --00	0x00 --00
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON	ADCS<2:0>			CHS<2:0>			GO/$\overline{DONE}$	ADON	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

TABLE 2-3: SPECIAL FUNCTION REGISTER SUMMARY (BANK 0) (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
Bank 0 (Continued)											
20h	PMADRL	PMADR<7:0>								0000 0000	0000 0000
21h	PMADRH	—	—	—	—	—	—	—	PMADR8	---- ---0	---- ---0
22h	PMDATL	PMDAT<7:0>								xxxx xxxx	uuuu uuuu
23h	PMDATH	—	—	PMDAT<13:8>						--xx xxxx	--uu uuuu
24h	PMCON1	—	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	1000 0000	1000 q000
25h	PMCON2	Program Memory Control Register 2 (not a physical register)								0000 0000	0000 0000
26h	CLKRCON	—	CLKROE	—	—	—	—	—	—	-0-- ----	-0-- ----
27h	NCO1ACCL	NCO1 Accumulator <7:0>								0000 0000	0000 0000
28h	NCO1ACCH	NCO1 Accumulator <15:8>								0000 0000	0000 0000
29h	NCO1ACCU	—				NCO1 Accumulator <19..16>				---- 0000	---- 0000
2Ah	NCO1INCL	NCO1 Increment <7:0>								0000 0001	0000 0001
2Bh	NCO1INCH	NCO1 Increment <15:8>								0000 0000	0000 0000
2Ch	—	Unimplemented								—	—
2Dh	NCO1CON	N1EN	N1OE	N1OUT	N1POL	—	—	—	N1PFM	0000 ---0	00x0 ---0
2Eh	NCO1CLK	N1PWS<2:0>			—	—	—	N1CKS<1:0>		000- --00	000- --00
2Fh	Reserved	Reserved								xxxx xxxx	uuuu uuuu
30h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
31h	CLC1CON	LC1EN	LC1OE	LC1OUT	LC1INTP	LC1INTN	LC1MODE<2:0>			00x0 -000	00x0 -000
32h	CLC1SEL0	—	LC1D2S<2:0>			—	LC1D1S<2:0>			-xxx -xxx	-uuu -uuu
33h	CLC1SEL1	—	LC1D4S<2:0>			—	LC1D3S<2:0>			-xxx -xxx	-uuu -uuu
34h	CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	0--- xxxx	0--- uuuu
35h	CLC1GLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	xxxx xxxx	uuuu uuuu
36h	CLC1GLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	xxxx xxxx	uuuu uuuu
37h	CLC1GLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	xxxx xxxx	uuuu uuuu
38h	CLC1GLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	xxxx xxxx	uuuu uuuu
39h	CWG1CON0	G1EN	G1OEB	G1OEA	G1POLB	G1POLA	—	—	G1CS0	0000 0--0	0000 0--0
3Ah	CWG1CON1	G1ASDLB<1:0>		G1ASDLA<1:0>		—	—	G1IS<1:0>		xxxx --xx	uuuu --uu
3Bh	CWG1CON2	G1ASE	G1ARSEN	—	—	—	—	G1ASDCLC1	G1ASDFLT	xx-- --xx	uu-- --uu
3Ch	CWG1DBR	—	—	CWG1DBR<5:0>						--xx xxxx	--uu uuuu
3Dh	CWG1DBF	—	—	CWG1DBF<5:0>						--xx xxxx	--uu uuuu
3Eh	VREGCON	—	—	—	—	—	—	VREGPM1	Reserved	---- --01	---- --01
3Fh	BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	10-- ---q	uu-- ---u

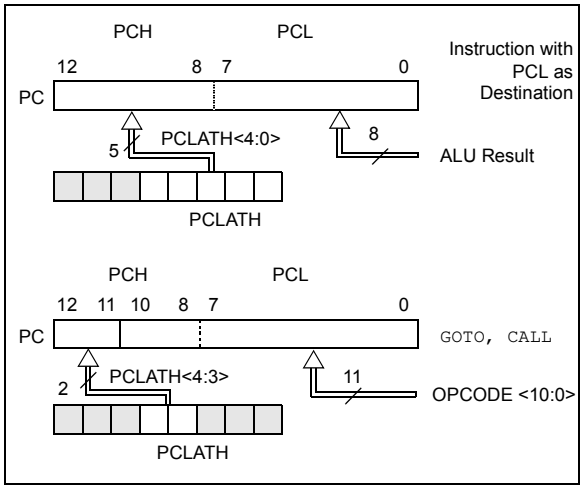
Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper five bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower eight bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 STACK

All devices have an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

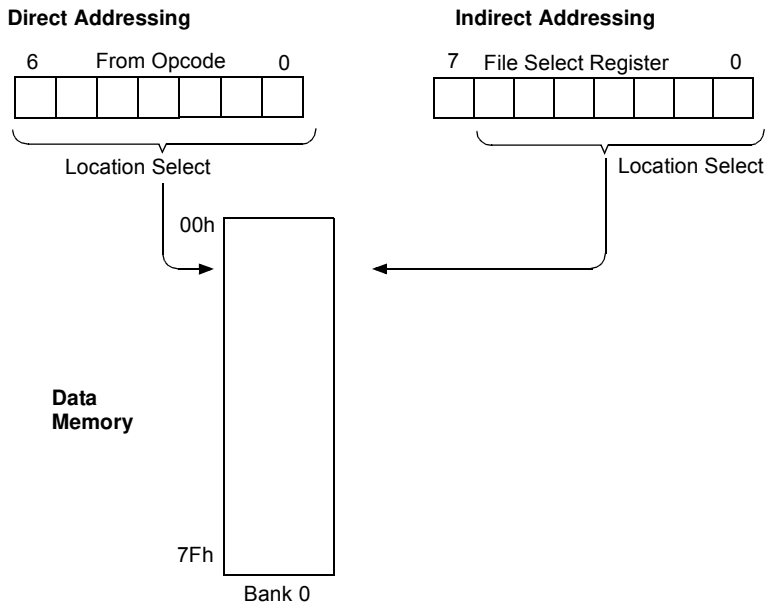
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-4.

A simple program to clear RAM location 40h-7Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
        MOVLW   0x40    ;initialize pointer
        MOVWF   FSR     ;to RAM
NEXT    CLRF    INDF    ;clear INDF register
        INCF    FSR     ;inc pointer
        BTFSS   FSR,7   ;all done?
        GOTO    NEXT    ;no clear next
CONTINUE                ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC10(L)F320/322



For memory map detail, see Figure 2-2.

3.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Word and Device ID.

3.1 Configuration Word

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word at 2007h.

3.2 Register Definitions: Configuration Word

REGISTER 3-1: CONFIG: CONFIGURATION WORD

U-1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1
—	WRT<1:0>		BORV	LPBOR	LVP
bit 13					bit 8

R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1
$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE<1:0>		BOREN<1:0>		FOSC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	P = Programmable bit

bit 13 **Unimplemented**: Read as '1'

bit 12-11 **WRT<1:0>:** Flash Memory Self-Write Protection bits
256 W Flash memory: PIC10(L)F320:
11 =Write protection off
10 =000h to 03Fh write-protected, 040h to 0FFh may be modified by PMCON control
01 =000h to 07Fh write-protected, 080h to 0FFh may be modified by PMCON control
00 =000h to 0FFh write-protected, no addresses may be modified by PMCON control
512 W Flash memory: PIC10(L)F322:
11 =Write protection off
10 =000h to 07Fh write-protected, 080h to 1FFh may be modified by PMCON control
01 =000h to 0FFh write-protected, 100h to 1FFh may be modified by PMCON control
00 =000h to 1FFh write-protected, no addresses may be modified by PMCON control

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (V_{BOR}), low trip point selected.
0 = Brown-out Reset voltage (V_{BOR}), high trip point selected.

bit 9 **LPBOR:** Low-Power Brown-out Reset Enable bit
1 = Low-power Brown-out Reset is enabled
0 = Low-power Brown-out Reset is disabled

bit 8 **LVP:** Low-Voltage Programming Enable bit
1 = Low-Voltage Programming enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$.
0 = High Voltage on $\overline{MCLR}/V_{PP}$ must be used for programming

bit 7 **$\overline{CP}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{MCLR}/V_{PP}$ Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$; Weak pull-up enabled.
0 = $\overline{MCLR}/V_{PP}$ pin function is digital input; $\overline{MCLR}$ internally disabled; Weak pull-up under control of WPUA3 bit.

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: Once enabled, code-protect can only be disabled by bulk erasing the device.
3: See V_{BOR} parameter for specific trip point voltages.

REGISTER 3-1: CONFIG: CONFIGURATION WORD (CONTINUED)

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-1 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset enabled; SBOREN bit is ignored
10 = Brown-out Reset enabled while running, disabled in Sleep; SBOREN bit is ignored
01 = Brown-out Reset controlled by the SBOREN bit in the BORCON register
00 = Brown-out Reset disabled; SBOREN bit is ignored

bit 0 **FOSC:** Oscillator Selection bit
1 = EC on CLKIN pin
0 = INTOSC oscillator I/O function available on CLKIN pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: Once enabled, code-protect can only be disabled by bulk erasing the device.
3: See VBOR parameter for specific trip point voltages.

3.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory protection are controlled independently. Internal access to the program memory and data memory are unaffected by any code protection setting.

3.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Word. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 3.4 "Write Protection"** for more information.

3.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Word define the size of the program memory block that is protected.

3.5 User ID

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 3.6 "Device ID and Revision ID"** for more information on accessing these memory locations. For more information on checksum calculation, see the "PIC10(L)F320/322 Flash Memory Programming Specification" (DS41572).

3.6 Device ID and Revision ID

The memory location 2006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See **Section 9.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

3.7 Register Definitions: Device and Revision

REGISTER 3-2: DEVID: DEVICE ID REGISTER(1)

R	R	R	R	R	R
DEV<8:3>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<2:0>			REV<4:0>				
bit 7							bit 0

Legend:	
R = Readable bit	
'1' = Bit is set	'0' = Bit is cleared

bit 13-5 **DEV<8:0>:** Device ID bits

Device	DEVID<13:0> Values	
	DEV<8:0>	REV<4:0>
PIC10F320	10 1001 101	x xxxx
PIC10LF320	10 1001 111	x xxxx
PIC10F322	10 1001 100	x xxxx
PIC10LF322	10 1001 110	x xxxx

bit 4-0 **REV<4:0>:** Revision ID bits

These bits are used to identify the revision.

Note 1: This location cannot be written.

4.0 OSCILLATOR MODULE

4.1 Overview

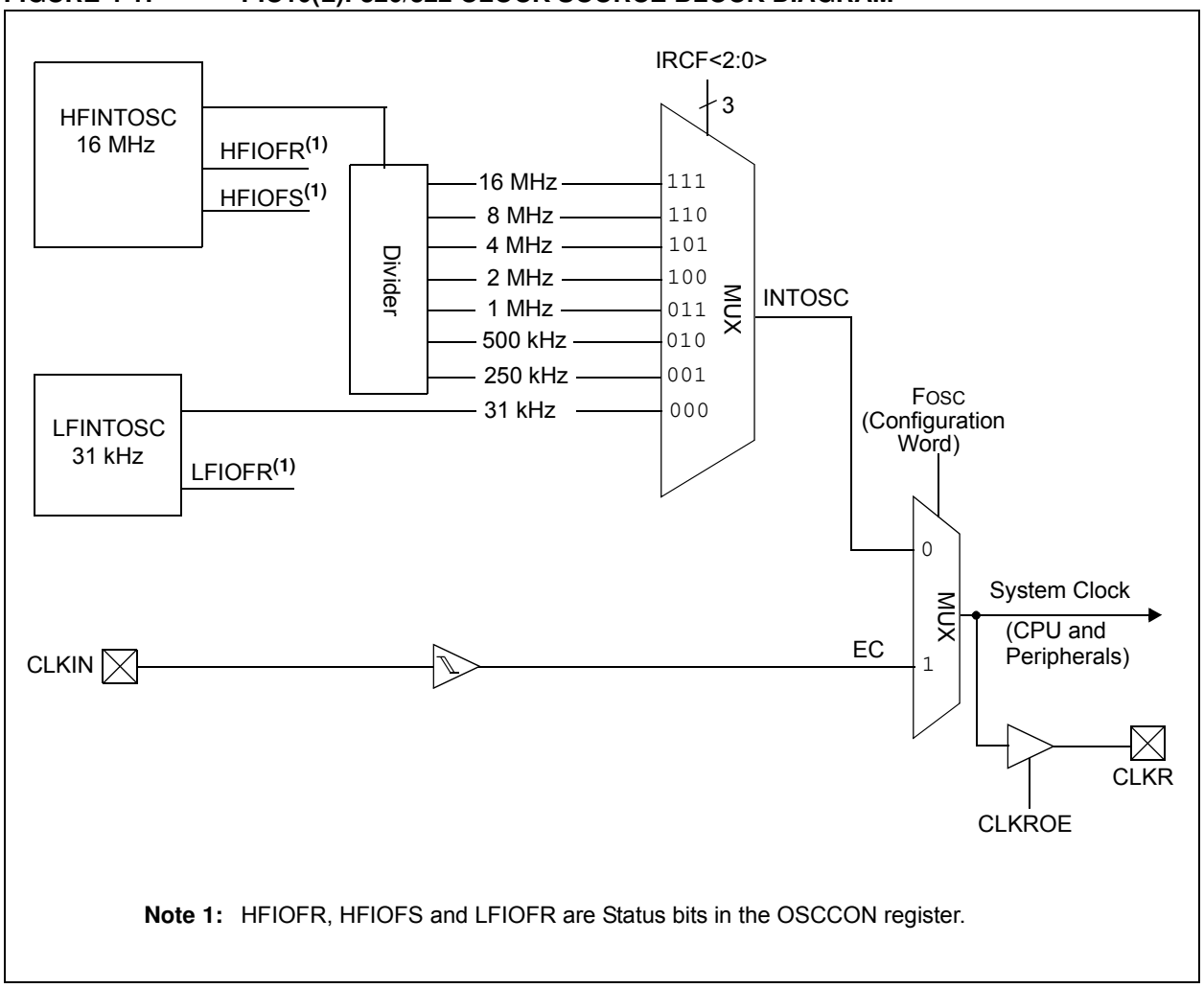
The oscillator module has a variety of clock sources and selection features that allow it to be used in a range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the oscillator module.

The system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bit in Configuration Word (CONFIG).

1. EC oscillator from CLKIN.
2. INTOSC oscillator, CLKIN not enabled.

FIGURE 4-1: PIC10(L)F320/322 CLOCK SOURCE BLOCK DIAGRAM



Note 1: HFIOFR, HFIOFS and LFIOFR are Status bits in the OSCCON register.

4.2 Clock Source Modes

Clock source modes can be classified as external or internal.

- Internal clock source (INTOSC) is contained within the oscillator module, which has eight selectable output frequencies, with a maximum internal frequency of 16 MHz.
- The External Clock mode (EC) relies on an external signal for the clock source.

The system clock can be selected between external or internal clock sources via the FOSC bit of the Configuration Word.

4.3 Internal Clock Modes

The internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate all internal system clock sources: the 16 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz (LFINTOSC).

The HFINTOSC consists of a primary and secondary clock. The secondary clock starts first with rapid start-up time, but low accuracy. The secondary clock ready signal is indicated with the HFIOFR bit of the OSCCON register. The primary clock follows with slower start-up time and higher accuracy. The primary clock is stable when the HFIOFS bit of the OSCCON register bit goes high.

4.3.1 INTOSC MODE

When the FOSC bit of the Configuration Word is cleared, the INTOSC mode is selected. When INTOSC is selected, CLKIN pin is available for general purpose I/O. See **Section 3.0 "Device Configuration"** for more information.

4.3.2 FREQUENCY SELECT BITS (IRCF)

The output of the 16 MHz HFINTOSC is connected to a divider and multiplexer (see Figure 4-1). The Internal Oscillator Frequency Select bits (IRCF) of the OSCCON register select the frequency output of the internal oscillator:

- HFINTOSC
  - 16 MHz
  - 8 MHz (default after Reset)
  - 4 MHz
  - 2 MHz
  - 1 MHz
  - 500 kHz
  - 250 kHz
- LFINTOSC
  - 31 kHz

Note:	Following any Reset, the IRCF<2:0> bits of the OSCCON register are set to '110' and the frequency selection is set to 8 MHz. The user can modify the IRCF bits to select a different frequency.

There is no delay when switching between HFINTOSC frequencies with the IRCF bits. This is because the switch involves only a change to the frequency output divider.

Start-up delay specifications are located in **Section 24.0 "Electrical Specifications"**.