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PIC12F635/PIC16F636/639
Data Sheet

8/14-Pin, Flash-Based 8-Bit CMOS Microcontrollers with nanoWatt Technology

*8-bit, 8-pin Devices Protected by Microchip's Low Pin Count Patent: U. S. Patent No. 5,847,450. Additional U.S. and foreign patents and applications may be issued or pending.

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PIC12F635/PIC16F636/639

8/14-Pin Flash-Based, 8-Bit CMOS Microcontrollers With nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Clock mode switching for low-power operation
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended Temperature range
- Power-on Reset (POR)
- Wake-up Reset (WUR)
- Independent weak pull-up/pull-down resistors
- Programmable Low-Voltage Detect (PLVD)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection (program and data independent)
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM Retention: > 40 years

Low-Power Features:

- Standby Current:
  - 1 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Peripheral Features:

- 6/12 I/O pins with individual direction control:
  - High-current source/sink for direct LED drive
  - Interrupt-on-change pin
  - Individually programmable weak pull-ups/ pull-downs
  - Ultra Low-Power Wake-up
- Analog Comparator module with:
  - Up to two analog comparators
  - Programmable On-chip Voltage Reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and outputs externally accessible
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- KEELOQ® compatible hardware Cryptographic module
- In-Circuit Serial Programming™ (ICSP™) via two pins

Low-Frequency Analog Front-End Features (PIC16F639 only):

- Three input pins for 125 kHz LF input signals
- High input detection sensitivity (3 mV_{PP}, typical)
- Demodulated data, Carrier clock or RSSI output selection
- Input carrier frequency: 125 kHz, typical
- Input modulation frequency: 4 kHz, maximum
- 8 internal Configuration registers
- Bidirectional transponder communication (LF talk back)
- Programmable antenna tuning capacitance (up to 63 pF, 1 pF/step)
- Low standby current: 5 μA (with 3 channels enabled), typical
- Low operating current: 15 μA (with 3 channels enabled), typical
- Serial Peripheral Interface (SPI) with internal MCU and external devices
- Supports Battery Back-up mode and batteryless operation with external circuits

Device	Program Memory	Data Memory		I/O	Comparators	Low Frequency Analog Front-End
	Flash (words)	SRAM (bytes)	EEPROM (bytes)			
PIC12F635	1024	64	128	6	1	N
PIC16F636	2048	128	256	12	2	N
PIC16F639	2048	128	256	12	2	Y

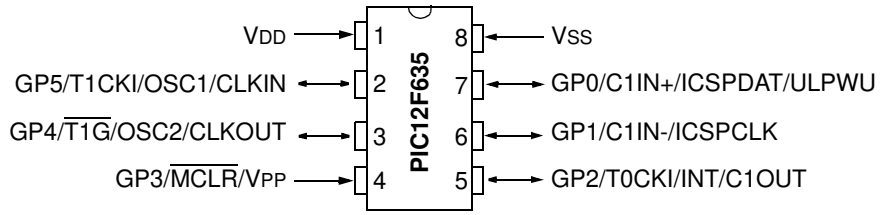
Note 1: Any references to PORTA, RAn, TRISA and TRISAn refer to GPIO, GPn, TRISIO and TRISIOn, respectively.

2: V_{DDT} is the supply voltage of the Analog Front-End section (PIC16F639 only). V_{DDT} is treated as V_{DD} in this document unless otherwise stated.

3: V_{SST} is the ground reference voltage of the Analog Front-End section (PIC16F639 only). V_{SST} is treated as V_{SS} in this document unless otherwise stated.

8-Pin Diagrams (PDIP, SOIC, DFN, DFN-S)

PDIP, SOIC



DFN, DFN-S

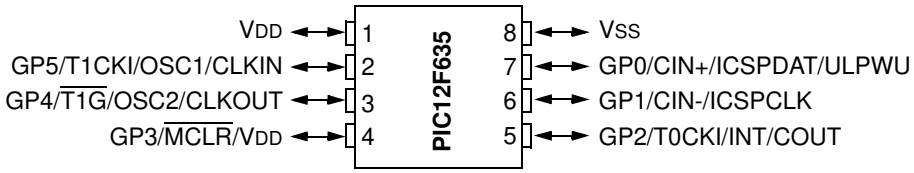


TABLE 1: 8-PIN SUMMARY (PDIP, SOIC, DFN, DFN-S)

I/O	Pin	Comparators	Timer	Interrupts	Pull-ups	Basic
GP0	7	C1IN+	—	IOC	Y	ICSPDAT/ULPWU
GP1	6	C1IN-	—	IOC	Y	ICSPCLK
GP2	5	C1OUT	T0CKI	INT/IOC	Y	—
GP3(1)	4	—	—	IOC	Y(2)	MCLR/VPP
GP4	3	—	T1G	IOC	Y	OSC2/CLKOUT
GP5	2	—	T1CKI	IOC	Y	OSC1/CLKIN
—	1	—	—	—	—	VDD
—	8	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

14-Pin Diagram (PDIP, SOIC, TSSOP)

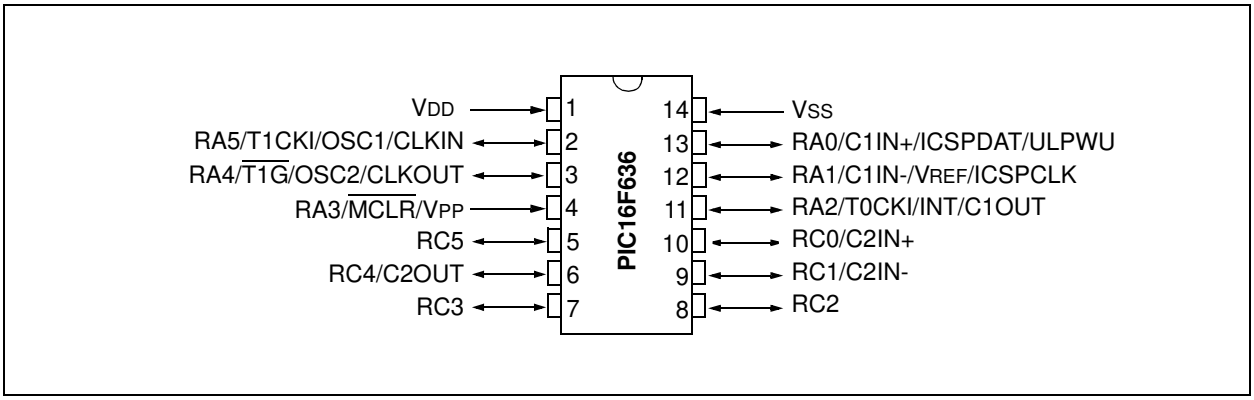


TABLE 2: 14-PIN SUMMARY (PDIP, SOIC, TSSOP)

I/O	Pin	Comparators	Timer	Interrupts	Pull-ups	Basic
RA0	13	C1IN+	—	IOC	Y	ICSPDAT/ULPWU
RA1	12	C1IN-	—	IOC	Y	VREF/ICSPCLK
RA2	11	C1OUT	T0CKI	INT/IOC	Y	—
RA3(1)	4	—	—	IOC	Y(2)	MCLR/VPP
RA4	3	—	T1G	IOC	Y	OSC2/CLKOUT
RA5	2	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	10	C2IN+	—	—	—	—
RC1	9	C2IN-	—	—	—	—
RC2	8	—	—	—	—	—
RC3	7	—	—	—	—	—
RC4	6	C2OUT	—	—	—	—
RC5	5	—	—	—	—	—
—	1	—	—	—	—	VDD
—	14	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

16-Pin Diagram

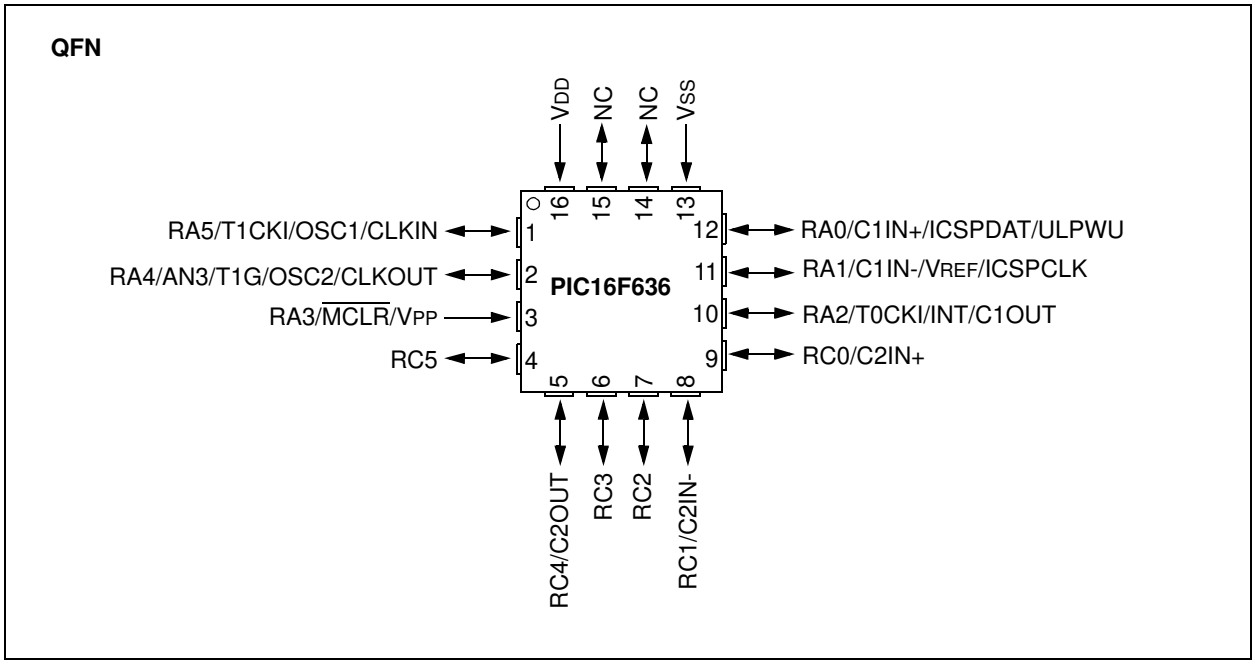


TABLE 3: 16-PIN SUMMARY

I/O	Pin	Comparators	Timer	Interrupts	Pull-ups	Basic
RA0	12	C1IN+	—	IOC	Y	ICSPDAT/ULPWU
RA1	11	C1IN-	—	IOC	Y	VREF/ICSPCLK
RA2	10	C1OUT	T0CKI	INT/IOC	Y	—
RA3(1)	3	—	—	IOC	Y(2)	$\overline{\text{MCLR}}$/VPP
RA4	2	—	$\overline{\text{T1G}}$	IOC	Y	OSC2/CLKOUT
RA5	1	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	9	C2IN+	—	—	—	—
RC1	8	C2IN-	—	—	—	—
RC2	7	—	—	—	—	—
RC3	6	—	—	—	—	—
RC4	5	C2OUT	—	—	—	—
RC5	4	—	—	—	—	—
—	16	—	—	—	—	VDD
—	13	—	—	—	—	VSS
—	14	—	—	—	—	NC
—	15	—	—	—	—	NC

Note 1: Input only.

2: Only when pin is configured for external $\overline{\text{MCLR}}$.

20-Pin Diagram

SSOP

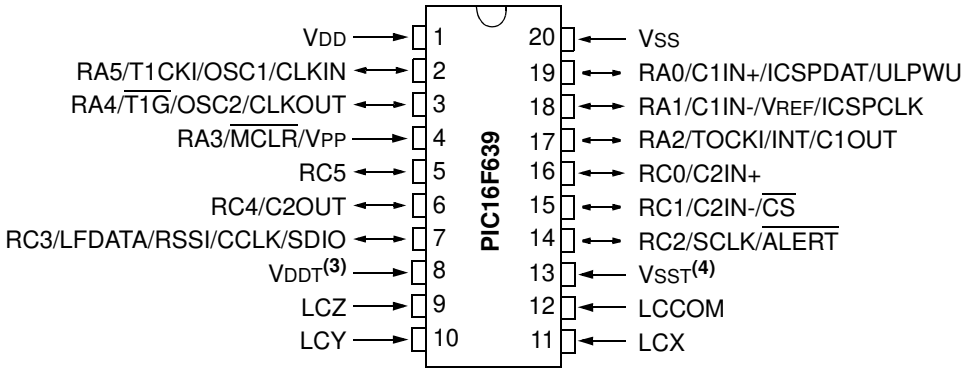


TABLE 4: 20-PIN SUMMARY

I/O	Pin	Analog Front-End	Comparators	Timer	Interrupts	Pull-ups	Basic
RA0	19	—	C1IN+	—	IOC	Y	ICSPDAT/ULPWU
RA1	18	—	C1IN-	—	IOC	Y	VREF/ICSPCLK
RA2	17	—	C1OUT	T0CKI	INT/IOC	Y	—
RA3(1)	4	—	—	—	IOC	Y(2)	MCLR/VPP
RA4	3	—	—	T1G	IOC	Y	OSC2/CLKOUT
RA5	2	—	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	16	—	C2IN+	—	—	—	—
RC1	15	—	C2IN-	—	—	—	CS
RC2	14	ALERT	—	—	—	—	SCLK
RC3	7	LFDATA/RSSI	—	—	—	—	CCLK/SDIO
RC4	6	—	C2OUT	—	—	—	—
RC5	5	—	—	—	—	—	—
—	8	—	—	—	—	—	VDDT(3)
—	13	—	—	—	—	—	VSST(4)
—	11	LCX	—	—	—	—	—
—	10	LCY	—	—	—	—	—
—	9	LCZ	—	—	—	—	—
—	12	LCCOM	—	—	—	—	—
—	1	—	—	—	—	—	VDD
—	20	—	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

3: VDDT is the supply voltage of the Analog Front-End section (PIC16F639 only). VDDT is treated as VDD in this document unless otherwise stated.

4: VSST is the ground reference voltage of the Analog Front-End section (PIC16F639 only). VSST is treated as VSS in this document unless otherwise stated.

Table of Contents

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC12F635/PIC16F636/639 devices.

Block Diagrams and pinout descriptions of the devices are as follows:

- PIC12F635 (Figure 1-1, Table 1-1)
- PIC16F636 (Figure 1-2, Table 1-2)
- PIC16F639 (Figure 1-3, Table 1-3)

FIGURE 1-1: PIC12F635 BLOCK DIAGRAM

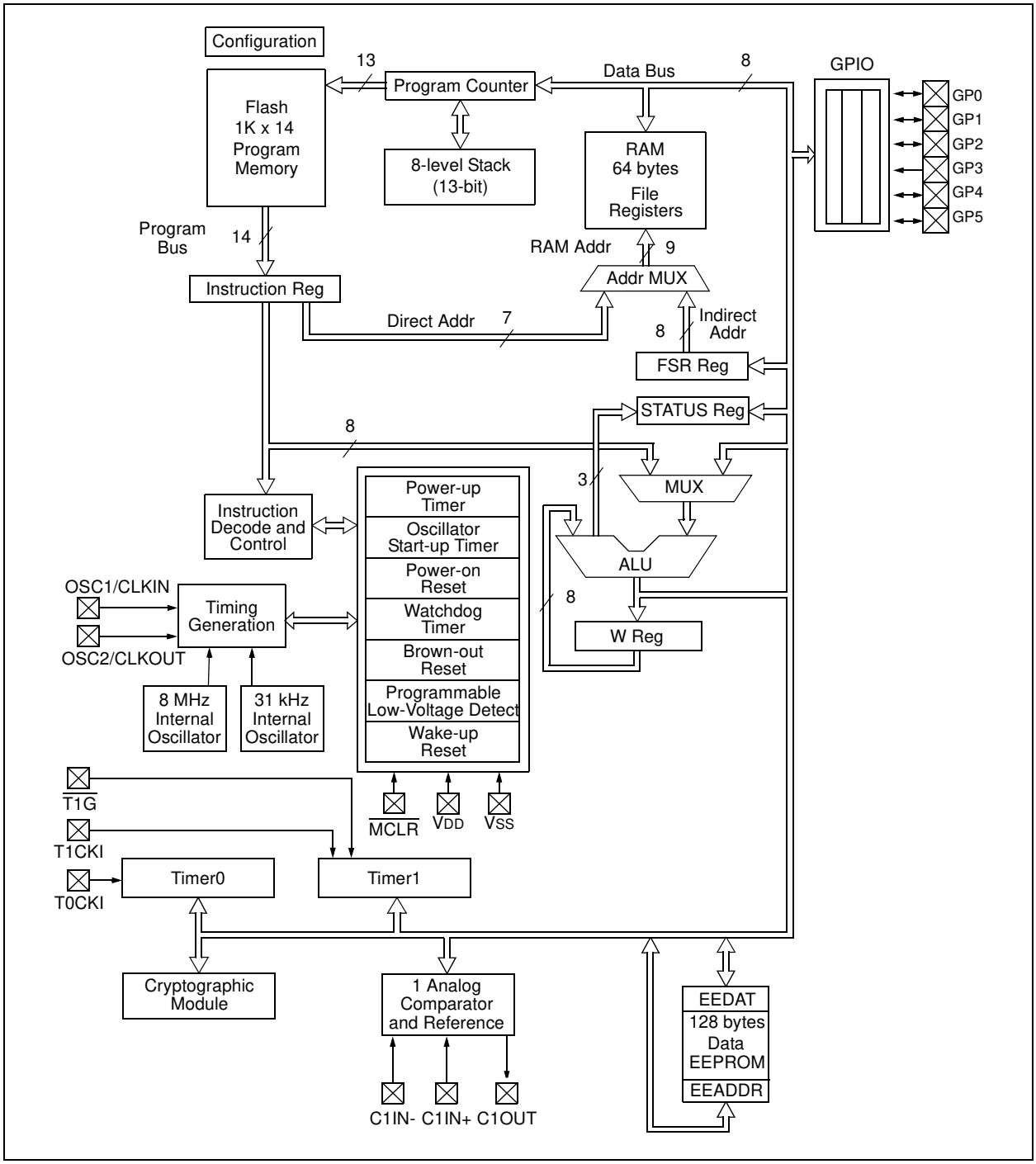


FIGURE 1-2: PIC16F636 BLOCK DIAGRAM

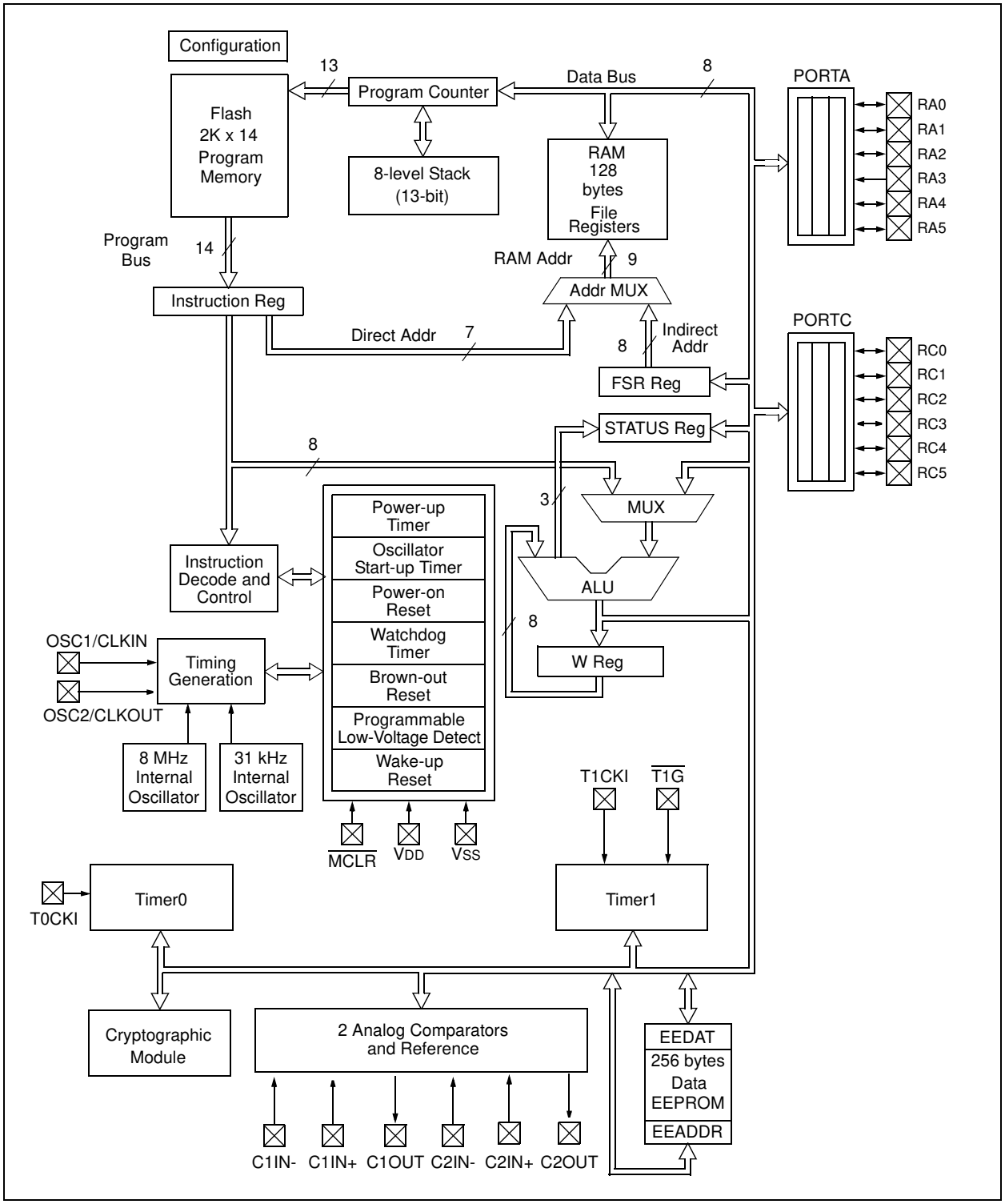


FIGURE 1-3: PIC16F639 BLOCK DIAGRAM

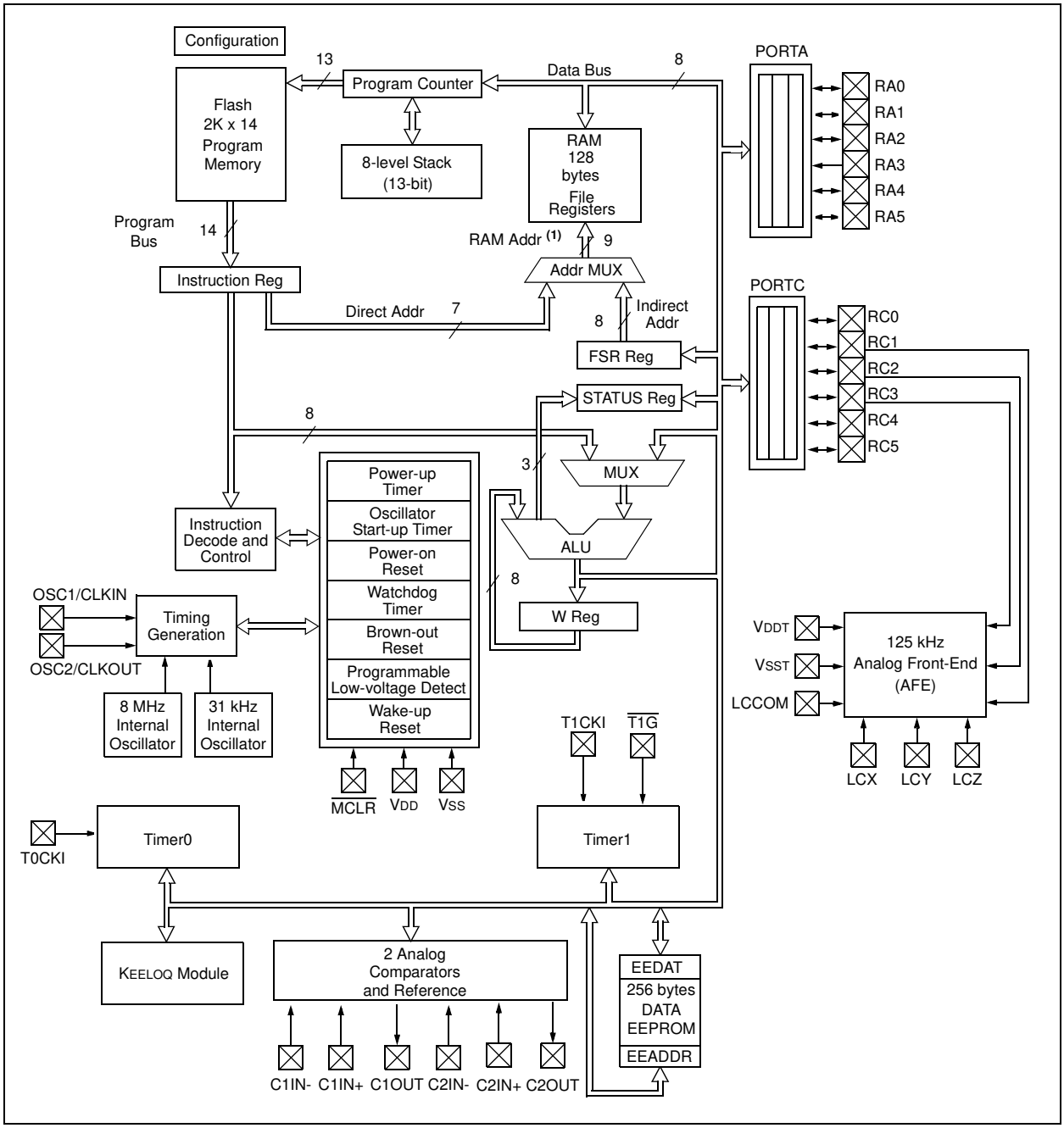


TABLE 1-1: PIC12F635 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
GP0/C1IN+/ICSPDAT/ULPWU	GP0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator 1 input – positive.
	ICSPDAT	TTL	CMOS	Serial programming data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
GP1/C1IN-/ICSPCLK	GP1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator 1 input – negative.
	ICSPCLK	ST	—	Serial programming clock.
GP2/T0CKI/INT/C1OUT	GP2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator 1 output.
GP3/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
GP4/$\overline{\text{T1G}}$/OSC2/CLKOUT	GP4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC/4 reference clock.
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC reference clock.
VDD	VDD	D	—	Power supply for microcontroller.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct
HV = High Voltage; ST = Schmitt Trigger input with CMOS levels
TTL = TTL compatible input; XTAL = Crystal

TABLE 1-2: PIC16F636 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
RA0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator 1 input – positive.
	ICSPDAT	TTL	CMOS	Serial programming data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator 1 input – negative.
	VREF	AN	—	External voltage reference
	ICSPCLK	ST	—	Serial programming clock.
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator 1 output.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC/4 reference clock.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC reference clock.
RC0/C2IN+	RC0	TTL	CMOS	General purpose I/O.
	C2IN+	AN	—	Comparator 1 input – positive.
RC1/C2IN-	RC1	TTL	CMOS	General purpose I/O.
	C2IN-	AN	—	Comparator 1 input – negative.
RC2	RC2	TTL	CMOS	General purpose I/O.
RC3	RC3	TTL	CMOS	General purpose I/O.
RC4/C2OUT	RC4	TTL	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator 2 output.
RC5	RC5	TTL	CMOS	General purpose I/O.
VDD	VDD	D	—	Power supply for microcontroller.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct
HV = High Voltage; ST = Schmitt Trigger input with CMOS levels
TTL = TTL compatible input; XTAL = Crystal

TABLE 1-3: PIC16F639 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
LCCOM	LCCOM	AN	—	Common reference for analog inputs.
LCX	LCX	AN	—	125 kHz analog X channel input.
LCY	LCY	AN	—	125 kHz analog Y channel input.
LCZ	LCZ	AN	—	125 kHz analog Z channel input.
RA0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator1 input – positive.
	ICSPDAT	TTL	CMOS	Serial Programming Data IO.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator1 input – negative.
	VREF	AN	—	External voltage reference
	ICSPCLK	ST	—	Serial Programming Clock.
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External Interrupt.
	C1OUT	—	CMOS	Comparator1 output.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC reference clock.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC/4 reference clock.
RC0/C2IN+	RC0	TTL	CMOS	General purpose I/O.
	C2IN+	AN	—	Comparator1 input – positive.
RC1/C2IN-/$\overline{\text{CS}}$	RC1	TTL	CMOS	General purpose I/O.
	C2IN-	AN	—	Comparator1 input – negative.
	$\overline{\text{CS}}$	TTL	—	Chip select input for SPI communication with internal pull-up resistor.
RC2/SCLK/$\overline{\text{ALERT}}$	RC2	TTL	CMOS	General purpose I/O.
	SCLK	TTL	—	Digital clock input for SPI communication.
	$\overline{\text{ALERT}}$	—	OD	Output with internal pull-up resistor for AFE error signal.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct
HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; OD = Open Drain
TTL = TTL compatible input; XTAL = Crystal

TABLE 1-3: PIC16F639 PINOUT DESCRIPTIONS (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC3/LFDATA/RSSI/CCLK/SDO	RC3	TTL	CMOS	General purpose I/O.
	LFDATA	—	CMOS	Digital output representation of analog input signal to LC pins.
	RSSI	—	Current	Received signal strength indicator. Analog current that is proportional to input amplitude.
	CCLK	—	—	Carrier clock output.
	SDIO	TTL	CMOS	Input/Output for SPI communication.
RC4/C2OUT	RC4	TTL	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator2 output.
RC5	RC5	TTL	CMOS	General purpose I/O.
VDDT	VDDT	D	—	Power supply for Analog Front-End. In this document, VDDT is treated the same as VDD, unless otherwise stated.
VSST	VSST	D	—	Ground reference for Analog Front-End. In this document, VSST is treated the same as VSS, unless otherwise stated.
VDD	VDD	D	—	Power supply for microcontroller.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct
HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; OD = Open Drain
TTL = TTL compatible input; XTAL = Crystal

NOTES:

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F635/PIC16F636/639 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh, for the PIC12F635) and 2K x 14 (0000h-07FFh, for the PIC16F636/639) is physically implemented. Accessing a location above these boundaries will cause a wraparound within the first 2K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are GPRs, implemented as static RAM for the PIC16F636/639. For the PIC12F635, register locations 40h through 7Fh are GPRs implemented as static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. RP0 of the STATUS register is the bank select bit.

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK OF THE PIC12F635

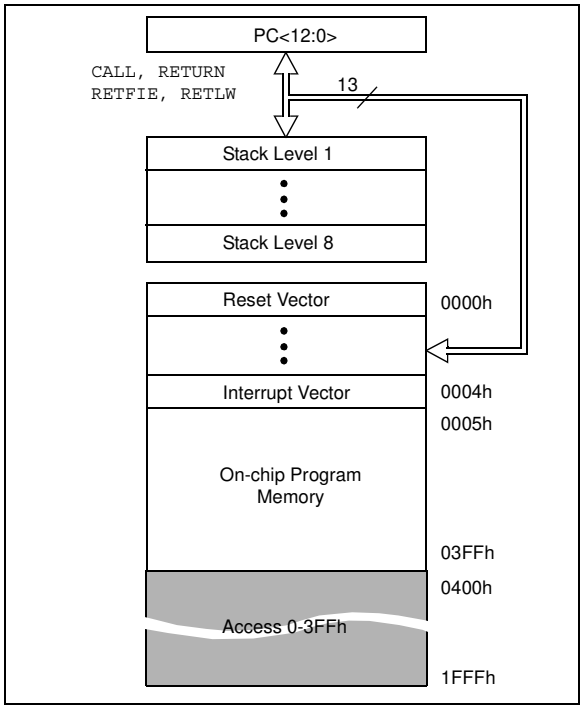
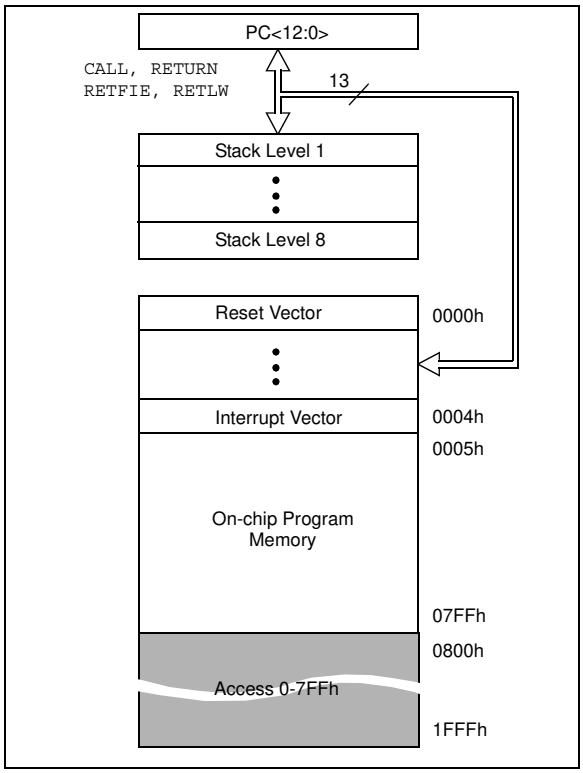


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK OF THE PIC16F636/639



2.2.1 GENERAL PURPOSE REGISTER

The register file is organized as 64 x 8 for the PIC12F635 and 128 x 8 for the PIC16F636/639. Each register is accessed, either directly or indirectly, through the File Select Register, FSR (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Figure 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-3: PIC12F635 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
GPIO	05h	TRISIO	85h		105h		185h
	06h		86h		106h		186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
	3Fh						
General Purpose Register 64 Bytes	40h		EFh		16Fh		1EFh
	7Fh	Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
			FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> registers are KEELOQ® hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

FIGURE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr. (1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
PORTA	05h	TRISA	85h		105h		185h
	06h		86h		106h		186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			C0h				
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> registers are KEELOQ hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

TABLE 2-1: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
01h	TMR0	Timer0 Module Register								xxxx xxxx	61,137
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xx00	47,137
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(2)	0000 000x	28,137
0Ch	PIR1	EEIF	LVDIF	CRIF	—	C1IF	OSFIF	—	TMR1IF	000- 00-0	30,137
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	68,137
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	144,137
19h	CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	79,137
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	82,137
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	—	Unimplemented								—	—
1Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

TABLE 2-2: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	63,137
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(3)	0000 000x	28,137
8Ch	PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	29,137
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	$\overline{WUR}$	—	$\overline{POR}$	$\overline{BOR}$	--01 q-qq	31,137
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	36,137
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	40,137
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA(2)	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA(2)	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: GP3 pull-up is enabled when pin is configured as $\overline{MCLR}$ in the Configuration Word register.

3: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset, but will set again if the mismatch exists.

TABLE 2-3: PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
01h	TMR0	Timer0 Module Register								xxxx xxxx	61,137
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xx00	48,137
06h	—	Unimplemented								—	—
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xx00	57,137
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(2)	0000 000x	28,137
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF	C1IF	OSFIF	—	TMR1IF	0000 00-0	30,137
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	68,137
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	144,137
19h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	79,137
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	82,137
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	—	Unimplemented								—	—
1Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.