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PIC16C505

14-Pin, 8-Bit CMOS Microcontroller

Device included in this Data Sheet:

PIC16C505

High-Performance RISC CPU:

- Only 33 instructions to learn
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle

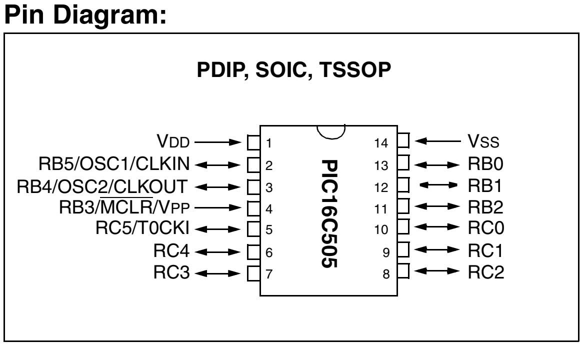
Device	Memory	
	Program	Data
PIC16C505	1024 x 12	72 x 8

- Direct, indirect and relative addressing modes for data and instructions
- 12-bit wide instructions
- 8-bit wide data path
- 2-level deep hardware stack
- Eight special function hardware registers
- Direct, indirect and relative addressing modes for data and instructions
- All single cycle instructions (200 ns) except for program branches which are two-cycle

Peripheral Features:

- 11 I/O pins with individual direction control
- 1 input pin
- High current sink/source for direct LED drive
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagram:



Special Microcontroller Features:

- In-Circuit Serial Programming (ICSP™)
- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with dedicated on-chip RC oscillator for reliable operation
- Programmable Code Protection
- Internal weak pull-ups on I/O pins
- Wake-up from Sleep on pin change
- Power-saving Sleep mode
- Selectable oscillator options:
  - INTRC: Precision internal 4 MHz oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High speed crystal/resonator
  - LP: Power saving, low frequency crystal

CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range (2.5V to 5.5V)
- Wide temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
  - < 1.0 μA typical standby current @ 5V
- Low power consumption
  - < 2.0 mA @ 5V, 4 MHz
  - 15 μA typical @ 3.0V, 32 kHz for TMR0 running in SLEEP mode
  - < 1.0 μA typical standby current @ 5V

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1.0 GENERAL DESCRIPTION

The PIC16C505 from Microchip Technology is a low-cost, high-performance, 8-bit, fully static, EPROM/ROM-based CMOS microcontroller. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 μs) except for program branches, which take two cycles. The PIC16C505 delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C505 product is equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are five oscillator configurations to choose from, including INTRC internal oscillator mode and the power-saving LP (Low Power) oscillator mode. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC16C505 is available in the cost-effective One-Time-Programmable (OTP) version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C505 product is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16C505 fits in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The EPROM technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller perfect for applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16C505 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic and PLD's in larger systems, and coprocessor applications).

TABLE 1-1: PIC16C505 DEVICE

		PIC16C505
Clock	Maximum Frequency of Operation (MHz)	20
Memory	EPROM Program Memory	1024
	Data Memory (bytes)	72
Peripherals	Timer Module(s)	TMR0
	Wake-up from SLEEP on pin change	Yes
Features	I/O Pins	11
	Input Pins	1
	Internal Pull-ups	Yes
	In-Circuit Serial Programming	Yes
	Number of Instructions	33
	Packages	14-pin DIP, SOIC, TSSOP

The PIC16C505 device has Power-on Reset, selectable Watchdog Timer, selectable code protect, high I/O current capability and precision internal oscillator.
The PIC16C505 device uses serial programming with data pin RB0 and clock pin RB1.

2.0 PIC16C505 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C505 Product Identification System at the back of this data sheet to specify the correct part number.

2.1 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility of frequent code updates or small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.2 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program medium to high quantity units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.3 Serialized Quick-Turnaround Production (SQTP^{SM}) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry-code, password or ID number.

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C505 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C505 uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The Table below lists program memory (EPROM) and data memory (RAM) for the PIC16C505.

Device	Memory	
	Program	Data
PIC16C505	1024 x 12	72 x 8

The PIC16C505 can directly or indirectly address its register files and data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16C505 has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of ‘special optimal situations’ make programming with the PIC16C505 simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C505 device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

FIGURE 3-1: PIC16C505 BLOCK DIAGRAM

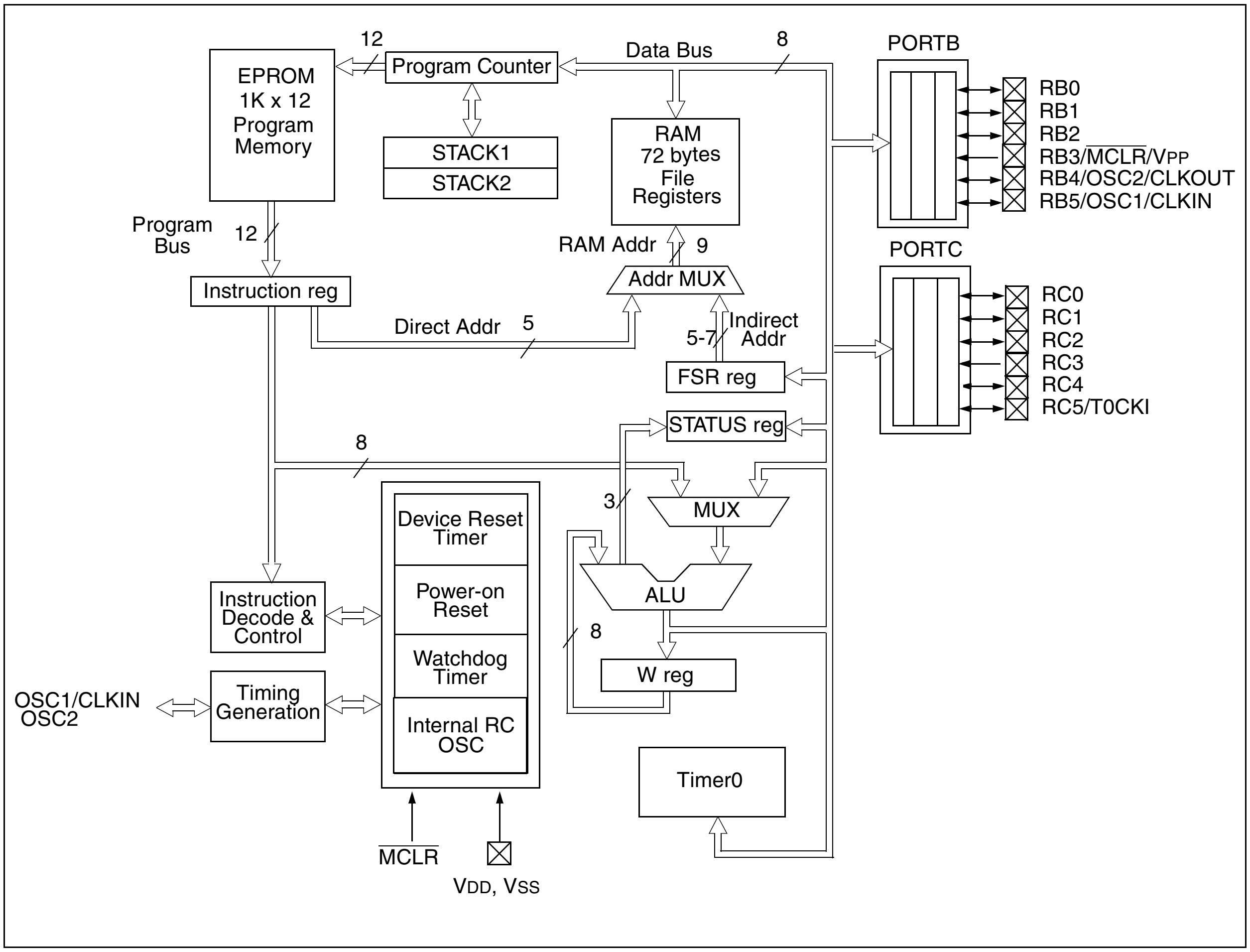


TABLE 3-1: PIC16C505 PINOUT DESCRIPTION

Name	DIP Pin #	SOIC Pin #	I/O/P Type	Buffer Type	Description
RB0	13	13	I/O	TTL/ST	Bi-directional I/O port/ serial programming data. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
RB1	12	12	I/O	TTL/ST	Bi-directional I/O port/ serial programming clock. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
RB2	11	11	I/O	TTL	Bi-directional I/O port.
RB3/$\overline{\text{MCLR}}$/VPP	4	4	I	TTL/ST	Input port/master clear (reset) input/programming voltage input. When configured as $\overline{\text{MCLR}}$, this pin is an active low reset to the device. Voltage on $\overline{\text{MCLR}}$/VPP must not exceed VDD during normal device operation. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. Weak pull-up only when configured as RB3. ST when configured as $\overline{\text{MCLR}}$.
RB4/OSC2/CLKOUT	3	3	I/O	TTL	Bi-directional I/O port/oscillator crystal output. Connections to crystal or resonator in crystal oscillator mode (XT and LP modes only, RB4 in other modes). Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. In EXTRC and INTRC modes, the pin output can be configured to CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RB5/OSC1/CLKIN	2	2	I/O	TTL/ST	Bidirectional IO port/oscillator crystal input/external clock source input (RB5 in Internal RC mode only, OSC1 in all other oscillator modes). TTL input when RB5, ST input in external RC oscillator mode.
RC0	10	10	I/O	TTL	Bi-directional I/O port.
RC1	9	9	I/O	TTL	Bi-directional I/O port.
RC2	8	8	I/O	TTL	Bi-directional I/O port.
RC3	7	7	I/O	TTL	Bi-directional I/O port.
RC4	6	6	I/O	TTL	Bi-directional I/O port.
RC5/T0CKI	5	5	I/O	ST	Bi-directional I/O port. Can be configured as T0CKI.
VDD	1	1	P	—	Positive supply for logic and I/O pins
VSS	14	14	P	—	Ground reference for logic and I/O pins

Legend: I = input, O = output, I/O = input/output, P = power, — = not used, TTL = TTL input,
ST = Schmitt Trigger input

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

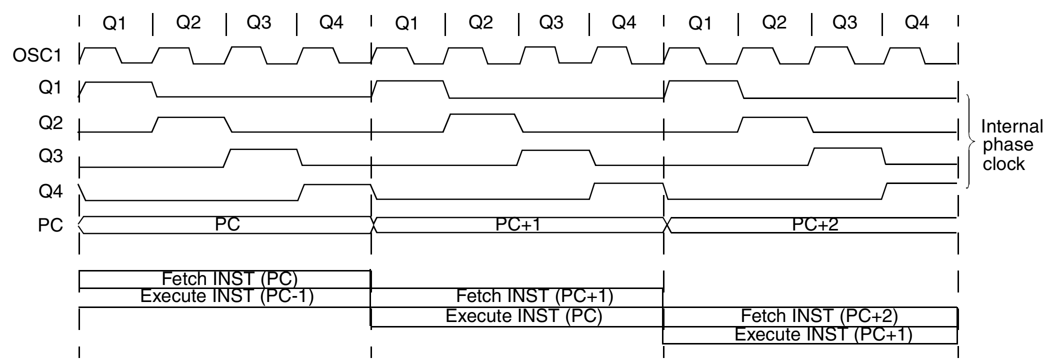
3.2 Instruction Flow/Pipelining

An Instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., `GOTO`) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

1. `MOVLW 03H`	Fetch 1	Execute 1				
2. `MOVWF PORTB`		Fetch 2	Execute 2			
3. `CALL SUB_1`			Fetch 3	Execute 3		
4. `BSF PORTB, BIT1`				Fetch 4	Flush	
					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

4.0 MEMORY ORGANIZATION

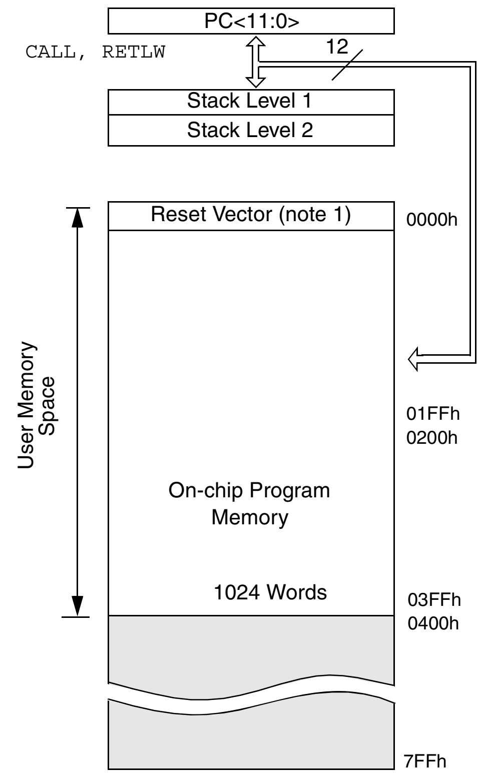
PIC16C505 memory is organized into program memory and data memory. For the PIC16C505, a paging scheme is used. Program memory pages are accessed using one STATUS register bit. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization

The PIC16C505 devices have a 12-bit Program Counter (PC).

The 1K x 12 (0000h-03FFh) for the PIC16C505 are physically implemented. Refer to Figure 4-1. Accessing a location above this boundary will cause a wrap-around within the first 1K x 12 space. The effective reset vector is at 0000h, (see Figure 4-1). Location 03FFh contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C505



Note 1: Address 0000h becomes the effective reset vector. Location 03FFh contains the `MOVLW XX` INTERNAL RC oscillator calibration value.

4.2 Data Memory Organization

Data memory is composed of registers or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PCL), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Function Registers are used to control the I/O port configuration and prescaler options.

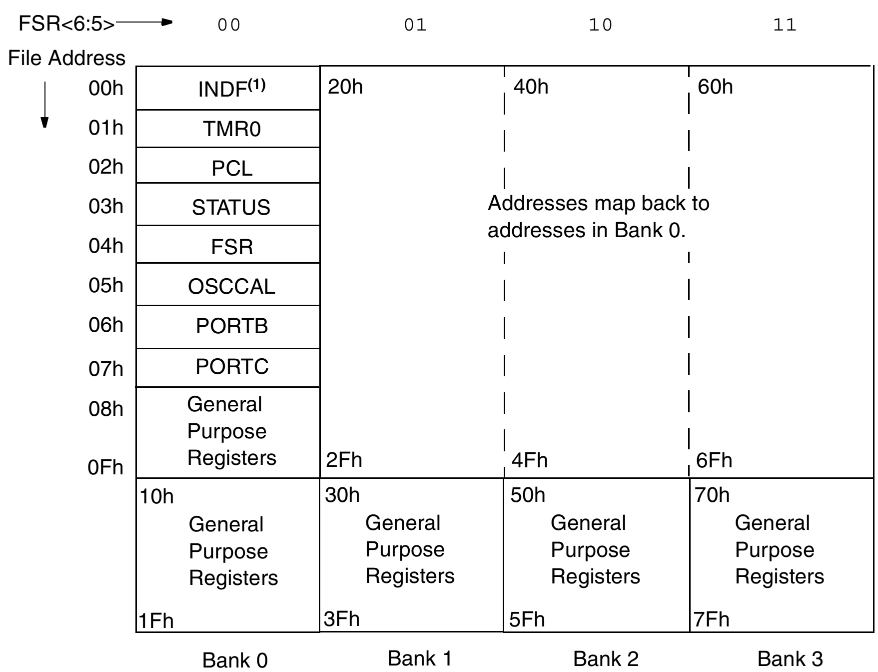
The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C505, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and 48 General Purpose Registers that may be addressed using a banking scheme (Figure 4-2).

4.2.1 GENERAL PURPOSE REGISTER FILE

The General Purpose Register file is accessed, either directly or indirectly, through the File Select Register FSR (Section 4.8).

FIGURE 4-2: PIC16C505 REGISTER FILE MAP



Note 1: Not a physical register.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets(2)
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	RBWUF	—	PAO	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	q00q quuu(1)
04h	FSR	Indirect data memory address pointer								110x xxxx	11uu uuuu
05h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	uuuu uu--
N/A	TRISB	—	—	I/O control registers						--11 1111	--11 1111
N/A	TRISC	—	—	I/O control registers						--11 1111	--11 1111
N/A	OPTION	$\overline{RBWU}$	$\overline{RBPU}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other rests will cause bit 7 = 0.

Note 2: Other (non-power-up) resets include external reset through $\overline{MCLR}$, watchdog timer and wake-up on pin change reset.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register, because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Instruction Set Summary.

REGISTER 4-1: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
RBWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **RBWUF**: I/O reset bit
1 = Reset due to wake-up from SLEEP on pin change
0 = After power up or other reset

bit 6: **Unimplemented**

bit 5: **PA0**: Program page preselect bits
1 = Page 1 (200h - 3FFh)
0 = Page 0 (000h - 1FFh)
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSB or MSB, respectively
0 = A carry did not occur	0 = A borrow occurred	

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

> **Note:** If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides OPTION control of $\overline{\text{RBPU}}$ and $\overline{\text{RBWU}}$).

REGISTER 4-2: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBWU}}$:** Enable wake-up on pin change (RB0, RB1, RB3, RB4)
1 = Disabled
0 = Enabled

bit 6: **$\overline{\text{RBPU}}$**: Enable weak pull-ups (RB0, RB1, RB3, RB4)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin (overrides TRIS <RC57>
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>:** Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal 4 MHz oscillator. It contains six bits for calibration

> **Note:** Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part, so it can be reprogrammed correctly later.

After you move in the calibration constant, do not change the value. See Section 7.2.5

REGISTER 4-3: OSCCAL REGISTER (ADDRESS 05h) PIC16C505

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7-2: **CAL<5:0>:** Calibration

bit 1-0: Unimplemented read as ‘0’

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

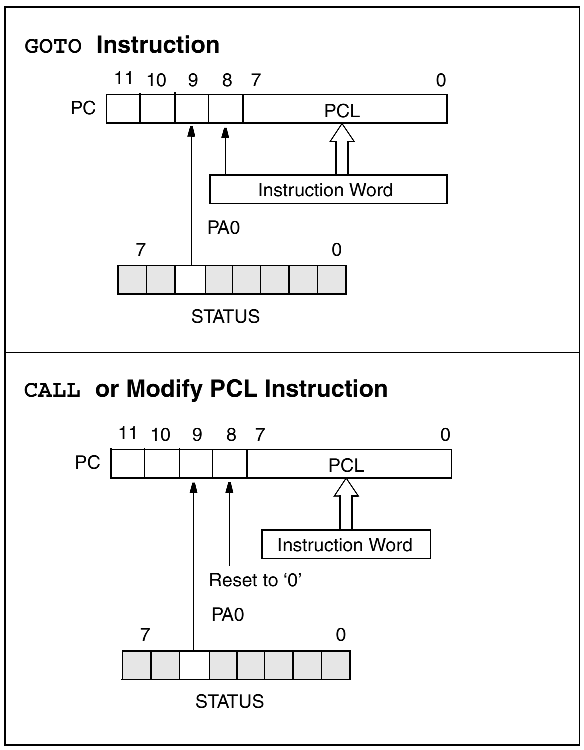
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-3).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-3).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC,5.

Note:	Because PC<8> is cleared in the CALL instruction or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-3: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C505



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction.) After executing MOVLW XX, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

PIC16C505 devices have a 12-bit wide hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Note 1:	There are no STATUS bits to indicate stack overflows or stack underflow conditions.
Note 2:	There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETLW, and instructions.

4.8 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

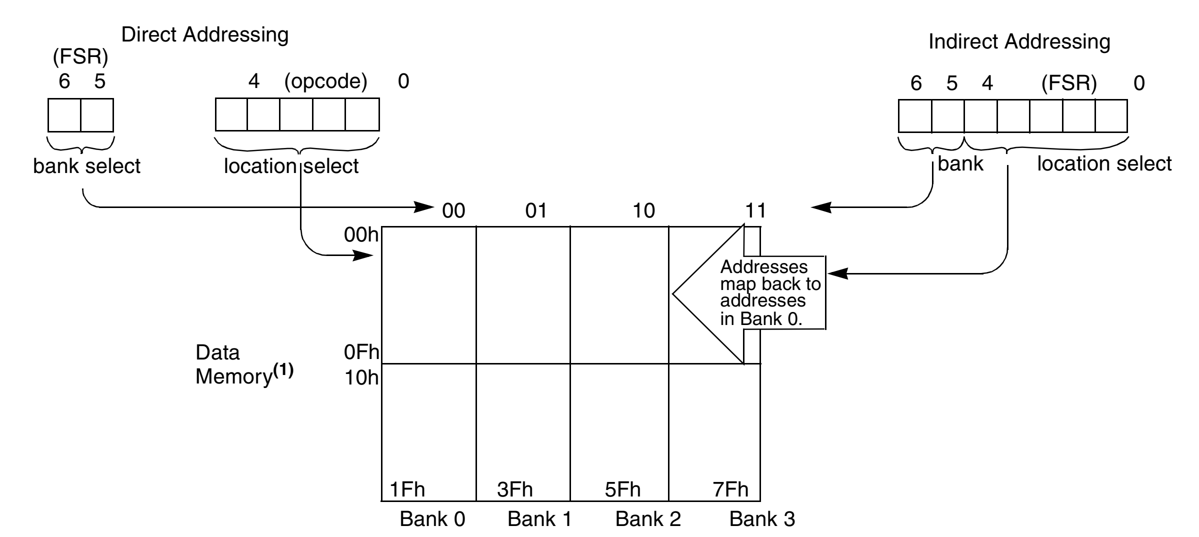
```
            movlw   0x10     ;initialize pointer
            movwf   FSR      ; to RAM
NEXT        clrf    INDF     ;clear INDF register
            incf    FSR,F    ;inc pointer
            btfsc   FSR,4    ;all done?
            goto    NEXT     ;NO, clear next
CONTINUE
            :                ;YES, continue
            :
```

The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

The device uses FSR<6:5> to select between banks 0:3.

FIGURE 4-4: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

5.0 I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers are all set.

5.1 PORTB

PORTB is an 8-bit I/O register. Only the low order 6 bits are used (RB<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that RB3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during port read. Pins RB0, RB1, RB3 and RB4 can be configured with weak pull-ups and also with wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If pin 4 is configured as $\overline{\text{MCLR}}$, weak pull-up is always off and wake-up on change for this pin is not enabled.

5.2 PORTC

PORTC is an 8-bit I/O register. Only the low order 6 bits are used (RC<5:0>). Bits 7 and 6 are unimplemented and read as '0's.

5.3 TRIS Registers

The output driver control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are RB3, which is input only, and RC5, which may be controlled by the option register. See Register 4-2.

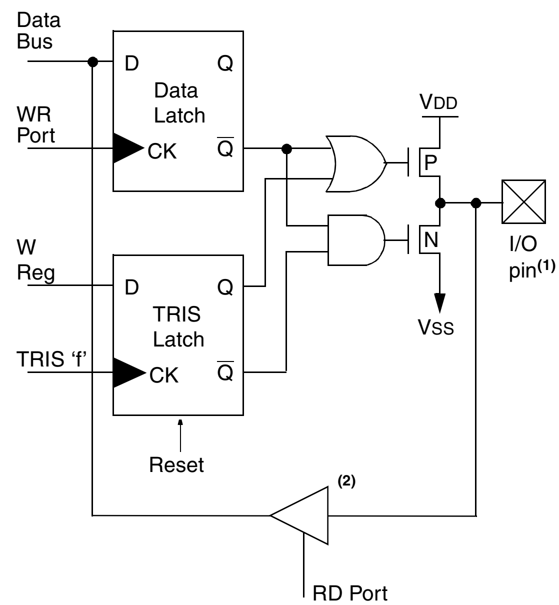
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.4 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins except RB3, which is input only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB,W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except RB3) can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

Note 2: See Table 3-1 for buffer type.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISB	—	—	I/O control registers						--11 1111	--11 1111
N/A	TRISC	—	—	I/O control registers						--11 1111	--11 1111
N/A	OPTION	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS	RBWUF	—	PAO	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	q00q quuu(1)
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as ‘0’, — = unimplemented, read as ‘0’, x = unknown, u = unchanged, q = depends on condition.

Note 1: If reset was due to wake-up on pin change, then bit 7 = 1. All other rests will cause bit 7 = 0.

5.5 I/O Programming Considerations

5.5.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin (“wired-or”, “wired-and”). The resulting high output currents may damage the chip.

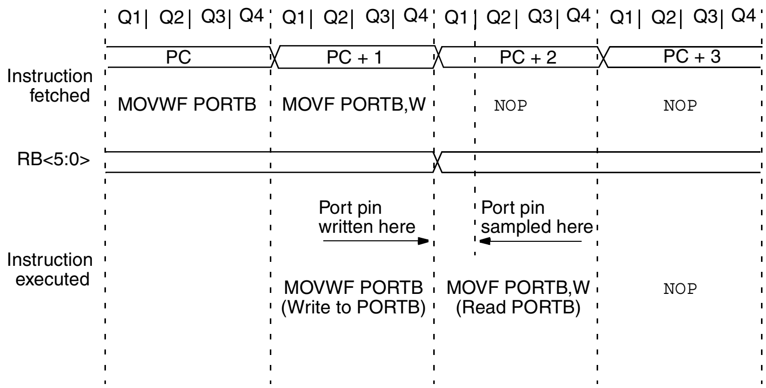
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORTB Settings
; PORTB<5:3> Inputs
; PORTB<2:0> Outputs
;
;                    PORTB latch  PORTB pins
;                    ----------  ----------
  BCF   PORTB, 5     ;--01 -ppp   --11 pppp
  BCF   PORTB, 4     ;--10 -ppp   --11 pppp
  MOVLW 007h         ;
  TRIS  PORTB        ;--10 -ppp   --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;RB5 to be latched as the pin value (High).
```

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



This example shows a write to PORTB followed by a read from PORTB.

Data setup time = (0.25 T_{CY} – T_{PD})

where: T_{CY} = instruction cycle.

T_{PD} = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

NOTES:

6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

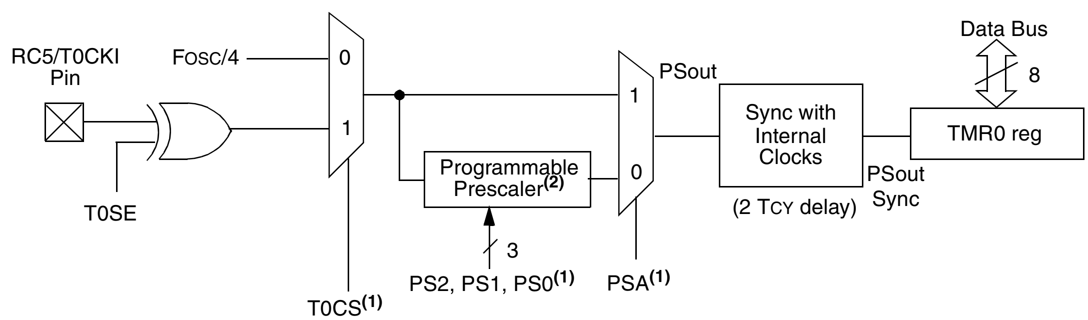
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

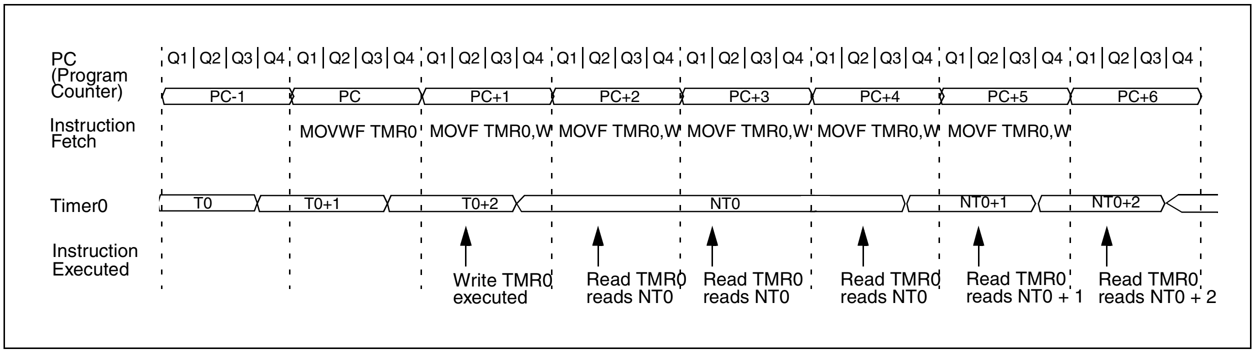


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

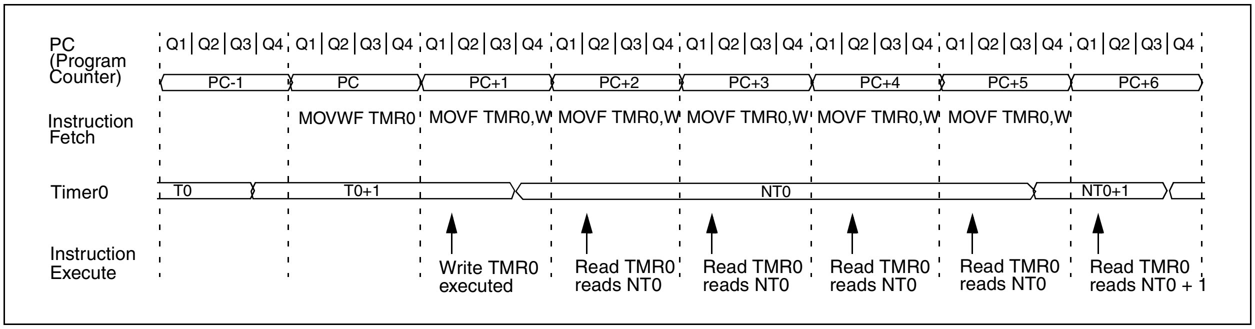


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	TRISC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--11 1111	--11 1111

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged.

6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

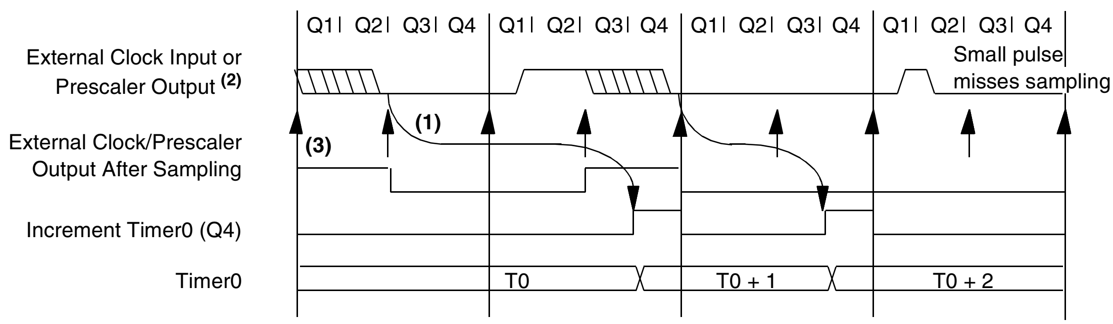
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.

2: External clock if no prescaler selected; prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.