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PIC16C6X

8-Bit CMOS Microcontrollers

Devices included in this data sheet:

- PIC16C61
- PIC16C62
- PIC16C62A
- PIC16CR62
- PIC16C63
- PIC16CR63
- PIC16C64
- PIC16C64A
- PIC16CR64
- PIC16C65
- PIC16C65A
- PIC16CR65
- PIC16C66
- PIC16C67

PIC16C6X Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide operating voltage range: 2.5V to 6.0V
- Commercial, Industrial, and Extended temperature ranges
- Low-power consumption:
  - < 2 mA @ 5V, 4 MHz
  - 15 μA typical @ 3V, 32 kHz
  - < 1 μA typical standby current

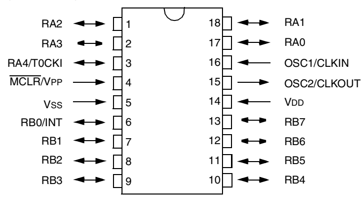
PIC16C6X Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture/Compare/PWM (CCP) module(s)
- Capture is 16-bit, max resolution is 12.5 ns, Compare is 16-bit, max resolution is 200 ns, PWM max resolution is 10-bit.
- Synchronous Serial Port (SSP) with SPI and I^{2}C™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC16C6X Features	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
Program Memory (EPROM) x 14	1K	2K	2K	—	4K	—	2K	2K	—	4K	4K	—	8K	8K
(ROM) x 14	—	—	—	2K	—	4K	—	—	2K	—	—	4K	—	—
Data Memory (Bytes) x 8	36	128	128	128	192	192	128	128	128	192	192	192	368	368
I/O Pins	13	22	22	22	22	22	33	33	33	33	33	33	22	33
Parallel Slave Port	—	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	—	Yes
Capture/Compare/PWM Module(s)	—	1	1	1	2	2	1	1	1	2	2	2	2	2
Timer Modules	1	3	3	3	3	3	3	3	3	3	3	3	3	3
Serial Communication	—	SPI/ I^{2}C	SPI/ I^{2}C	SPI/ I^{2}C	SPI/I^{2}C, USART	SPI/I^{2}C, USART	SPI/ I^{2}C	SPI/ I^{2}C	SPI/ I^{2}C	SPI/I^{2}C, USART	SPI/I^{2}C, USART	SPI/I^{2}C, USART	SPI/I^{2}C, USART	SPI/I^{2}C, USART
In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset	—	—	Yes	Yes	Yes	Yes	—	Yes	Yes	—	Yes	Yes	Yes	Yes
Interrupt Sources	3	7	7	7	10	10	8	8	8	11	11	11	10	11
Sink/Source Current (mA)	25/20	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25

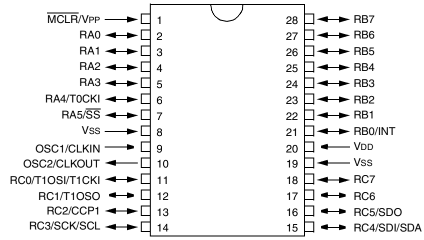
Pin Diagrams

PDIP, SOIC, Windowed CERDIP



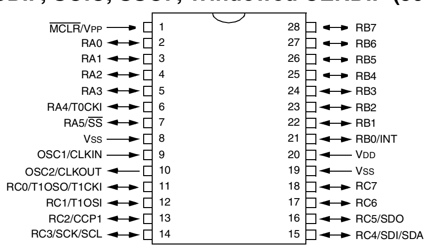
PIC16C61

SDIP, SOIC, SSOP, Windowed CERDIP (300 mil)



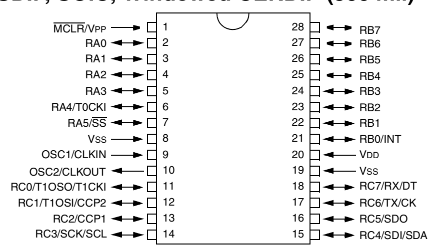
PIC16C62

SDIP, SOIC, SSOP, Windowed CERDIP (300 mil)



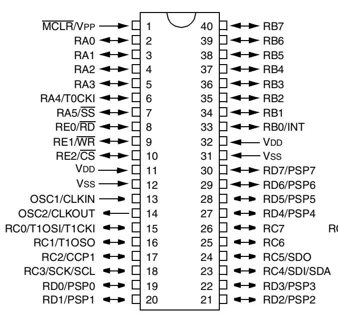
PIC16C62A
PIC16CR62

SDIP, SOIC, Windowed CERDIP (300 mil)

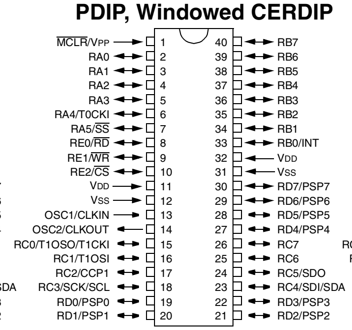


PIC16C63
PIC16CR63
PIC16C66

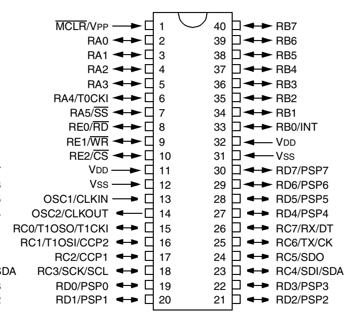
PDIP, Windowed CERDIP



PIC16C64



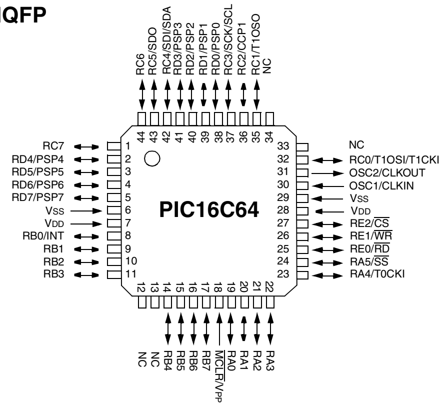
PIC16C64A
PIC16CR64



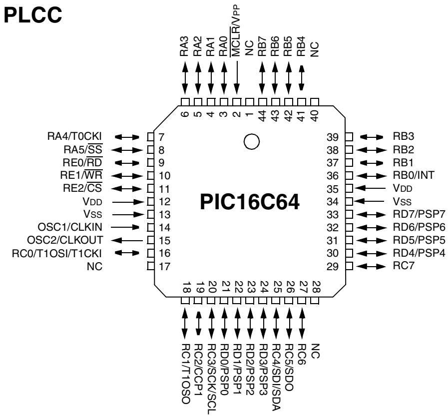
PIC16C65
PIC16C65A
PIC16CR65
PIC16C67

Pin Diagrams (Cont.'d)

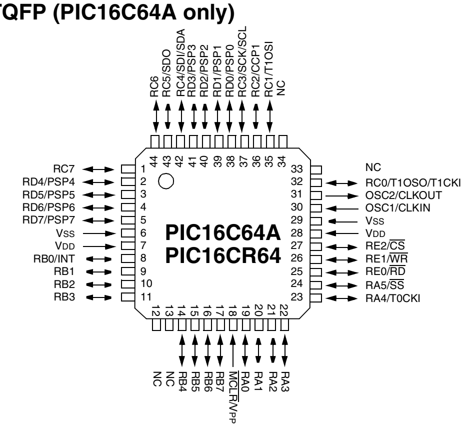
MQFP



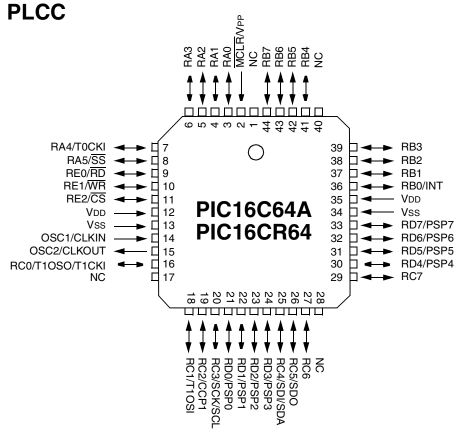
PLCC



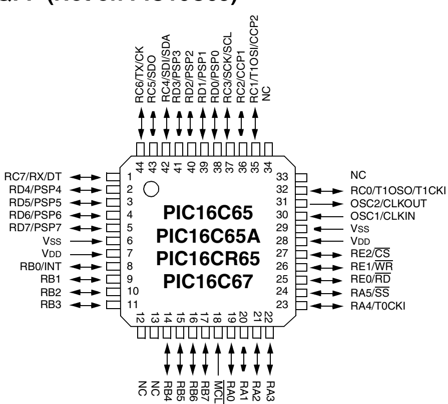
MQFP, TQFP (PIC16C64A only)



PLCC



MQFP, TQFP (Not on PIC16C65)



PLCC

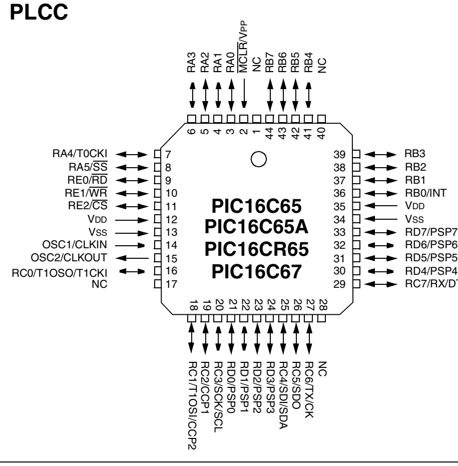


Table Of Contents

For register and module descriptions in this data sheet, device legends show which devices apply to those sections. For example, the legend below shows that some features of only the PIC16C62A, PIC16CR62, PIC16C63, PIC16C64A, PIC16CR64, and PIC16C65A are described in this section.

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

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1.0 GENERAL DESCRIPTION

The PIC16CXX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C61** device has 36 bytes of RAM and 13 I/O pins. In addition a timer/counter is available.

The **PIC16C62/62A/R62** devices have 128 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI™) or the two-wire Inter-Integrated Circuit (I^2C) bus.

The **PIC16C63/R63** devices have 192 bytes of RAM, while the **PIC16C66** has 368 bytes. All three devices have 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also know as a Serial Communications Interface or SCI.

The **PIC16C64/64A/R64** devices have 128 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. An 8-bit Parallel Slave Port is also provided.

The **PIC16C65/65A/R65** devices have 192 bytes of RAM, while the **PIC16C67** has 368 bytes. All four devices have 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also known as a Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is also provided.

The PIC16C6X device family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers a power saving mode. The user can wake the chip from SLEEP through several external and internal interrupts, and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C6X family fits perfectly in applications ranging from high-speed automotive and appliance control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use, and I/O flexibility make the PIC16C6X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions, and co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (Appendix B).

1.2 Development Support

PIC16C6X devices are supported by the complete line of Microchip Development tools.

Please refer to Section 15.0 for more details about Microchip's development tools.

TABLE 1-1: PIC16C6X FAMILY OF DEVICES

		PIC16C61	PIC16C62A	PIC16CR62	PIC16C63	PIC16CR63
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20
Memory	EPROM Program Memory (x14 words)	1K	2K	—	4K	—
	ROM Program Memory (x14 words)	—	—	2K	—	4K
	Data Memory (bytes)	36	128	128	192	192
Peripherals	Timer Module(s)	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/ PWM Module(s)	—	1	1	2	2
	Serial Port(s) (SPI/I^{2}C, USART)	—	SPI/I^{2}C	SPI/I^{2}C	SPI/I^{2}C, USART	SPI/I^{2}C USART
	Parallel Slave Port	—	—	—	—	—
Features	Interrupt Sources	3	7	7	10	10
	I/O Pins	13	22	22	22	22
	Voltage Range (Volts)	3.0-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	—	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SO	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC	28-pin SDIP, SOIC

		PIC16C64A	PIC16CR64	PIC16C65A	PIC16CR65	PIC16C66	PIC16C67
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
Memory	EPROM Program Memory (x14 words)	2K	—	4K	—	8K	8K
	ROM Program Memory (x14 words)	—	2K	—	4K	—	—
	Data Memory (bytes)	128	128	192	192	368	368
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/PWM Module(s)	1	1	2	2	2	2
	Serial Port(s) (SPI/I^{2}C, USART)	SPI/I^{2}C	SPI/I^{2}C	SPI/I^{2}C, USART	SPI/I^{2}C, USART	SPI/I^{2}C, USART	SPI/I^{2}C, USART
	Parallel Slave Port	Yes	Yes	Yes	Yes	—	Yes
Features	Interrupt Sources	8	8	11	11	10	11
	I/O Pins	33	33	33	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	Yes	Yes	Yes	Yes	Yes
	Packages	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C6X Family devices use serial programming with clock pin RB6 and data pin RB7.

2.0 PIC16C6X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C6X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C6X family of devices, there are four device “types” as indicated in the device number:

1. **C**, as in PIC16**C**64. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**64. These devices have EPROM type memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**64. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**64. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® Plus and PRO MATE® II programmers both support programming of the PIC16C6X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

ROM devices do not allow serialization information in the program memory space. The user may have this information programmed in the data memory space.

For information on submitting ROM code, please contact your regional sales office.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data may be fetched from the same memory using the same bus. Separating program and data busses further allows instructions to be sized differently than 8-bit wide data words. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C61 addresses 1K x 14 of program memory. The PIC16C62/62A/R62/64/64A/R64 address 2K x 14 of program memory, and the PIC16C63/R63/65/65A/R65 devices address 4K x 14 of program memory. The PIC16C66/67 address 8K x 14 program memory. All program memory is internal.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of “special optimal situations” makes programming with the PIC16CXX simple yet efficient, thus significantly reducing the learning curve.

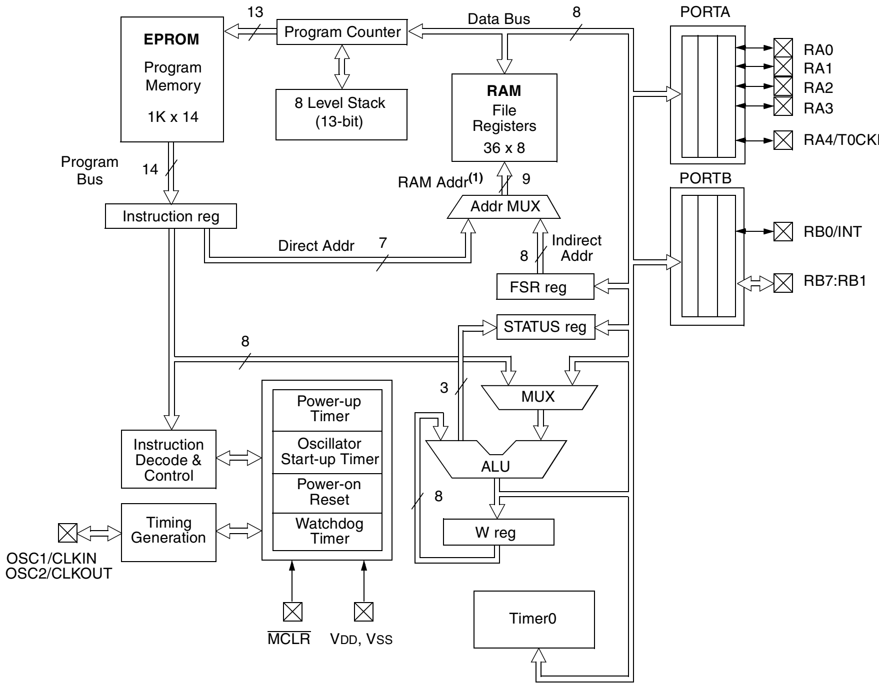
The PIC16CXX device contains an 8-bit ALU and working register (W). The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

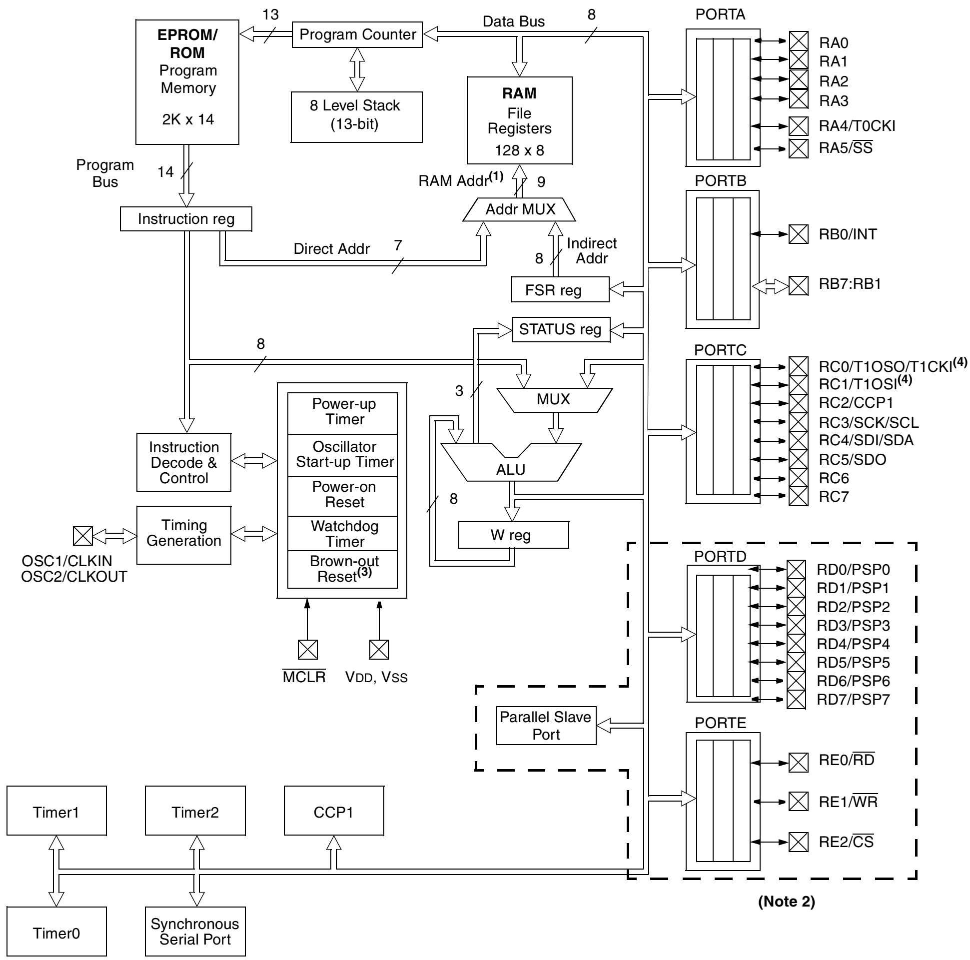
Depending upon the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. Bits C and DC operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 3-1: PIC16C61 BLOCK DIAGRAM



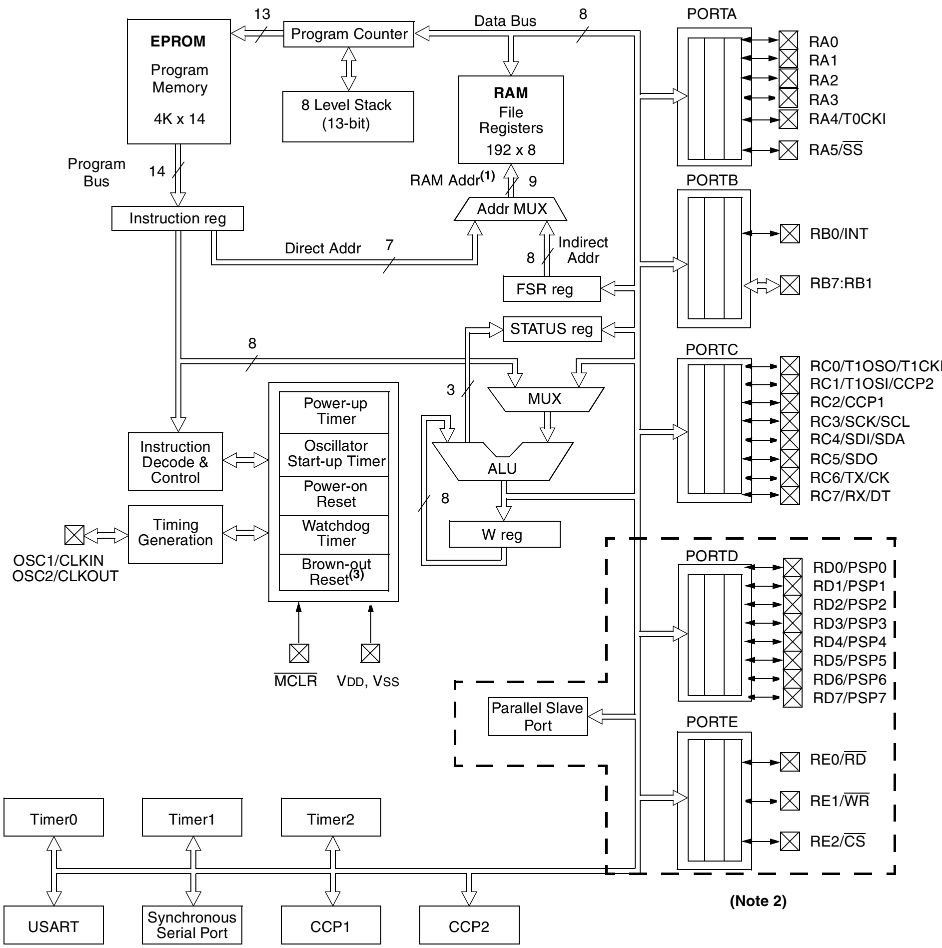
Note 1: Higher order bits are from the STATUS register.

FIGURE 3-2: PIC16C62/62A/R62/64/64A/R64 BLOCK DIAGRAM



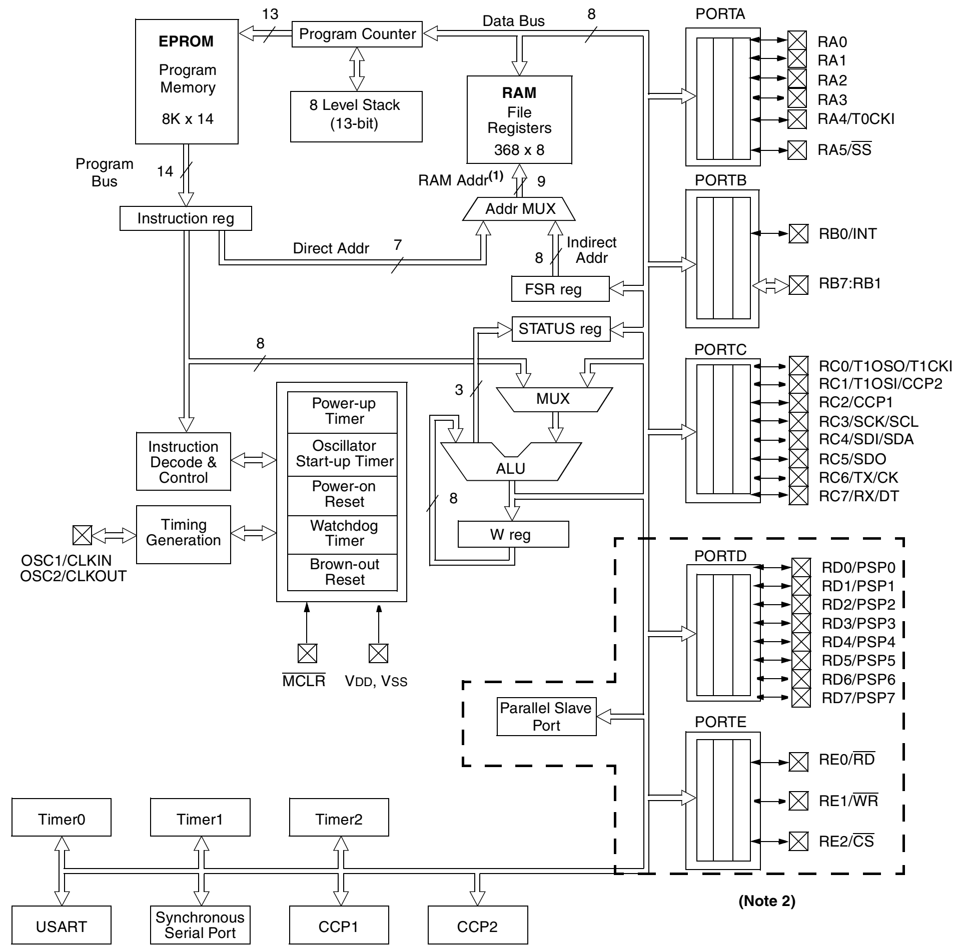
Note 1: Higher order bits are from the STATUS register.
2: PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C62/62A/R62.
3: Brown-out Reset is not available on the PIC16C62/64.
4: Pin functions T1OSI and T1OSO are swapped on the PIC16C62/64.

FIGURE 3-3: PIC16C63/R63/65/65A/R65 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C63/R63.
3: Brown-out Reset is not available on the PIC16C65.

FIGURE 3-4: PIC16C66/67 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C66.

TABLE 3-1: PIC16C61 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS(1)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST(2)	RB0 can also be the external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when configured as the external interrupt.
3: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-2: PIC16C62/62A/R62/63/R63/66 PINOUT DESCRIPTION

Pin Name	Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	9	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}/V_{PP}$	1	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
				PORTA is a bi-directional I/O port.
RA0	2	I/O	TTL	
RA1	3	I/O	TTL	
RA2	4	I/O	TTL	
RA3	5	I/O	TTL	
RA4/T0CKI	6	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{SS}$	7	I/O	TTL	RA5 can also be the slave select for the synchronous serial port.
				PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	I/O	TTL/ST(4)	RB0 can also be the external interrupt pin.
RB1	22	I/O	TTL	
RB2	23	I/O	TTL	
RB3	24	I/O	TTL	
RB4	25	I/O	TTL	Interrupt on change pin.
RB5	26	I/O	TTL	Interrupt on change pin.
RB6	27	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming clock.
RB7	28	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming data.
				PORTC is a bi-directional I/O port.
RC0/T1OSO(1)/T1CKI	11	I/O	ST	RC0 can also be the Timer1 oscillator output(1) or Timer1 clock input.
RC1/T1OSI(1)/CCP2(2)	12	I/O	ST	RC1 can also be the Timer1 oscillator input(1) or Capture2 input/Compare2 output/PWM2 output(2).
RC2/CCP1	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK(2)	17	I/O	ST	RC6 can also be the USART Asynchronous Transmit(2) or Synchronous Clock(2).
RC7/RX/DT(2)	18	I/O	ST	RC7 can also be the USART Asynchronous Receive(2) or Synchronous Data(2).
V_{SS}	8,19	P	—	Ground reference for logic and I/O pins.
V_{DD}	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C62.
2: The USART and CCP2 are not available on the PIC16C62/62A/R62.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
5: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-3: PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLK-OUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{\text{MCLR}}$/VPP	1	2	18	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	2	3	19	I/O	TTL	
RA1	3	4	20	I/O	TTL	
RA2	4	5	21	I/O	TTL	
RA3	5	6	22	I/O	TTL	
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{\text{SS}}$	7	8	24	I/O	TTL	RA5 can also be the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(4)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO(1)/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output(1) or Timer1 clock input.
RC1/T1OSI(1)/CCP2(2)	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input(1) or Capture2 input/Compare2 output/PWM2 output(2).
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK(2)	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit(2) or Synchronous Clock(2).
RC7/RX/DT(2)	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive(2) or Synchronous Data(2).

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.
2: CCP2 and the USART are not available on the PIC16C64/64A/R64.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
5: This buffer is a Schmitt Trigger input when used in serial programming mode.
6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

TABLE 3-3: PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION (Cont.'d)

Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(6)	
RD1/PSP1	20	22	39	I/O	ST/TTL(6)	
RD2/PSP2	21	23	40	I/O	ST/TTL(6)	
RD3/PSP3	22	24	41	I/O	ST/TTL(6)	
RD4/PSP4	27	30	2	I/O	ST/TTL(6)	
RD5/PSP5	28	31	3	I/O	ST/TTL(6)	
RD6/PSP6	29	32	4	I/O	ST/TTL(6)	
RD7/PSP7	30	33	5	I/O	ST/TTL(6)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{RD}$	8	9	25	I/O	ST/TTL(6)	RE0 can also be read control for the parallel slave port.
RE1/$\overline{WR}$	9	10	26	I/O	ST/TTL(6)	RE1 can also be write control for the parallel slave port.
RE2/$\overline{CS}$	10	11	27	I/O	ST/TTL(6)	RE2 can also be select control for the parallel slave port.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17, 28,40	12,13, 33,34	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.
2: CCP2 and the USART are not available on the PIC16C64/64A/R64.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
5: This buffer is a Schmitt Trigger input when used in serial programming mode.
6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3, and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clock and instruction execution flow is shown in Figure 3-5.

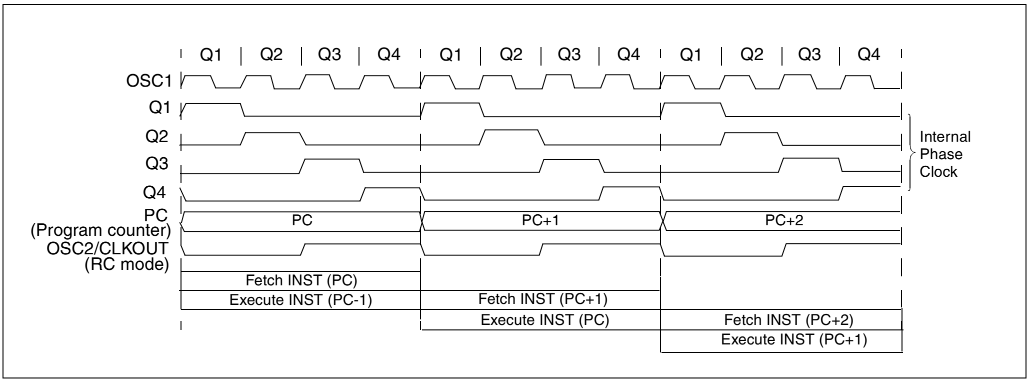
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. `GOTO`) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-5: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

	Tcy0	Tcy1	Tcy2	Tcy3	Tcy4	Tcy5
`1. MOVLW 55h`	Fetch 1	Execute 1				
`2. MOVWF PORTB`		Fetch 2	Execute 2			
`3. CALL SUB_1`			Fetch 3	Execute 3		
`4. BSF PORTA, BIT3 (Forced NOP)`				Fetch 4	Flush	
`5. Instruction @ address SUB_1`					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

4.0 MEMORY ORGANIZATION

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

4.1 Program Memory Organization

The PIC16C6X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

Device	Program Memory	Address Range
PIC16C61	1K x 14	0000h-03FFh
PIC16C62	2K x 14	0000h-07FFh
PIC16C62A	2K x 14	0000h-07FFh
PIC16CR62	2K x 14	0000h-07FFh
PIC16C63	4K x 14	0000h-0FFFh
PIC16CR63	4K x 14	0000h-0FFFh
PIC16C64	2K x 14	0000h-07FFh
PIC16C64A	2K x 14	0000h-07FFh
PIC16CR64	2K x 14	0000h-07FFh
PIC16C65	4K x 14	0000h-0FFFh
PIC16C65A	4K x 14	0000h-0FFFh
PIC16CR65	4K x 14	0000h-0FFFh
PIC16C66	8K x 14	0000h-1FFFh
PIC16C67	8K x 14	0000h-1FFFh

For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C61 PROGRAM MEMORY MAP AND STACK

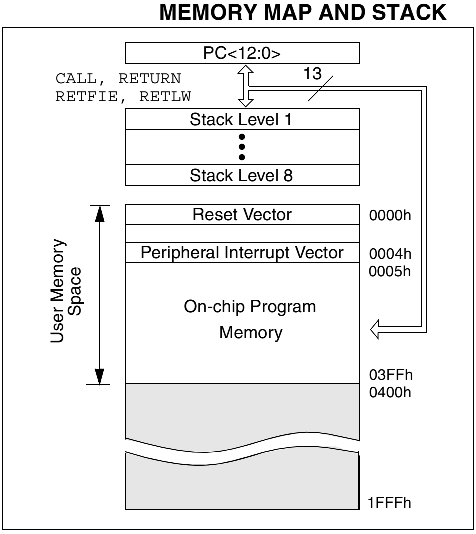


FIGURE 4-2: PIC16C62/62A/R62/64/64A/R64 PROGRAM MEMORY MAP AND STACK

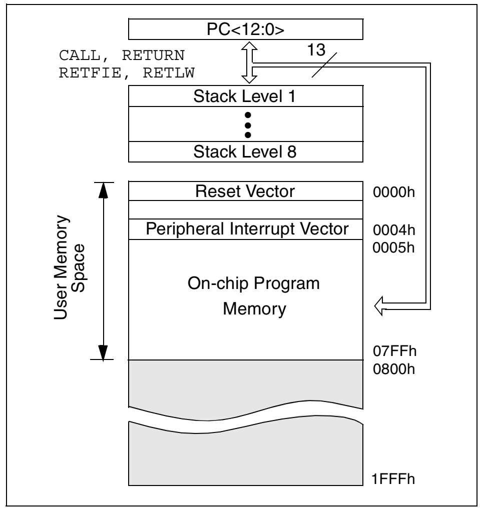


FIGURE 4-3: PIC16C63/R63/65/65A/R65 PROGRAM MEMORY MAP AND STACK

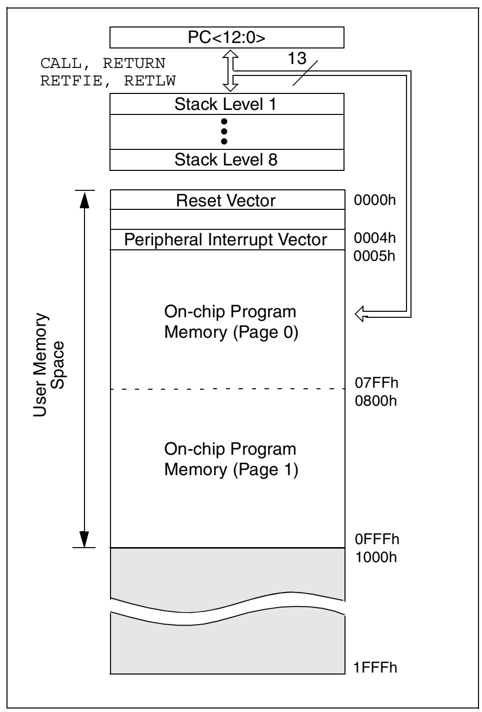
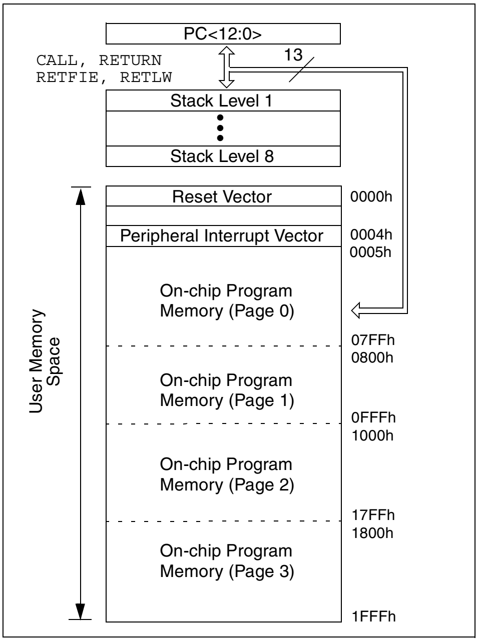


FIGURE 4-4: PIC16C66/67 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Applicable Devices													
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1:RP0 (STATUS<6:5>)
= 00 → Bank0
= 01 → Bank1
= 10 → Bank2
= 11 → Bank3

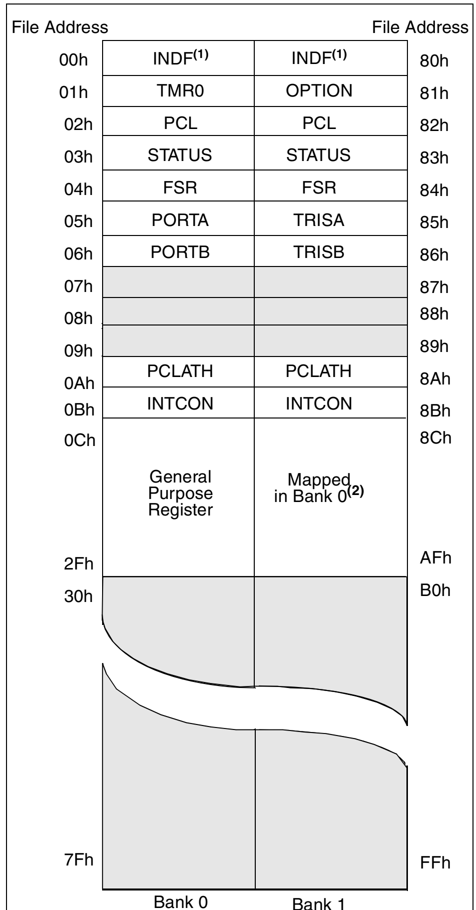
Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some “high use” special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTERS

These registers are accessed either directly or indirectly through the File Select Register (FSR) (Section 4.5).

For the PIC16C61, general purpose register locations 8Ch-AFh of Bank 1 are not physically implemented. These locations are mapped into 0Ch-2Fh of Bank 0.

FIGURE 4-5: PIC16C61 REGISTER FILE MAP



Unimplemented data memory location; read as '0'.
Note 1: Not a physical register.
2: These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

FIGURE 4-6: PIC16C62/62A/R62/64/64A/R64 REGISTER FILE MAP

File Address	Bank 0	Bank 1	File Address
00h	INDF(1)	INDF(1)	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD(2)	TRISD(2)	88h
09h	PORTE(2)	TRISE(2)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h–1Fh			98h–9Fh
20h–7Fh	General Purpose Register	General Purpose Register	A0h–BFh
			C0h–FFh

Bank 0 Bank 1

☐ Unimplemented data memory location; read as '0'.

Note 1: Not a physical register.

2: PORTD and PORTE are not available on the PIC16C62/62A/R62.

FIGURE 4-7: PIC16C63/R63/65/65A/R65 REGISTER FILE MAP

File Address	Bank 0	Bank 1	File Address
00h	INDF(1)	INDF(1)	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD(2)	TRISD(2)	88h
09h	PORTE(2)	TRISE(2)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	PIR2	PIE2	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h–7Fh	General Purpose Register	General Purpose Register	A0h–FFh

Bank 0 Bank 1

☐ Unimplemented data memory location; read as '0'.

Note 1: Not a physical register

2: PORTD and PORTE are not available on the PIC16C63/R63.

FIGURE 4-8: PIC16C66/67 DATA MEMORY MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD (1)	08h	TRISD (1)	88h		108h		188h
PORTE (1)	09h	TRISE (1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
PIR2	0Dh	PIE2	8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh		8Fh		10Fh		18Fh
T1CON	10h		90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h		91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch		9Ch		11Ch		19Ch
CCP2CON	1Dh		9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h
			EFh		16Fh		1EFh
		accesses 70h-7Fh in Bank 0	F0h	accesses 70h-7Fh in Bank 0	170h	accesses 70h-7Fh in Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh

[grey box] Unimplemented data memory locations, read as '0'.

* Not a physical register.

These registers are not implemented on the PIC16C66.

Note: The upper 16 bytes of data memory in banks 1, 2, and 3 are mapped in Bank 0. This may require relocation of data memory usage in the user application code if upgrading to the PIC16C66/67.

4.2.2 SPECIAL FUNCTION REGISTERS:

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). The registers associated with the “core” functions are described in this section and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTERS FOR THE PIC16C61

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module’s register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	PORTA Data Latch when written: PORTA pins when read					---x xxxx	---u uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	—	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0-00 000x	0-00 000u
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111
86h	TRISB	PORTB Data Direction Control Register								1111 1111	1111 1111
87h	–	Unimplemented								—	—
88h	–	Unimplemented								—	—
89h	–	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	—	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0-00 000x	0-00 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented locations read as '0'. Shaded locations are unimplemented and read as ‘0’

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C61, always maintain these bits clear.

TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(6)	(6)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The $\overline{BOR}$ bit is reserved on the PIC16C62, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	**(6)**	**(6)**	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$(4)	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	--00 0000	--00 0000
95h-9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{\text{MCLR}}$ and the Watchdog Timer reset.

4: The $\overline{\text{BOR}}$ bit is reserved on the PIC16C62, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.