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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# PIC16(L)F151X/152X Memory Programming Specification

**This document includes the programming specifications for the following devices:**

- PIC16F1512
- PIC16LF1512
- PIC16F1513
- PIC16LF1513
- PIC16F1516
- PIC16LF1516
- PIC16F1517
- PIC16LF1517
- PIC16F1518
- PIC16LF1518
- PIC16F1519
- PIC16LF1519
- PIC16F1526
- PIC16LF1526
- PIC16F1527
- PIC16LF1527

## 1.0 OVERVIEW

The PIC16(L)F151X/152X devices can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP™ method.

### 1.1 Hardware Requirements

#### 1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP™ mode, these devices require two programmable power supplies; one for VDD and one for the MCLR/VPP pin.

#### 1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP™ mode, these devices can be programmed using a single VDD source in the operating range. The MCLR/VPP pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

##### 1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to VIHH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

**Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR/VPP pin.

**2:** While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

## 1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1 and Table 1-2.

**TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1526 AND PIC16(L)F1527**

| Pin Name | During Programming | | |
|---|---|---|---|
| | Function | Pin Type | Pin Description |
| RB6 | ICSPCLK | I | Clock Input – Schmitt Trigger Input |
| RB7 | ICSPDAT | I/O | Data Input/Output – Schmitt Trigger Input |
| RG5/$\overline{MCLR}$/VPP | Program/Verify mode | P(1) | Program Mode Select/Programming Power Supply |
| VDD | VDD | P | Power Supply |
| VSS | VSS | P | Ground |

**Legend:** I = Input, O = Output, P = Power

**Note 1:** The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

**TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516, PIC16(L)F1517, PIC16(L)F1518 and PIC16(L)F1519**

| Pin Name | During Programming | | |
|---|---|---|---|
| | Function | Pin Type | Pin Description |
| RB6 | ICSPCLK | I | Clock Input – Schmitt Trigger Input |
| RB7 | ICSPDAT | I/O | Data Input/Output – Schmitt Trigger Input |
| RE3/$\overline{MCLR}$/VPP | Program/Verify mode | P(1) | Program Mode Select/Programming Power Supply |
| VDD | VDD | P | Power Supply |
| VSS | VSS | P | Ground |

**Legend:** I = Input, O = Output, P = Power

**Note 1:** The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

## 2.0 DEVICE PINOUTS

The pin diagrams for the PIC16(L)F151X/152X family are shown in Figure 2-1 through Figure 2-7. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

**FIGURE 2-1: 28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518**

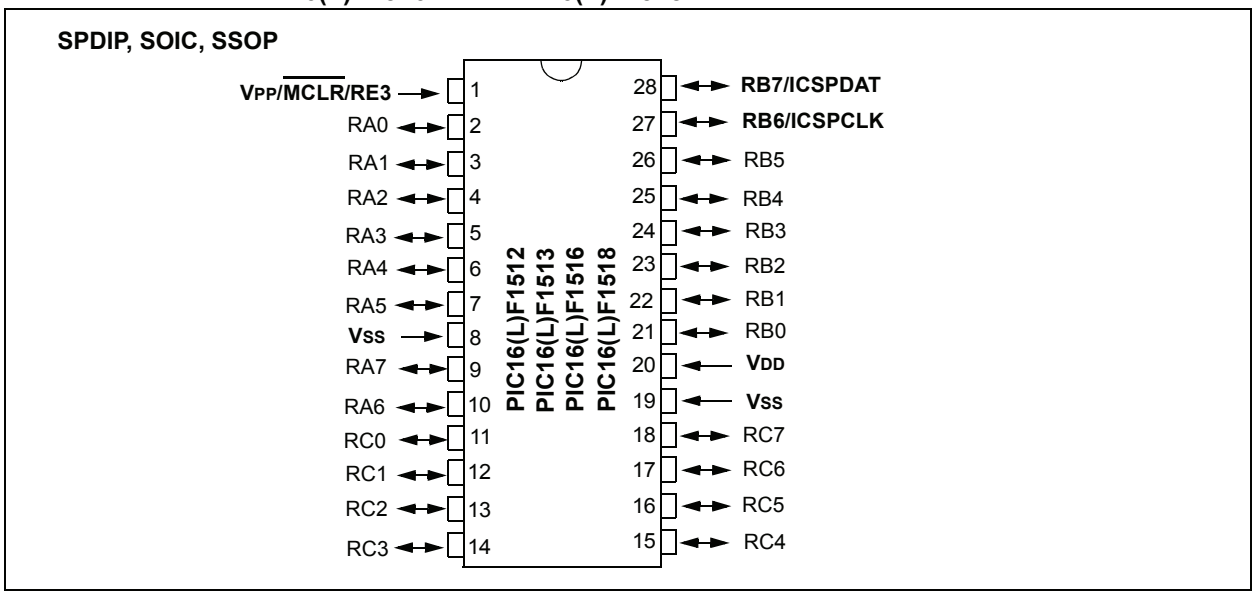


**FIGURE 2-2: 28-PIN UQFN DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518**

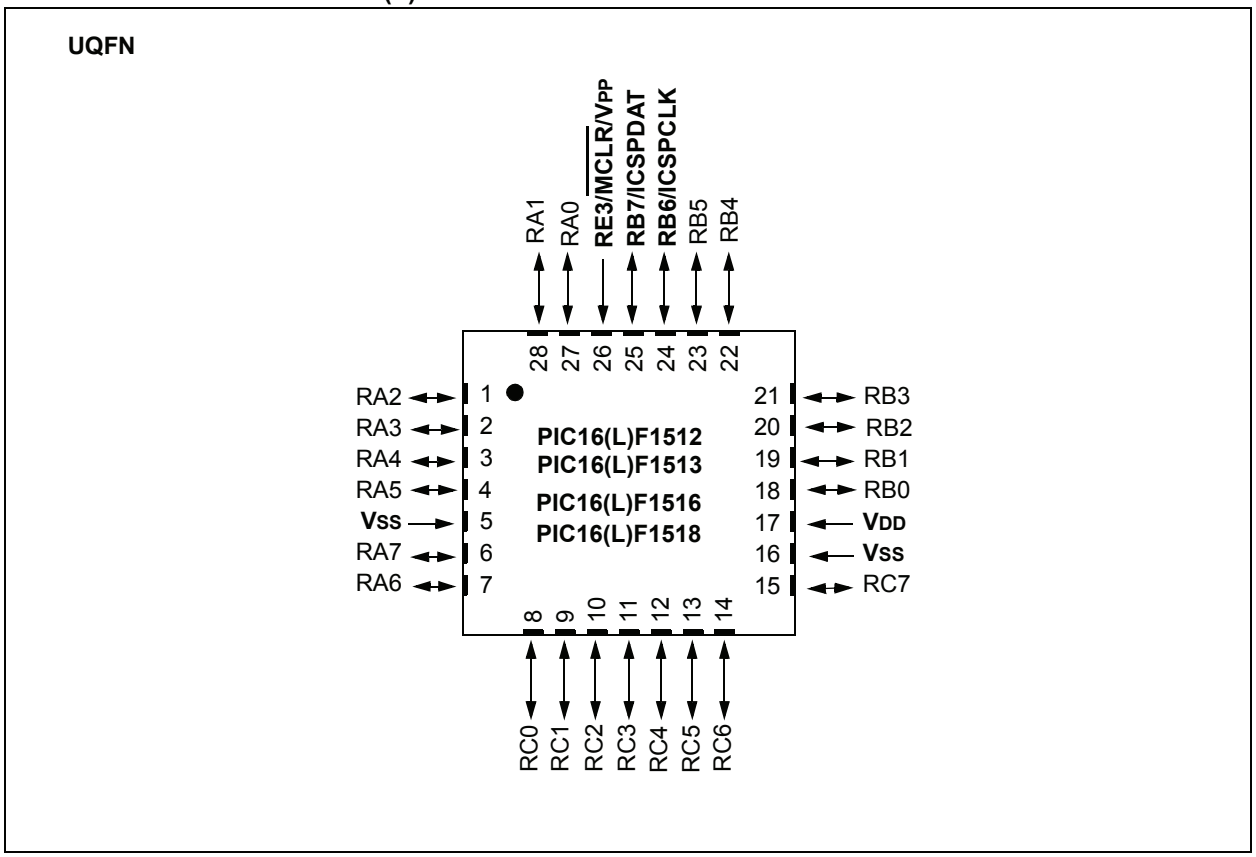


**FIGURE 2-3: 40-PIN PDIP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519**

**PDIP**

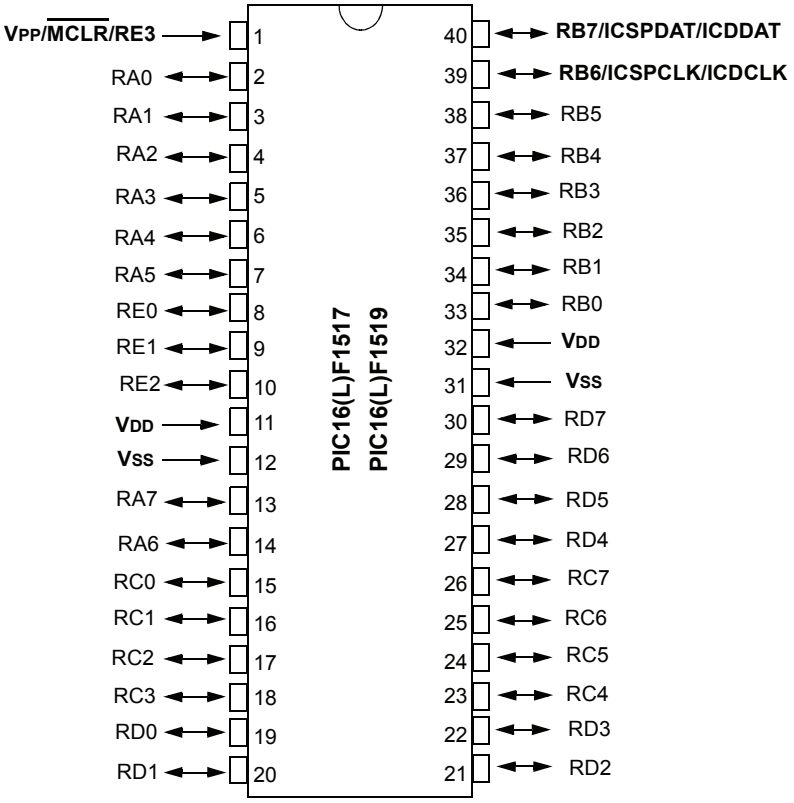



**FIGURE 2-4: 40-PIN UQFN DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519**

**UQFN**

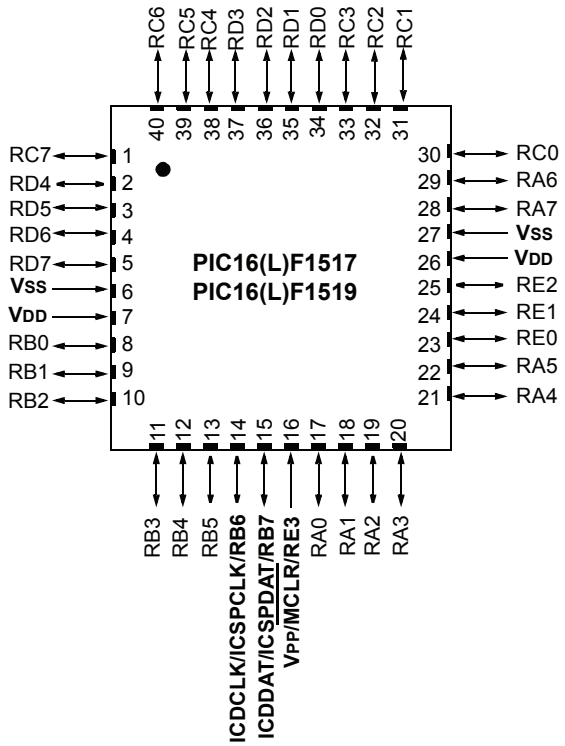


**FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519**

**TQFP**

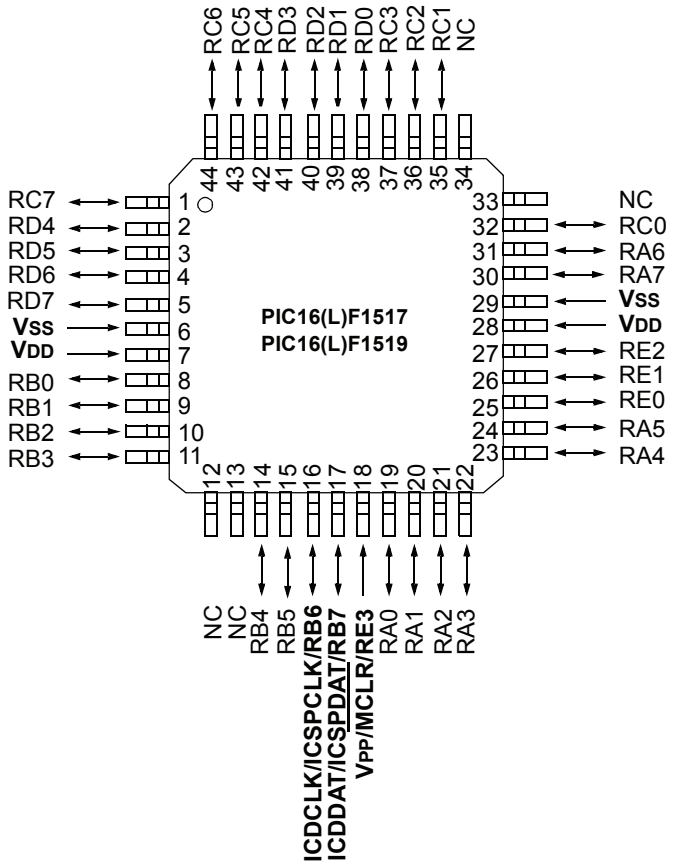


**FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527**

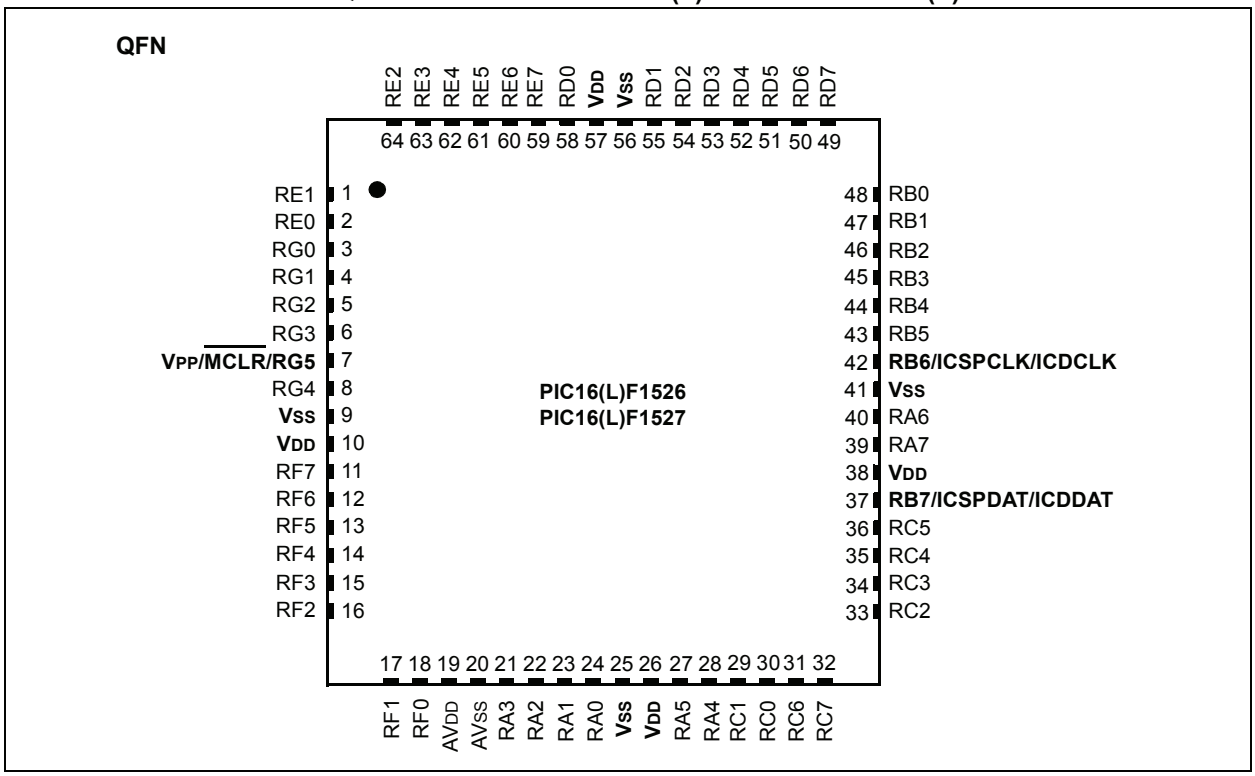
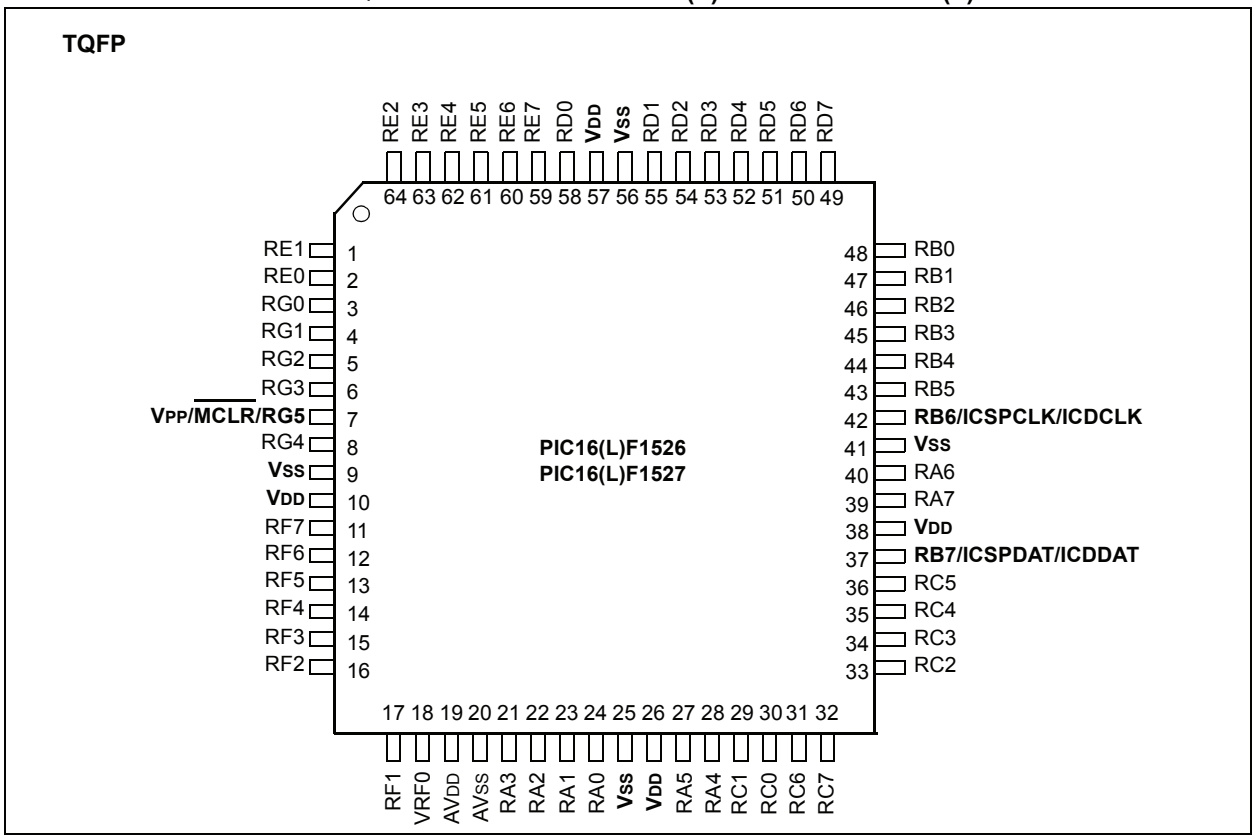



**FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527**



## 3.0 MEMORY MAP

The memory for the PIC16(L)F151X/152X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

**FIGURE 3-1: PIC16(L)F1512 PROGRAM MEMORY MAPPING**

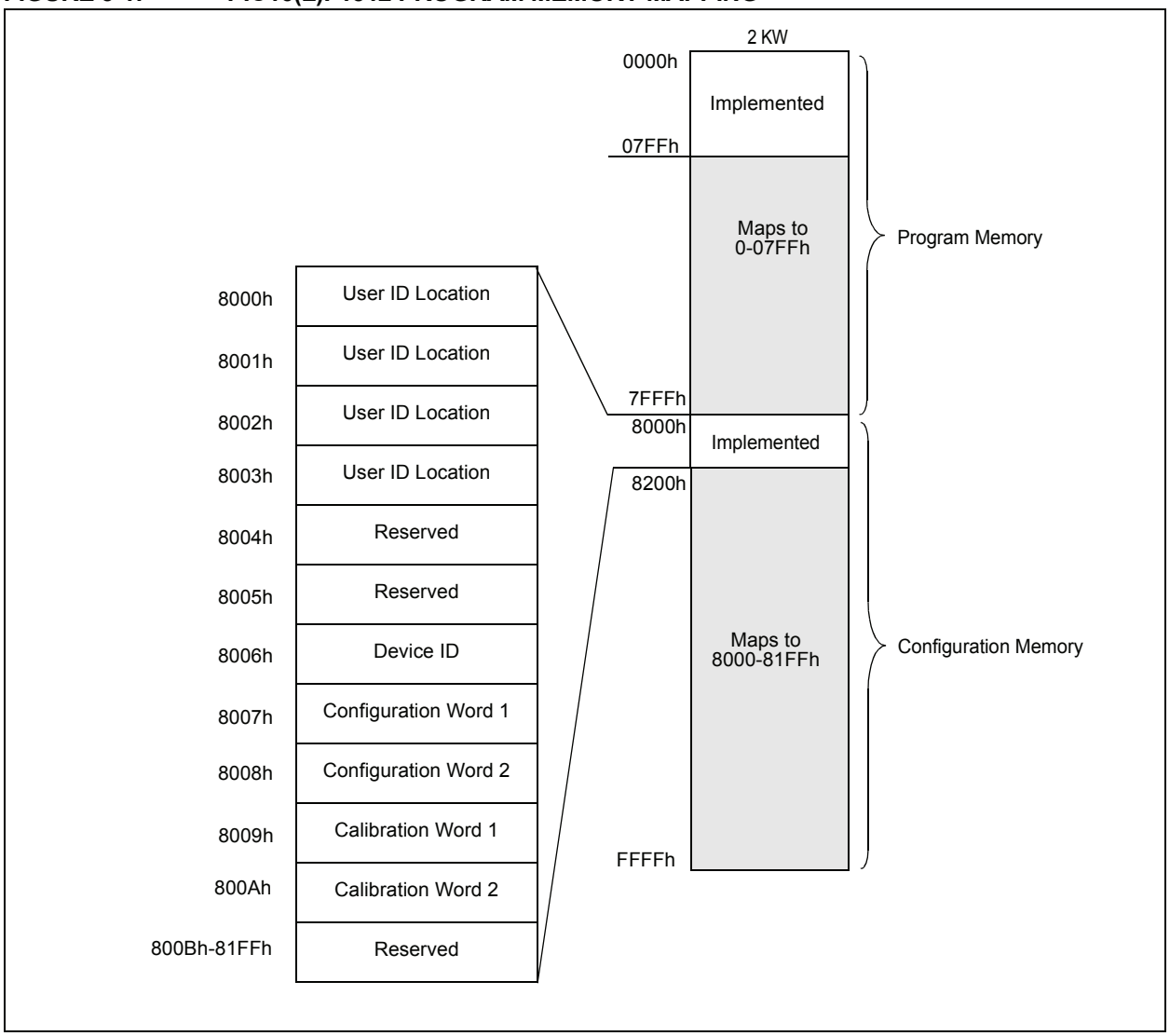


**FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING**

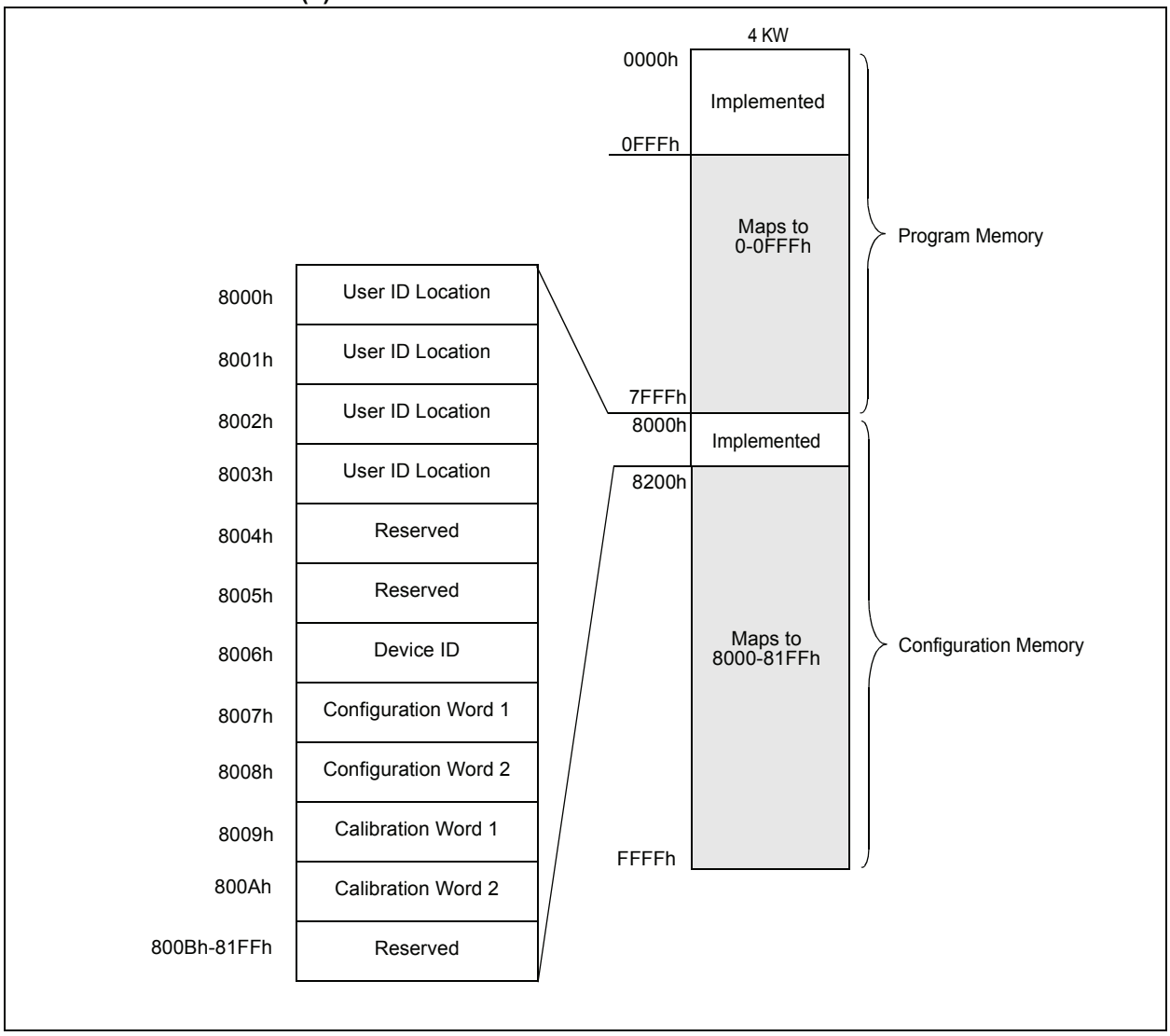


**FIGURE 3-3: PIC16(L)F1526, PIC16(L)F1516 AND PIC16(L)F1517 PROGRAM MEMORY MAPPING**

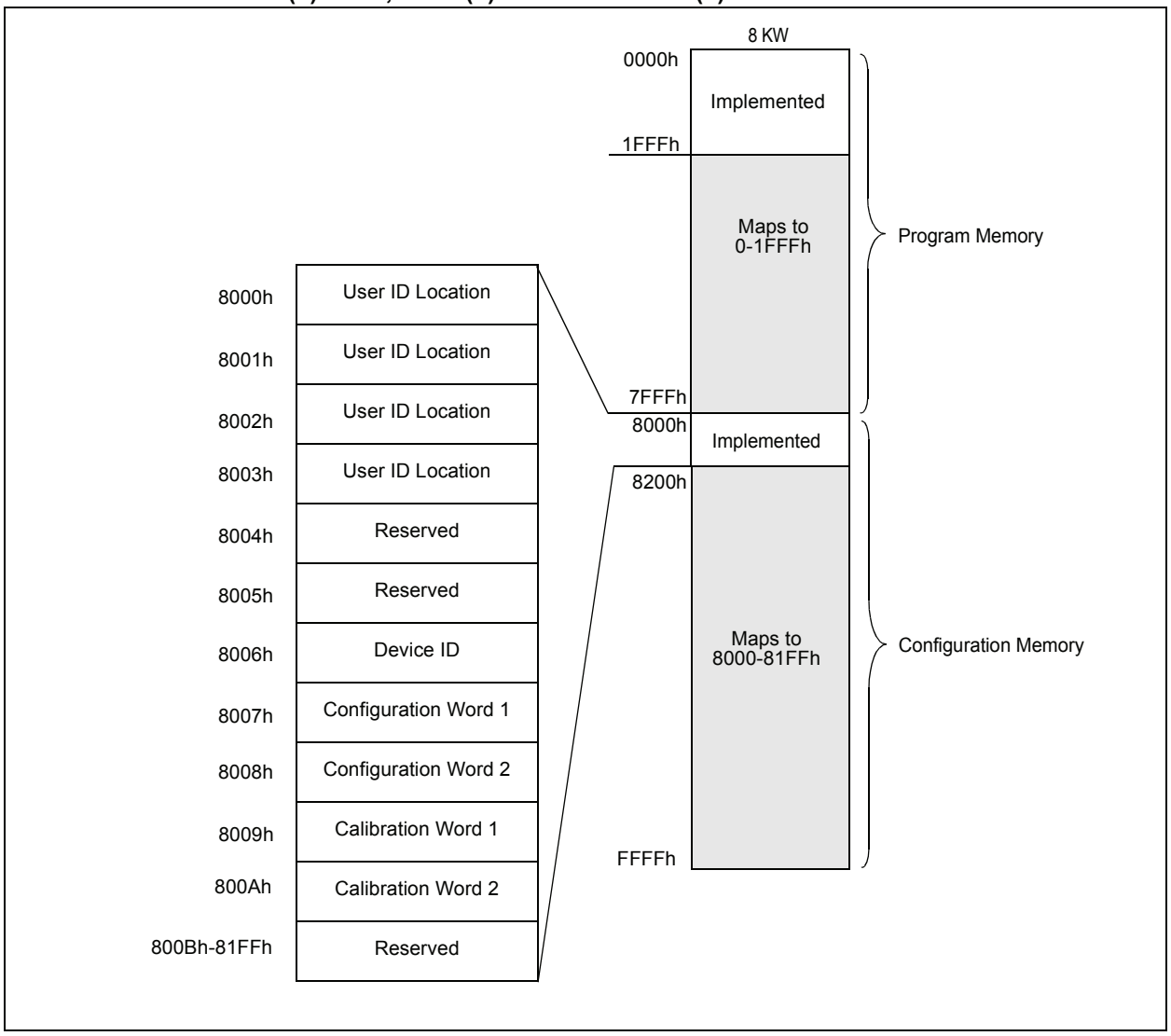
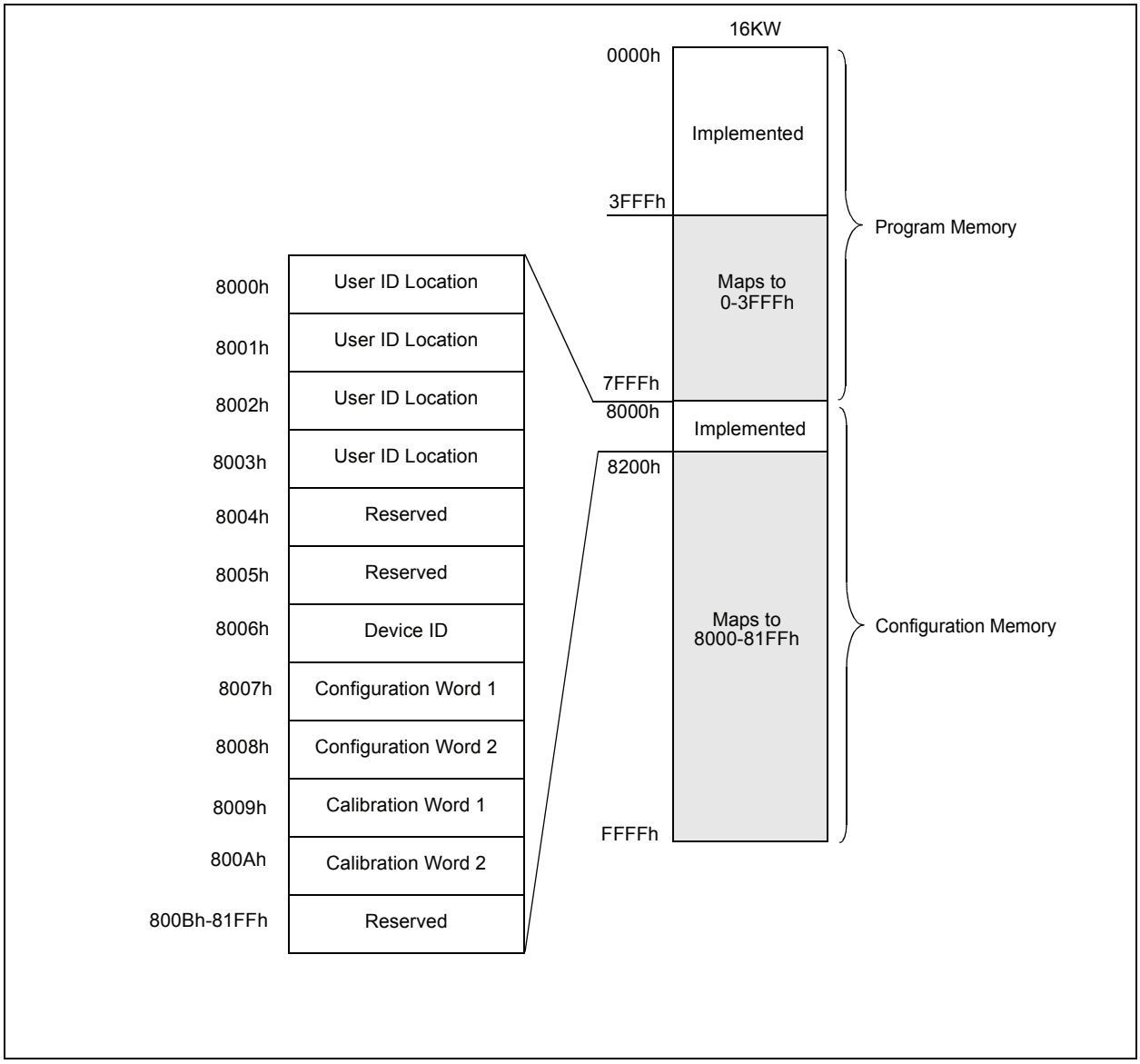


**FIGURE 3-4: PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING**



## 3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

**Note:** MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

## 3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

**REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)**

| R | R | R | R | R | R |
|---|---|---|---|---|---|
| DEV<8:3> | | | | | |
| bit 13 | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEV<2:0> | | | REV<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | P = Programmable bit | U = Unimplemented bit, read as ‘0’ |
|---|---|---|
| R = Readable bit | W = Writable bit | ‘0’ = Bit is cleared |
| -n = Value at POR | ‘1’ = Bit is set | x = Bit is unknown |

bit 13-5 **DEV<8:0>:** Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to identify the revision.

**Note 1:** This location cannot be written.

**TABLE 3-1: DEVICE ID VALUES**

| DEVICE | DEVICE ID VALUES | |
|---|---|---|
| | DEV | REV |
| PIC16F1527 | 0001 0101 101 | x xxxx |
| PIC16F1526 | 0001 0101 100 | x xxxx |
| PIC16LF1527 | 0001 0101 111 | x xxxx |
| PIC16LF1526 | 0001 0101 110 | x xxxx |
| PIC16F1519 | 0001 0110 111 | x xxxx |
| PIC16F1518 | 0001 0110 110 | x xxxx |
| PIC16F1517 | 0001 0110 101 | x xxxx |
| PIC16F1516 | 0001 0110 100 | x xxxx |
| PIC16F1513 | 0001 0110 010 | x xxxx |
| PIC16F1512 | 0001 0111 000 | x xxxx |
| PIC16LF1519 | 0001 0111 111 | x xxxx |
| PIC16LF1518 | 0001 0111 110 | x xxxx |
| PIC16LF1517 | 0001 0111 101 | x xxxx |
| PIC16LF1516 | 0001 0111 100 | x xxxx |
| PIC16LF1513 | 0001 0111 010 | x xxxx |
| PIC16LF1512 | 0001 0111 001 | x xxxx |

## 3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

## 3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

**REGISTER 3-2: CONFIGURATION WORD 1**

| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 |
|---|---|---|---|---|---|
| FCMEN | IESO | $\overline{\text{CLKOUTEN}}$ | BOREN<1:0> | | — |
| bit 13 | | | | | bit 8 |

| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{CP}}$ | MCLRE | $\overline{\text{PWRTE}}$ | WDTE<1:0> | | FOSC<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | P = Programmable bit | U = Unimplemented bit, read as '1' |
| '0' = Bit is cleared | '1' = Bit is set | -n = Value when blank or after Bulk Erase |

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 8 **Unimplemented:** Read as '1'

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA register.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = ECH: External Clock, High-Power mode: on CLKIN pin
110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
101 = ECL: External Clock, Low-Power mode: on CLKIN pin
100 = INTOSC oscillator: I/O function on OSC1 pin
011 = EXTRC oscillator: RC function on OSC1 pin
010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

**Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
**2:** The entire program memory will be erased when the code protection is turned off.

**REGISTER 3-3: CONFIGURATION WORD 2**

| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 |
|---|---|---|---|---|---|
| LVP | $\overline{\text{DEBUG}}$ | $\overline{\text{LPBOR}}$ | BORV | STVREN | — |
| bit 13 | | | | | bit 8 |

| U-1 | U-1 | U-1 | R/P-1 | U-1 | U-1 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | $\overline{\text{VCAPEN}}$(2) | — | — | WRT<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | P = Programmable bit | U = Unimplemented bit, read as '1' |
| '0' = Bit is cleared | '1' = Bit is set | -n = Value when blank or after Bulk Erase |

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
1 = Low-voltage programming enabled
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (VBOR), low trip point selected
0 = Brown-out Reset voltage (VBOR), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8-5 **Unimplemented:** Read as '1'

bit 4 **$\overline{\text{VCAPEN}}$:** Voltage Regulator Capacitor Enable bits(1)
0 = VCAP functionality is enabled on VCAP pin
1 = All VCAP pin functions are disabled

bit 3-2 **Unimplemented:** Read as '1'

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

**Note 1:** The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
**2:** Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the $\overline{\text{VCAPEN}}$ bit is unimplemented.

## 4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

### 4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

#### 4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{\text{PWRTE}}$ = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

#### 4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

#### 4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

### 4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to VIL. See Figure 8-8 and Figure 8-9.

| **Note:** | To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts. |
|---|---|

## 4.3 Program/Verify Commands

The PIC16(L)F151X/152X implements 10 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

**TABLE 4-1: COMMAND MAPPING**

| Command | Mapping | | | | | | | Data/Note |
|---|---|---|---|---|---|---|---|---|
| | Binary (MSb … LSb) | | | | | | Hex | |
| Load Configuration | x | 0 | 0 | 0 | 0 | 0 | 00h | 0, data (14), 0 |
| Load Data For Program Memory | x | 0 | 0 | 0 | 1 | 0 | 02h | 0, data (14), 0 |
| Read Data From Program Memory | x | 0 | 0 | 1 | 0 | 0 | 04h | 0, data (14), 0 |
| Increment Address | x | 0 | 0 | 1 | 1 | 0 | 06h | — |
| Reset Address | x | 1 | 0 | 1 | 1 | 0 | 16h | — |
| Begin Internally Timed Programming | x | 0 | 1 | 0 | 0 | 0 | 08h | — |
| Begin Externally Timed Programming | x | 1 | 1 | 0 | 0 | 0 | 18h | — |
| End Externally Timed Programming | x | 0 | 1 | 0 | 1 | 0 | 0Ah | — |
| Bulk Erase Program Memory | x | 0 | 1 | 0 | 0 | 1 | 09h | Internally Timed |
| Row Erase Program Memory | x | 1 | 0 | 0 | 0 | 1 | 11h | Internally Timed |

### 4.3.1 LOAD CONFIGURATION

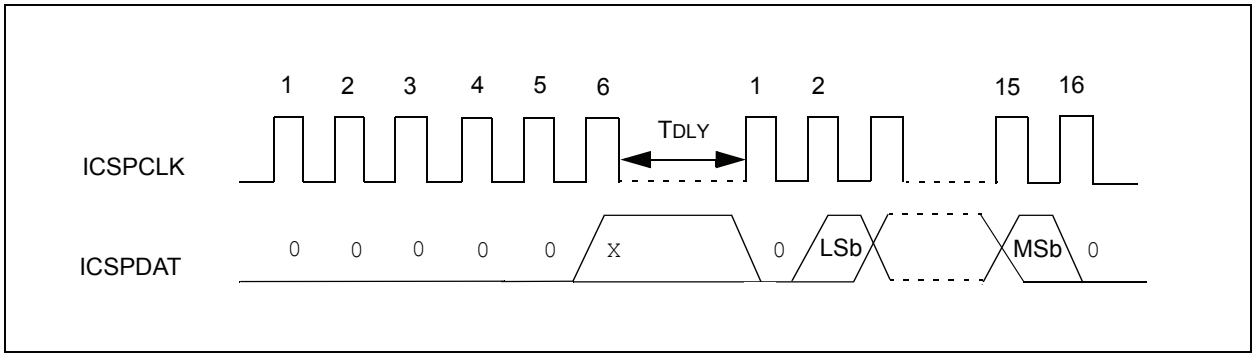
The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

**Note:** Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

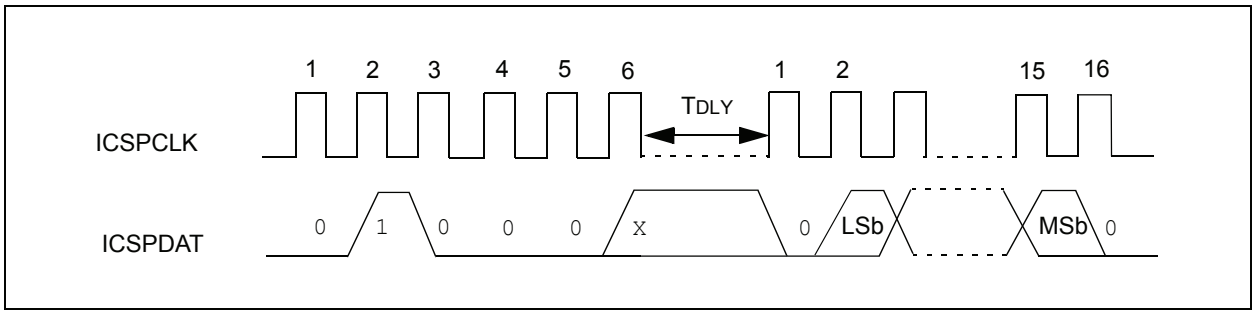
**FIGURE 4-1: LOAD CONFIGURATION**



### 4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

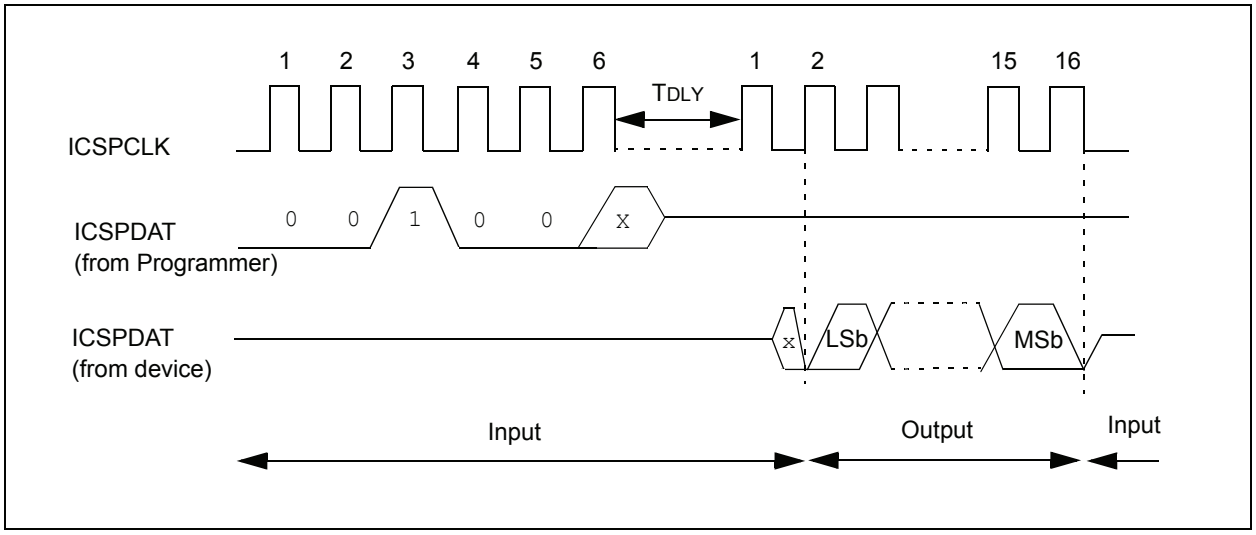
**FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY**




### 4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

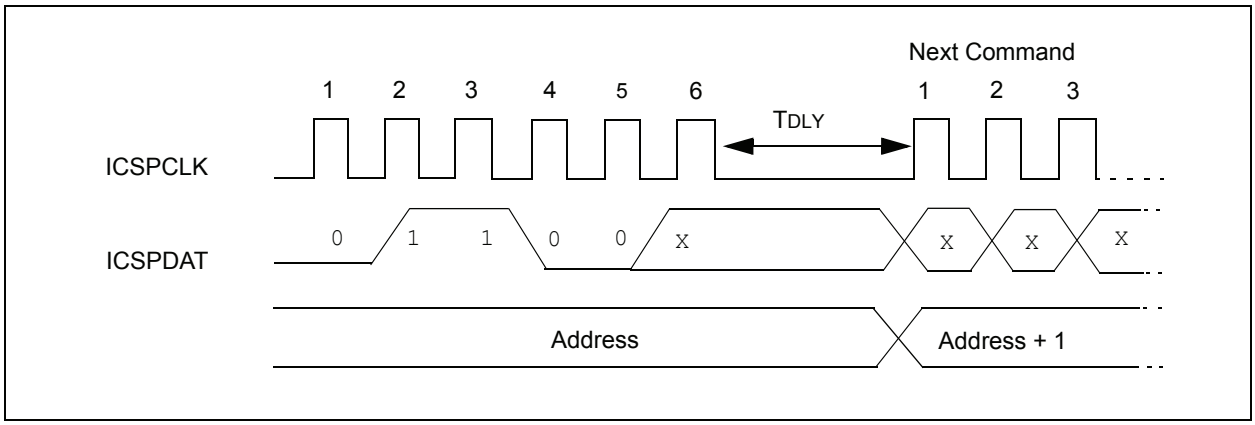
**FIGURE 4-3: READ DATA FROM PROGRAM MEMORY**



### 4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

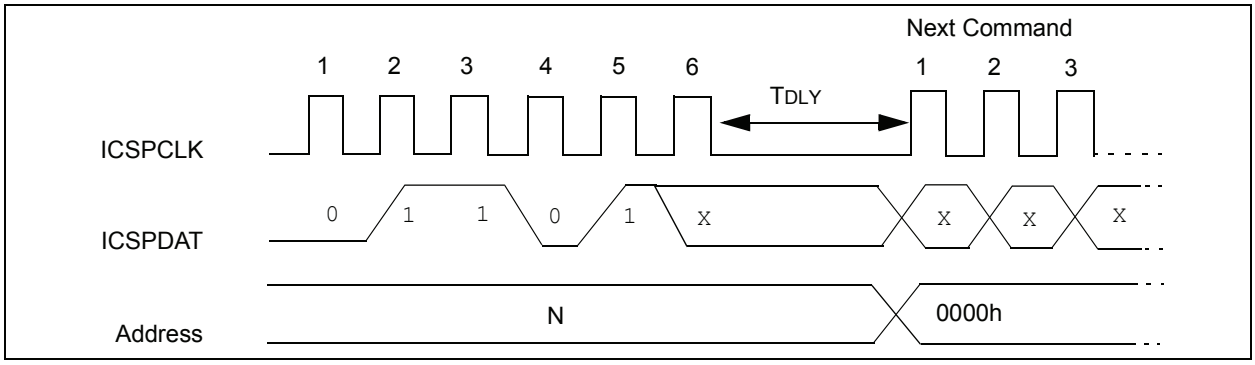
**FIGURE 4-4: INCREMENT ADDRESS**




### 4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

**FIGURE 4-5: RESET ADDRESS**



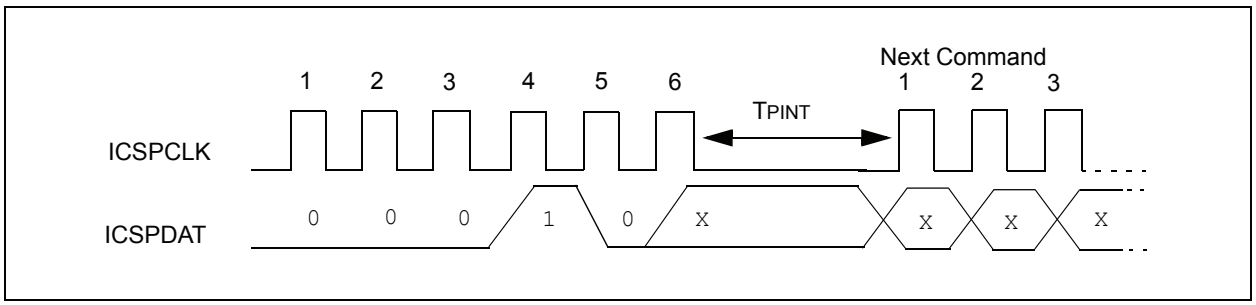
### 4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

**FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING**

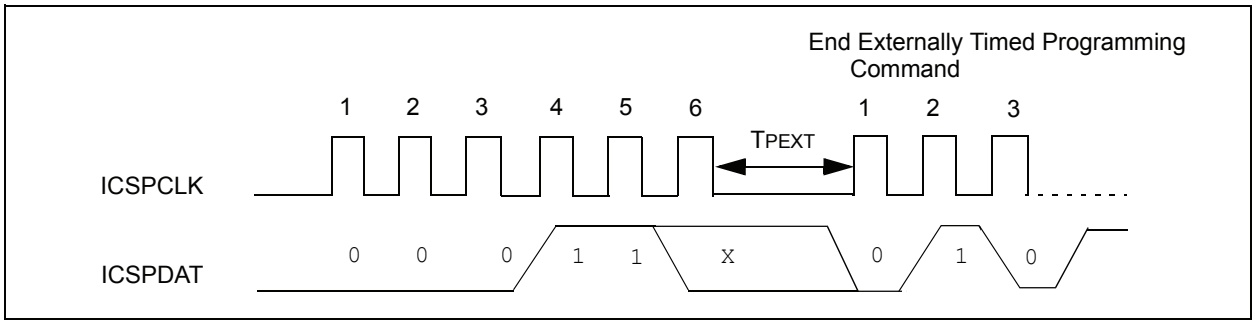



### 4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

**FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING**



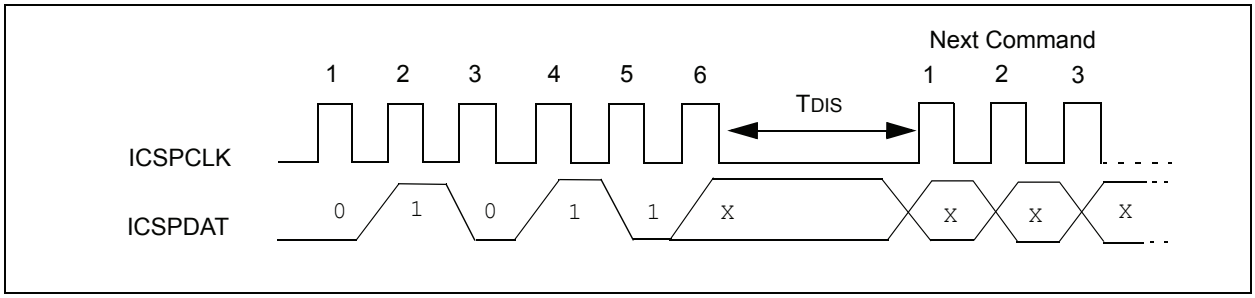

 

### 4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

**FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING**




### 4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8008h:

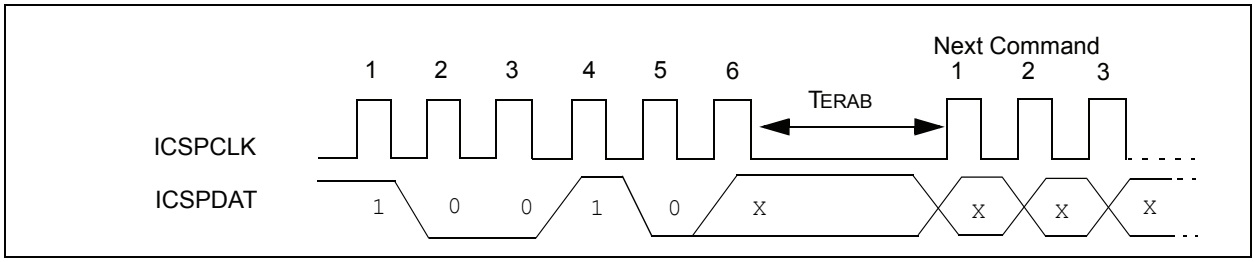
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

| **Note:** | The code protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command. |
|---|---|

**FIGURE 4-9: BULK ERASE PROGRAM MEMORY**



### 4.3.10 ROW ERASE PROGRAM MEMORY

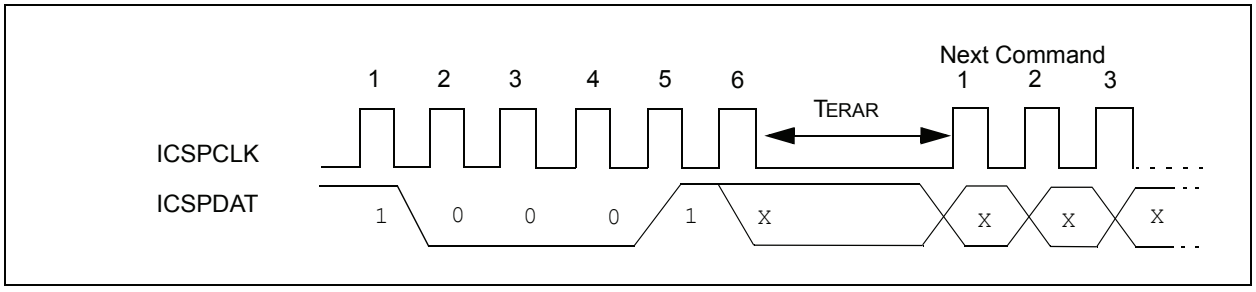
The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, TERAR, has expired.

**TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES**

| Devices | PC | Row Size | Number of Latches |
|---|---|---|---|
| PIC16(L)F151X/152X | <15:5> | 32 | 32 |

**FIGURE 4-10: ROW ERASE PROGRAM MEMORY**



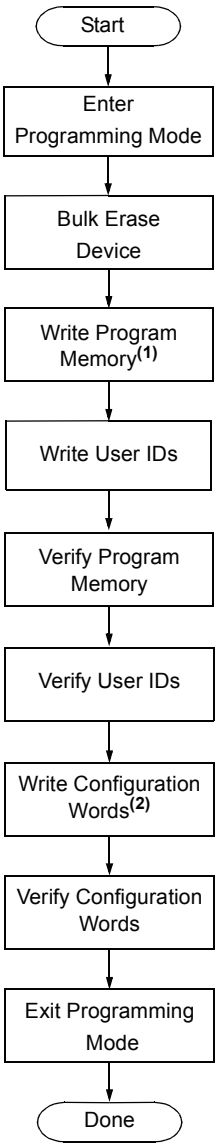
## 5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

**FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART**

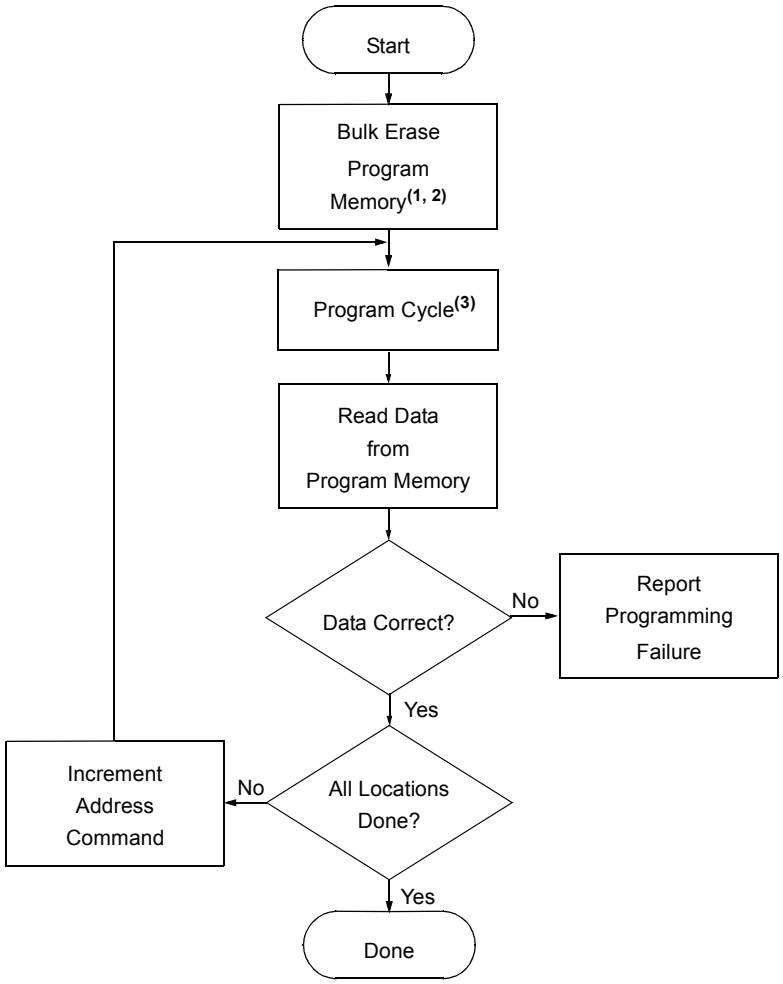



**Note 1:** See Figure 5-2.

**2:** See Figure 5-5.

**FIGURE 5-2: PROGRAM MEMORY FLOWCHART**




**Note 1:** This step is optional if device has already been erased or has not been previously programmed.

**2:** If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-6.

**3:** See Figure 5-3 or Figure 5-4.