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Full-Featured 8/14-Pin Microcontrollers

Description

PIC16(L)F15313/23 microcontrollers feature Analog, Core Independent Peripherals and Communication Peripherals, combined with eXtreme Low-Power (XLP) technology for a wide range of general purpose and low-power applications.

The devices feature multiple PWMs, multiple communication, temperature sensor, and memory features like Memory Access Partition (MAP) to support customers in data protection and bootloader applications, and Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
 - DC – 32 MHz clock input
 - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
 - 8-bit Timer2 with Hardware Limit Timer (HLT)
 - 16-bit Timer0/1
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
 - Variable prescaler selection
 - Variable window size selection
 - All sources configurable in hardware or software
- Programmable Code Protection

Memory

- 3.5 KB Flash Program Memory
- 256 Bytes Data SRAM
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
 - Write protect
 - Customizable Partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

Operating Characteristics

- Operating Voltage Range:
 - 1.8V to 3.6V (PIC16LF15313/23)
 - 2.3V to 5.5V (PIC16F15313/23)
- Temperature Range:
 - Industrial: -40°C to 85°C
 - Extended: -40°C to 125°C

Power-Saving Functionality

- DOZE mode: Ability to Run the CPU Core Slower than the System Clock
- IDLE mode: Ability to halt CPU Core while Internal Peripherals Continue Operating
- SLEEP mode: Lowest Power Consumption
- Peripheral Module Disable (PMD):
 - Ability to disable hardware module to minimize active power consumption of unused peripherals

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Operating Current:
 - 8 μ A @ 32 kHz, 1.8V, typical
 - 32 μ A/MHz @ 1.8V, typical

Digital Peripherals

- Four Configurable Logic Cells (CLC):
 - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
 - Rising and falling edge dead-band control
 - Full-bridge, half-bridge, 1-channel drive
 - Multiple signal sources
- Two Capture/Compare/PWM (CCP) module:
 - 16-bit resolution for Capture/Compare modes
 - 10-bit resolution for PWM mode
- Four 10-Bit PWMs
- Numerically Controlled Oscillator (NCO):
 - Generates true linear frequency control and increased frequency resolution
 - Input Clock: 0 Hz < F_{NCO} < 32 MHz
 - Resolution: $F_{NCO}/2^{20}$
- One EUSART, RS-232, RS-485, LIN compatible

Digital Peripherals (Cont.)

- I/O Pins:
 - Individually programmable pull-ups
 - Slew rate control
 - Interrupt-on-change with edge-select
 - Input level selection control (ST or TTL)
 - Digital open-drain enable
- Peripheral Pin Select (PPS):
 - Enables pin mapping of digital I/O

Analog Peripherals

- Analog-to-Digital Converter (ADC):
 - 10-bit with up to 43 external channels
 - Operates in Sleep
- Up to two Comparators:
 - FVR, DAC and external input pin available on inverting and noninverting input
 - Software selectable hysteresis
 - Outputs available internally to other modules, or externally through PPS
- 5-Bit Digital-to-Analog Converter (DAC):
 - 5-bit resolution, rail-to-rail
 - Positive Reference Selection
 - Unbuffered I/O pin output
 - Internal connections to ADCs and comparators
- Voltage Reference:
 - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detect module:
 - AC high voltage zero-crossing detection for simplifying TRIAC control
 - Synchronized switching control and timing

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
 - Software selectable frequency range up to 32 MHz, $\pm 1\%$ typical
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External Oscillator Block with:
 - Three crystal/resonator modes up to 20 MHz
 - Three external clock modes up to 32 MHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if primary clock stops
- Oscillator Start-up Timer (OST):
 - Ensures stability of crystal oscillator resources

PIC16(L)F15313/23

TABLE 1: PIC16(L)F153XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (KW)	Program Flash Memory (KB)	Storage Area Flash (B)	Data SRAM (bytes)	I/OPins	10-bit ADC	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer	CCP/10-bit PWM	CWG	NCO	CLC	Zero-Cross Detect	Temperature Indicator	Memory Access Partition	Device Information Area	EUSART/ I ² C-SPI	Peripheral Pin Select	Peripheral Module Disable	Debug (1)
PIC16(L)F15313	(C)	2	3.5	224	256	6	5	1	1	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16(L)F15323	(C)	2	3.5	224	256	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16(L)F15324	(D)	4	7	224	512	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15325	(B)	8	14	224	1024	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15344	(D)	4	7	224	512	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15345	(B)	8	14	224	1024	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15354	(A)	4	7	224	512	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15355	(A)	8	14	224	1024	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15356	(E)	16	28	224	2048	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15375	(E)	8	14	224	1024	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15376	(E)	16	28	224	2048	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15385	(E)	8	14	224	1024	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15386	(E)	16	28	224	2048	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I

Note 1: I - Debugging integrated on chip.

Data Sheet Index:

- A:** DS40001853 [PIC16\(L\)F15354/5 Data Sheet, 28-Pin](#)
- B:** DS40001865 [PIC16\(L\)F15325/45 Data Sheet, 14/20-Pin](#)
- C:** DS40001897 [PIC16\(L\)F15313/23 Data Sheet, 8/14-Pin](#)
- D:** DS40001889 [PIC16\(L\)F15324/44 Data Sheet, 14/20-Pin](#)
- E:** DS40001866 [PIC16\(L\)F15356/75/76/85/86 Data Sheet, 28/40/48-Pin](#)

Note: For other small form-factor package availability and marking information, visit www.microchip.com/packaging or contact your local sales office.

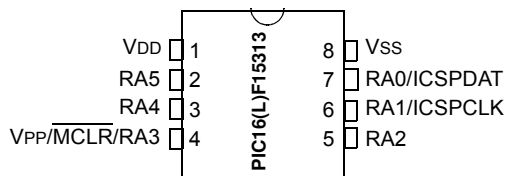
PIC16(L)F15313/23

TABLE 2: PACKAGES

Device	PDIP	SOIC	DFN	TSSOP	UQFN (4x4)
PIC16(L)F15313	•	•	•		
PIC16(L)F15323	•	•		•	•

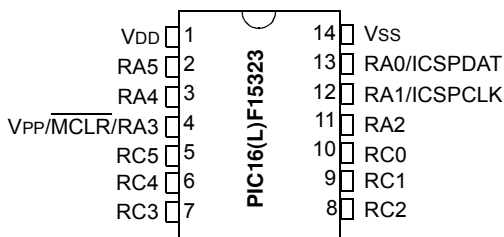
PIN DIAGRAMS

8-PIN PDIP, SOIC, MSOP



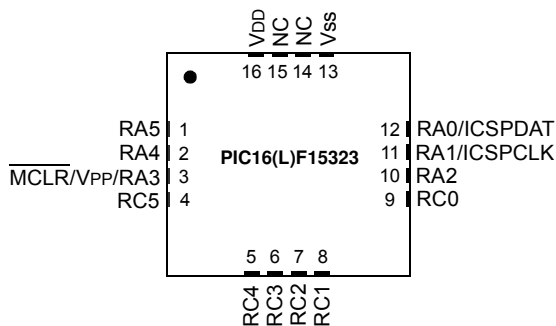
Note: See [Table 3](#) for location of all peripheral functions.

14-PIN PDIP, SOIC, TSSOP



Note: See [Table 4](#) for location of all peripheral functions.

16-PIN UQFN (4X4)



Note 1: See [Table 4](#) for location of all peripheral functions.

Note 2: It is recommended that the exposed bottom pad be connected to Vss.

PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F15313)

I/O ⁽²⁾	8-Pin PDIP/SOIC/MSOP	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	7	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	TX1/ CK1 ⁽¹⁾	CLCIN3 ⁽¹⁾	—	IOCA0	Y	ICSPDAT
RA1	6	ANA1	VREF+	C1IN0-	—	DAC1REF+	T0CK1 ⁽¹⁾	—	—	—	SCK1 ⁽⁴⁾ SCL1 ^(1,4)	—	RX1/ DT1 ⁽¹⁾	CLCIN2 ⁽¹⁾	—	IOCA1	Y	ICSPCLK
RA2	5	ANA2	—	—	—	—	—	—	—	CWG1IN ⁽¹⁾	SDA1 ^(1,4) SDI1 ⁽¹⁾	ZCD1	—	—	—	INT ⁽¹⁾ IOCA2	Y	—
RA3	4	—	—	—	—	—	—	—	—	—	SS1 ⁽¹⁾	—	—	CLCIN0 ⁽¹⁾	—	IOCA3	Y	MCLR V _{PP}
RA4	3	ANA4	—	C1IN1-	—	—	T1G ⁽¹⁾	—	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	ANA5 ADACT ⁽¹⁾	—	—	—	—	T1CK1 ⁽¹⁾ T2IN ⁽¹⁾	CCP1 ⁽¹⁾ CCP2 ⁽¹⁾	—	—	—	—	—	CLCIN1 ⁽¹⁾	—	IOCA5	Y	CLKIN OSC1 EIN
V _{DD}	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V _{DD}
V _{SS}	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V _{SS}
OUT ⁽²⁾	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3OUT	CWG1A	SDO1	—	DT1 ⁽³⁾	CLC1OUT	CLKR	—	—	—
	—	—	—	—	—	—	—	CCP2	PWM4OUT	CWG1B	SCK1	—	CK1	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	PWM5OUT	CWG1C	SCL1 ^(3,4)	—	TX1	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	PWM6OUT	CWG1D	SDA1 ^(3,4)	—	—	CLC4OUT	—	—	—	—

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I²C specific or SMBUS input buffer thresholds.

TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F15323)

I/O ⁽²⁾	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	T0CKI ⁽¹⁾	—	—	—	—	—	—	—	—	IOCA1	Y	ICSPCLK
RA2	11	10	ANA2	—	—	—	—	—	—	—	CWG1IN ⁽¹⁾	—	ZCD1	—	—	—	INT ⁽¹⁾ IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	2	ANA4	—	—	—	—	T1G ⁽¹⁾	—	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	T1CKI ⁽¹⁾ T2IN	—	—	—	—	—	—	CLCIN3 ⁽¹⁾	—	IOCA5	Y	CLKIN OSC1 EIN
RC0	10	9	ANC0	—	C2IN0+	—	—	—	—	—	—	SCK1 ⁽¹⁾ SCL1 ^(1,4)	—	TX2 ⁽¹⁾ CK2 ⁽¹⁾	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	SDA1 ^(1,4) SDI1 ⁽¹⁾	—	RX2 ⁽¹⁾ DT2 ⁽¹⁾	CLCIN2 ⁽¹⁾	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	—	CCP2 ⁽¹⁾	—	—	SS1 ⁽¹⁾	—	—	CLCIN0 ⁽¹⁾	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	—	—	—	—	—	TX1 ⁽¹⁾ CK1 ⁽¹⁾	CLCIN1 ⁽¹⁾	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	—	CCP1 ⁽¹⁾	—	—	—	—	RX1 ⁽¹⁾ DT1 ⁽¹⁾	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I²C specific or SMBUS input buffer thresholds.

TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F15323) (CONTINUED)

I/O ⁽²⁾	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT ⁽²⁾	—	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3OUT	CWG1A	SDO1	—	DT1 ⁽³⁾	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	CCP2	PWM4OUT	CWG1B	SCK1	—	CK1	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	PWM5OUT	CWG1C	SCL1 ^(3,4)	—	TX1	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	PWM6OUT	CWG1D	SDA1 ^(3,4)	—	DT2 ⁽³⁾	CLC4OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—	CK2	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—	—	TX2	—	—	—	—	—	—

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I²C specific or SMBUS input buffer thresholds.

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1.0 DEVICE OVERVIEW

The PIC16(L)F15313/23 are described within this data sheet. The PIC16(L)F15313/23 devices are available in 8/14-pin PDIP, SSOP, SOIC, DFN, and UQFN packages. [Figure 1-1](#) and [Figure 1-2](#) shows the block diagrams of the PIC16(L)F15313/23 devices. [Table 1-2](#) and [Table 1-3](#) shows the pinout descriptions.

Reference [Table 1-1](#) for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral	PIC16(L)F15313	PIC16(L)F15323
Analog-to-Digital Converter	•	•
Digital-to-Analog Converter (DAC1)	•	•
Fixed Voltage Reference (FVR)	•	•
Numerically Controlled Oscillator (NCO1)	•	•
Temperature Indicator Module (TIM)	•	•
Zero-Cross Detect (ZCD1)	•	•
Capture/Compare/PWM Modules (CCP)		
	CCP1	• •
	CCP2	• •
Comparator Module (Cx)		
	C1	• •
	C2	• •
Configurable Logic Cell (CLC)		
	CLC1	• •
	CLC2	• •
	CLC3	• •
	CLC4	• •
Complementary Waveform Generator (CWG)		
	CWG1	• •
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)		
	EUSART1	• •
Master Synchronous Serial Ports (MSSP)		
	MSSP1	• •
Pulse-Width Modulator (PWM)		
	PWM3	• •
	PWM4	• •
	PWM5	• •
	PWM6	• •
Timers		
	Timer0	• •
	Timer1	• •
	Timer2	• •

1.1 Register and Bit Naming Conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterNamebits.ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

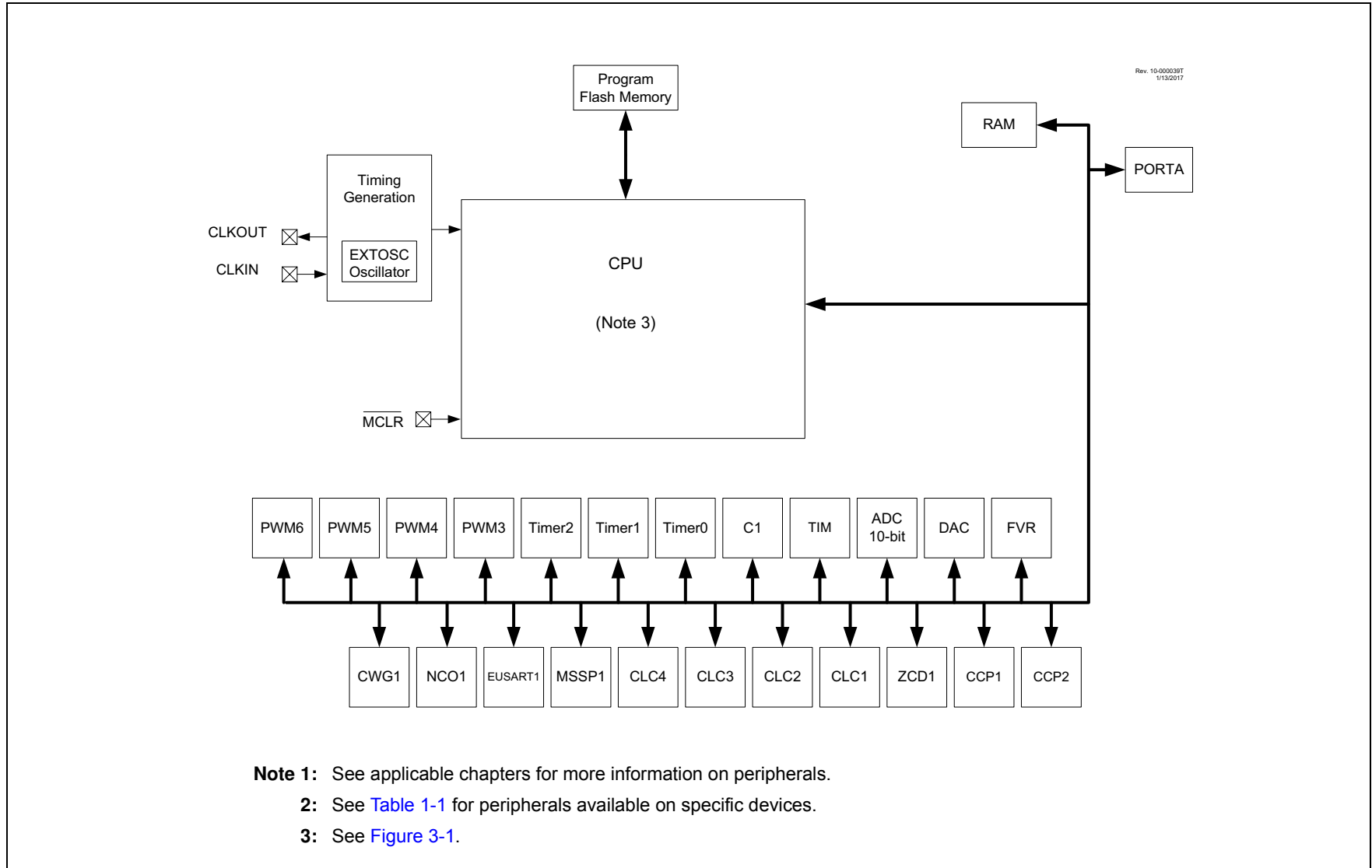
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

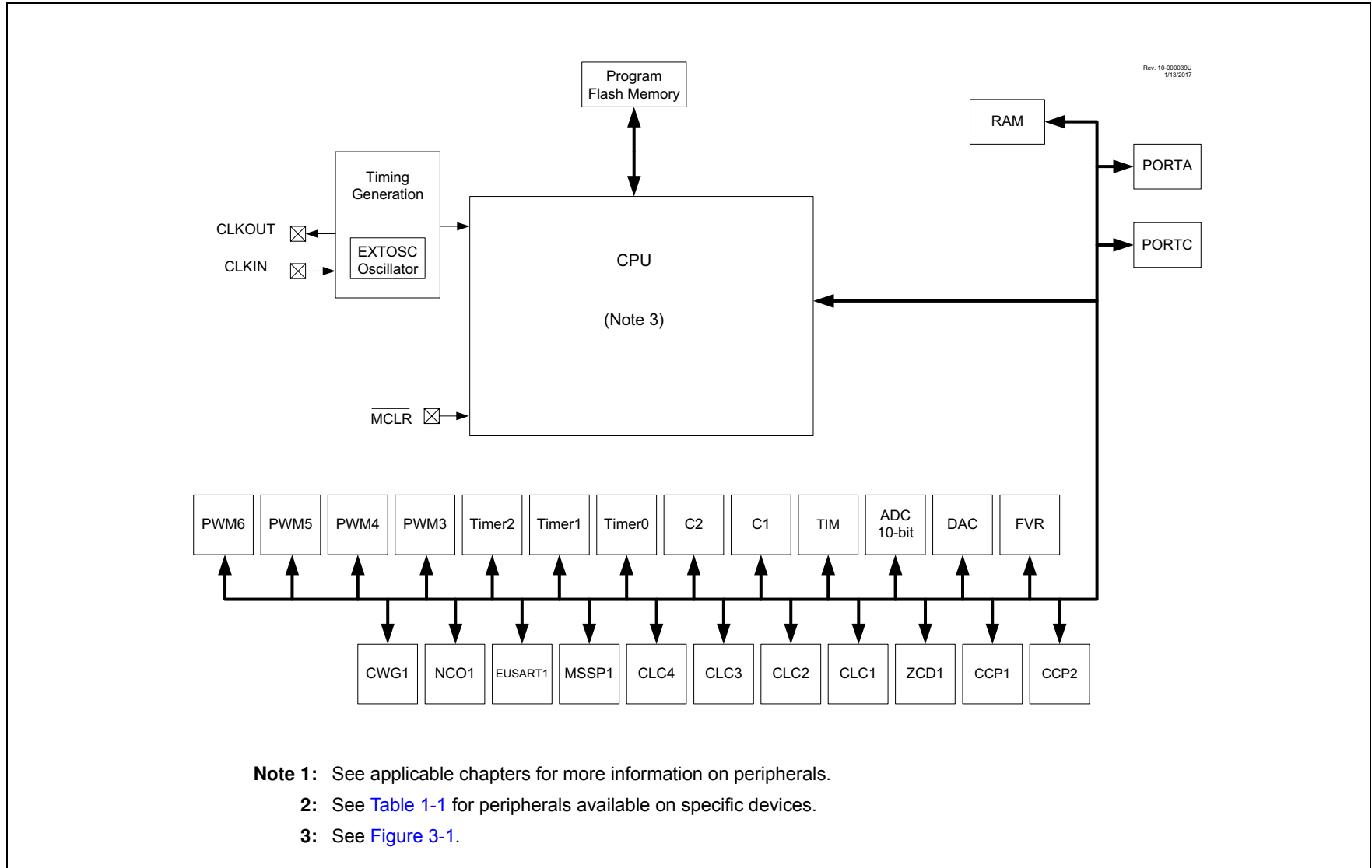
- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F15313 BLOCK DIAGRAM



- Note 1:** See applicable chapters for more information on peripherals.
2: See [Table 1-1](#) for peripherals available on specific devices.
3: See [Figure 3-1](#).

FIGURE 1-2: PIC16(L)F15323 BLOCK DIAGRAM



- Note 1:** See applicable chapters for more information on peripherals.
2: See [Table 1-1](#) for peripherals available on specific devices.
3: See [Figure 3-1](#).

TABLE 1-2: PIC16(L)F15313 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/TX1/ CK1 ⁽¹⁾ /CLCIN3 ⁽¹⁾ /ICSPDAT/IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0+	AN	—	Comparator 1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	TX1	—	CMOS	EUSART1 asynchronous transmit.
	CK1 ⁽¹⁾	TTL/ST	CMOS/OD	EUSART1 synchronous mode clock input/output.
	CLCIN3 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ and debugging data input/output.
RA1/ANA1/VREF+/C1IN0-/DAC1REF+/ T0CK1 ⁽¹⁾ /SCK1 ⁽⁴⁾ /SCL1 ^(1,4) /RX1/ DT1 ⁽¹⁾ /CLCIN2 ⁽¹⁾ /ICSPCLK/IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	C1IN0-	AN	—	Comparator 1 negative input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
	T0CK1 ⁽¹⁾	TTL/ST	—	Timer0 clock input.
	SCK1 ⁽⁴⁾	I ² C	OD	I ² C, OD, MSSP1 I ² C input/output.
	SCL1 ^(1,4)	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	RX1	TTL/ST	—	EUSART1 Asynchronous mode receiver data input.
	DT1 ⁽¹⁾	TTL/ST	CMOS/OD	EUSART1 Synchronous mode data input/output.
	CLCIN2 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
RA2/ANA2/CWG1IN ⁽¹⁾ /SDA1 ^(1,4) / SDI1 ⁽¹⁾ /ZCD1/INT ⁽¹⁾ /IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	CWG1IN ⁽¹⁾	TTL/ST	—	Complementary Waveform Generator 1 input.
	SDA1 ^(1,4)	I ² C	OD	MSSP1 I ² C serial data input/output.
	SDI1 ⁽¹⁾	TTL/ST	—	MSSP1 SPI serial data input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/source).
	INT ⁽¹⁾	TTL/ST	—	External interrupt request input.
	IOCA2	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 15-3](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 15-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F15313 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA3/ $\overline{SS1}^{(1)}$ /CLCIN0 ⁽¹⁾ /VPP/ \overline{MCLR} /IOCA3	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	$\overline{SS1}^{(1)}$	TTL/ST	—	MSSP1 SPI slave select input.
	CLCIN0 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	VPP	HV	—	ICSP™ High-Voltage Programming mode entry input.
	\overline{MCLR}	ST	—	Master clear input with internal weak pull up resistor.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
RA4/ANA4/C1IN1-/T1G ⁽¹⁾ /CLKOUT/OSC2/IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	T1G ⁽¹⁾	ST	—	Timer1 Gate input.
	CLKOUT	—	CMOS/OD	Fosc/4 digital output (in non-crystal/resonator modes).
	OSC2	—	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
RA5/ANA5/ADACT ⁽¹⁾ /T1CKI ⁽¹⁾ /T2IN ⁽¹⁾ /CCP1 ⁽¹⁾ /CCP2 ⁽¹⁾ /CLCIN1 ⁽¹⁾ /CLKIN/OSC1/EIN/IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	ADACT ⁽¹⁾	TTL/ST	—	ADC Auto-Conversion Trigger input.
	T1CKI ⁽¹⁾	TTL/ST	—	Timer1 external digital clock input.
	T2IN ⁽¹⁾	TTL/ST	—	Timer2 external input.
	CCP1 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM1 (default input location for capture function).
	CCP2 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM2 (default input location for capture function).
	CLCIN1 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	CLKIN	TTL/ST	—	External digital clock input.
	OSC1	XTAL	—	External Crystal/Resonator (LP, XT, HS modes) driver input.
	EIN	TTL/ST	—	External digital clock input.
IOCA5	TTL/ST	—	Interrupt-on-change input.	
VDD	VDD	Power	—	Positive supply voltage input.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 15-3](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 15-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 1-2: PIC16(L)F15313 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT ⁽²⁾	C1OUT	—	CMOS/OD	Comparator 1 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	DT1 ⁽³⁾	—	CMOS/OD	EUSART Synchronous mode data output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	SCL1 ^(3,4)	—	CMOS/OD	MSSP1 I ² C output.
	SDA1 ^(3,4)	—	CMOS/OD	MSSP1 I ² C output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP1 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	PWM5OUT	—	CMOS/OD	PWM5 output.
	PWM6OUT	—	CMOS/OD	PWM6 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.	
NCO1OUT	—	CMOS/OD	Numerically Controller Oscillator output.	
CLKR	—	CMOS/OD	Clock Reference module output.	

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
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 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 1-3: PIC16(L)F15323 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/ICSPDAT/IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0+	AN	—	Comparator 1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ and debugging data input/output.
RA1/ANA1/VREF+/C1IN0-/C2IN0-/DAC1REF+/T0CKI ⁽¹⁾ /ICSPCLK/IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	C1IN0-	AN	—	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
	T0CKI ⁽¹⁾	TTL/ST	—	Timer0 clock input.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
RA2/ANA2/CWG1IN ⁽¹⁾ /ZCD1/INT ⁽¹⁾ /IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	CWG1IN ⁽¹⁾	TTL/ST	—	Complementary Waveform Generator 1 input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/source).
	INT ⁽¹⁾	TTL/ST	—	External interrupt request input.
RA3/MCLR/VPP/IOCA3	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	MCLR	ST	—	Master clear input with internal weak pull up resistor.
	VPP	HV	—	ICSP™ High-Voltage Programming mode entry input.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
RA4/ANA4/T1G ⁽¹⁾ /CLKOUT/OSC2/IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T1G ⁽¹⁾	ST	—	Timer1 Gate input.
	CLKOUT	—	CMOS/OD	Fosc/4 digital output (in non-crystal/resonator modes).
	OSC2	—	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
IOCA4	TTL/ST	—	Interrupt-on-change input.	

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 15-3](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 15-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 1-3: PIC16(L)F15323 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/ANA5/T1CK1 ⁽¹⁾ /T2IN/CLCIN3 ⁽¹⁾ /CLKIN/OSC1/EIN/IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	T1CK1 ⁽¹⁾	TTL/ST	—	Timer1 external digital clock input.
	T2IN	TTL/ST	—	Timer2 external input.
	CLCIN3 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	CLKIN	TTL/ST	—	External digital clock input.
	OSC1	XTAL	—	External Crystal/Resonator (LP, XT, HS modes) driver input.
	EIN	TTL/ST	—	External digital clock input.
RC0/ANC0/C2IN0+/SCL1 ^(1,4) /SCK1 ⁽¹⁾ /IOCC0	RC0	TTL/ST	CMOS/OD	General purpose I/O.
	ANC0	AN	—	ADC Channel C0 input.
	C2IN0+	AN	—	Comparator 2 positive input.
	SCL1 ^(1,4)	I ² C	OD	I ² C, OD, MSSP1 I ² C input/output.
	SCK1 ⁽¹⁾	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	IOCC0	TTL/ST	—	Interrupt-on-change input.
RC1/ANC1/C1IN1-/C2IN1-/SDA1 ^(1,4) /SDI1 ⁽¹⁾ /CLCIN2 ⁽¹⁾ /IOCC1	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	ANC1	AN	—	ADC Channel C1 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	SDA1 ^(1,4)	I ² C	OD	MSSP1 I ² C serial data input/output.
	SDI1 ⁽¹⁾	TTL/ST	—	MSSP1 SPI serial data input.
	CLCIN2 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	IOCC1	TTL/ST	—	Interrupt-on-change input.
RC2/ANC2/C1IN2-/C2IN2-/IOCC2	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	ANC2	AN	—	ADC Channel C2 input.
	C1IN2-	AN	—	Comparator 1 negative input.
	C2IN2-	AN	—	Comparator 2 negative input.
	IOCC2	TTL/ST	—	Interrupt-on-change input.

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HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 15-3](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pins options as described in [Table 15-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 1-3: PIC16(L)F15323 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC3/ANC3/C1IN3-/C2IN3-/CCP2 ⁽¹⁾ / SS1 ⁽¹⁾ /CLCIN0 ⁽¹⁾ /IOCC3	RC3	TTL/ST	CMOS/OD	General purpose I/O.
	ANC3	AN	—	ADC Channel C3 input.
	C1IN3-	AN	—	Comparator 1 positive input.
	C2IN3-	AN	—	Comparator 2 positive input.
	CCP2 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM2 (default input location for capture function).
	SS1 ⁽¹⁾	TTL/ST	—	MSSP1 SPI slave select input.
	CLCIN0 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
RC4/ANC4/TX1 ⁽¹⁾ /CK1 ⁽¹⁾ /CLCIN1 ⁽¹⁾ / IOCC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
	TX1	—	CMOS	EUSART1 asynchronous transmit.
	CLCIN1 ⁽¹⁾	TTL/ST	—	Configurable Logic Cell source input.
	CK1 ⁽¹⁾	TTL/ST	CMOS/OD	EUSART1 synchronous mode clock input/output.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
RC5/ANC5/CCP1 ⁽¹⁾ /RX1 ⁽¹⁾ /DT1 ⁽¹⁾ / IOCC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	CCP1 ⁽¹⁾	TTL/ST	CMOS/OD	Capture/compare/PWM1 (default input location for capture function).
	RX1 ⁽¹⁾	TTL/ST	—	EUSART1 Asynchronous mode receiver data input.
	DT1 ⁽¹⁾	TTL/ST	CMOS/OD	EUSART1 Synchronous mode data input/output.
	IOCC5	TTL/ST	—	Interrupt-on-change input.
VDD	Vbd	Power	—	Positive supply voltage input.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
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- Note**
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TABLE 1-3: PIC16(L)F15323 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT ⁽²⁾	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	DT1 ⁽³⁾	—	CMOS/OD	EUSART Synchronous mode data output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	SCL1 ^(3,4)	—	CMOS/OD	MSSP1 I ² C output.
	SDA1 ^(3,4)	—	CMOS/OD	MSSP1 I ² C output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP1 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	PWM5OUT	—	CMOS/OD	PWM5 output.
	PWM6OUT	—	CMOS/OD	PWM6 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.	
NCO1OUT	—	CMOS/OD	Numerically Controller Oscillator output.	
CLKR	—	CMOS/OD	Clock Reference module output.	

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note** 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 15-3](#) for details on which PORT pins may be used for this signal.
- 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 15-3](#).
- 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
- 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

2.0 GUIDELINES FOR GETTING STARTED WITH PIC16(L)F15313/23 MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F15313/23 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see [Section 2.2 “Power Supply Pins”](#))
- MCLR pin (see [Section 2.3 “Master Clear \(MCLR\) Pin”](#))

These pins must also be connected if they are being used in the end application:

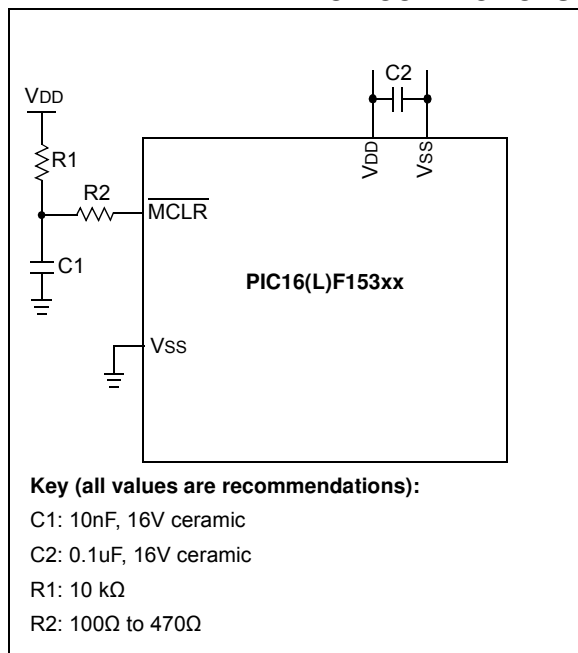
- ICSPCLK/ICSPDAT pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see [Section 2.4 “ICSP™ Pins”](#))
- OSCI and OSCO pins when an external oscillator source is used (see [Section 2.5 “External Oscillator Pins”](#))

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in [Figure 2-1](#).

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 10-25V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.

2.3 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

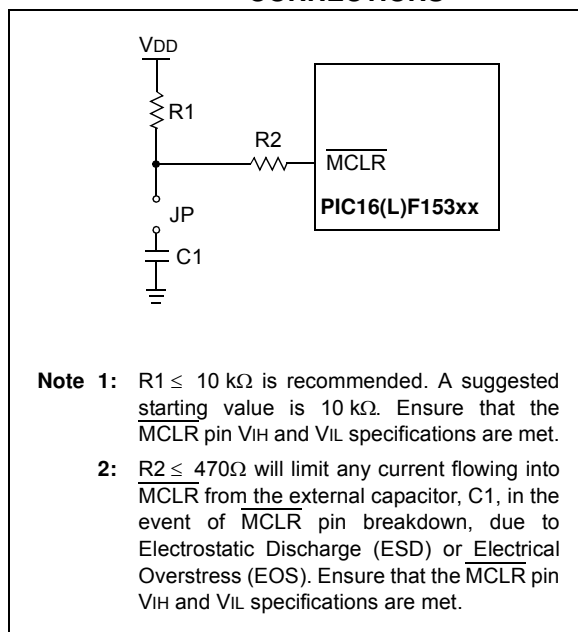
The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

For device emulation, ensure that the “Communication Channel Select” (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to Section 39.0 “Development Support”.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to [Section 9.0 “Oscillator Module \(with Fail-Safe Clock Monitor\)”](#) for details). The PIC16(L)F15313/23 devices do not have a secondary oscillator.

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in [Figure 2-3](#). In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

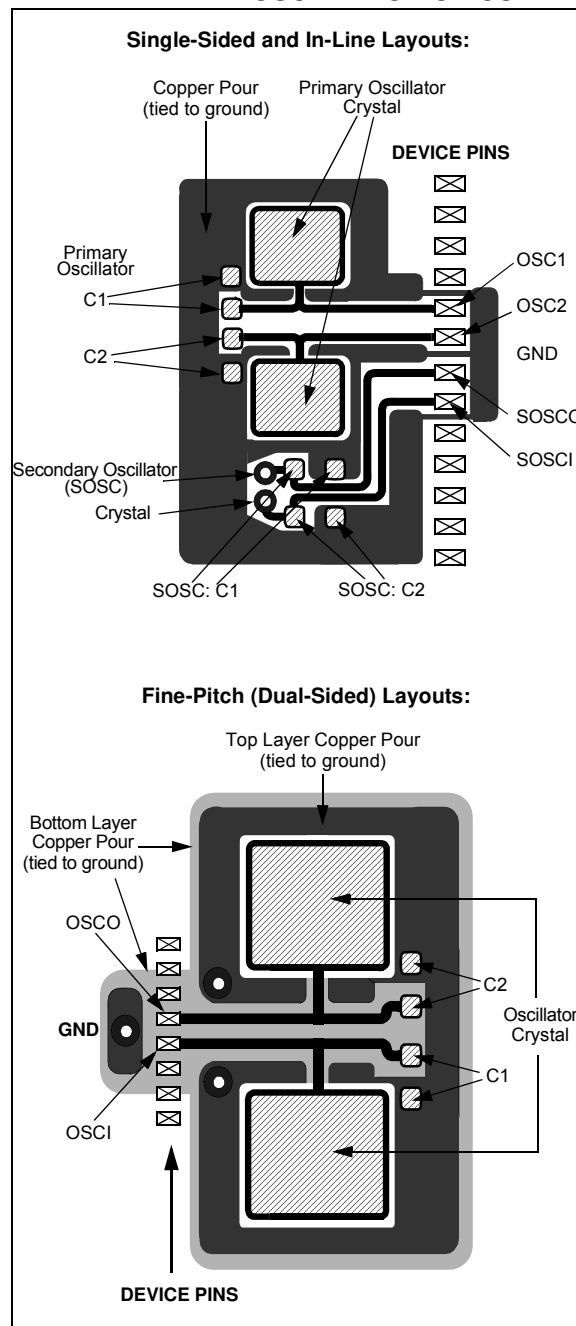
For additional information and design guidance on oscillator circuits, refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices”
- AN849, “Basic PICmicro® Oscillator Design”
- AN943, “Practical PICmicro® Oscillator Analysis and Design”
- AN949, “Making Your Oscillator Work”

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving.

The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 3-1: CORE DATA PATH DIAGRAM

