Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


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# PIC16(L)F15325/45

## Full-Featured 14/20-Pin Microcontrollers

### Description

PIC16(L)F15325/45 microcontrollers feature Analog, Core Independent Peripherals and Communication Peripherals, combined with eXtreme Low-Power (XLP) technology for a wide range of general purpose and low-power applications.

The devices feature multiple PWMs, multiple communication, temperature sensor, and memory features like Memory Access Partition (MAP) to support customers in data protection and bootloader applications, and Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 48 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - 8-bit Timer2 with Hardware Limit Timer (HLT)
  - 16-bit Timer0/1
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software
- Programmable Code Protection

### Memory

- Up to 14 KB Flash Program Memory
- Up to 1 KB Data SRAM
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write protect
  - Customizable Partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF15325/45)
  - 2.3V to 5.5V (PIC16F15325/45)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### Power-Saving Functionality

- DOZE mode: Ability to Run the CPU Core Slower than the System Clock
- IDLE mode: Ability to halt CPU Core while Internal Peripherals Continue Operating
- SLEEP mode: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to disable hardware module to minimize active power consumption of unused peripherals

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 32 μA/MHz @ 1.8V, typical

### Digital Peripherals

- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Two Capture/Compare/PWM (CCP) module:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Four 10-Bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0 Hz < $F_{NCO}$ < 32 MHz
  - Resolution: $F_{NCO}/2^{20}$
- Two EUSART, RS-232, RS-485, LIN compatible
- One SPI
- One $I^2C$, SMBus, PMBus™ compatible

## Digital Peripherals (Cont.)

- I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

## Analog Peripherals

- Analog-to-Digital Converter (ADC):
  - 10-bit with up to 43 external channels
  - Operates in Sleep
- Two Comparators:
  - FVR, DAC and external input pin available on inverting and noninverting input
  - Software selectable hysteresis
  - Outputs available internally to other modules, or externally through PPS
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detect module:
  - AC high voltage zero-crossing detection for simplifying TRIAC control
  - Synchronized switching control and timing

## Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Software selectable frequency range up to 32 MHz, ±1% typical
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 32 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if primary clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator resources

**TABLE 1: PIC16(L)F153XX FAMILY TYPES**

| Device | Data Sheet Index | Program Flash Memory (KW) | Program Flash Memory (KB) | Storage Area Flash (B) | Data SRAM (bytes) | I/OPins | 10-bit ADC | 5-bit DAC | Comparator | 8-bit/ (with HLT) Timer | 16-bit Timer | Window Watchdog Timer | CCP/10-bit PWM | CWG | NCO | CLC | Zero-Cross Detect | Temperature Indicator | Memory Access Partition | Device Information Area | EUSART/ $I^2C$-SPI | Peripheral Pin Select | Peripheral Module Disable | Debug (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC16(L)F15313 | (C) | 2 | 3.5 | 224 | 256 | 6 | 5 | 1 | 1 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 1/1 | Y | Y | I |
| PIC16(L)F15323 | (C) | 2 | 3.5 | 224 | 256 | 12 | 11 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 1/1 | Y | Y | I |
| PIC16(L)F15324 | (D) | 4 | 7 | 224 | 512 | 12 | 11 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/1 | Y | Y | I |
| PIC16(L)F15325 | (B) | 8 | 14 | 224 | 1024 | 12 | 11 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/1 | Y | Y | I |
| PIC16(L)F15344 | (D) | 4 | 7 | 224 | 512 | 18 | 17 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/1 | Y | Y | I |
| PIC16(L)F15345 | (B) | 8 | 14 | 224 | 1024 | 18 | 17 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/1 | Y | Y | I |
| PIC16(L)F15354 | (A) | 4 | 7 | 224 | 512 | 25 | 24 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |
| PIC16(L)F15355 | (A) | 8 | 14 | 224 | 1024 | 25 | 24 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |
| PIC16(L)F15356 | (E) | 16 | 28 | 224 | 2048 | 25 | 24 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |
| PIC16(L)F15375 | (E) | 8 | 14 | 224 | 1024 | 36 | 35 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |
| PIC16(L)F15376 | (E) | 16 | 28 | 224 | 2048 | 36 | 35 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |
| PIC16(L)F15385 | (E) | 8 | 14 | 224 | 1024 | 44 | 43 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |
| PIC16(L)F15386 | (E) | 16 | 28 | 224 | 2048 | 44 | 43 | 1 | 2 | 1 | 2 | Y | 2/4 | 1 | 1 | 4 | Y | Y | Y | Y | 2/2 | Y | Y | I |

**Note 1:** I - Debugging integrated on chip.

**Data Sheet Index:**

- **A: DS40001853** PIC16(L)F15354/5 Data Sheet, 28-Pin
- **B: DS40001865** PIC16(L)F15325/45 Data Sheet, 14/20-Pin
- **C:** Future Release PIC16(L)F15313/23 Data Sheet, 8/14-Pin
- **D:** Future Release PIC16(L)F15324/44 Data Sheet, 14/20-Pin
- **E: DS40001866** PIC16(L)F15356/75/76/85/86 Data Sheet, 28/40/48-Pin

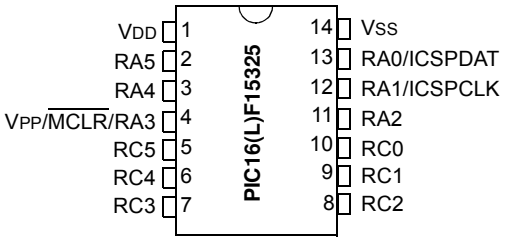
**Note:** For other small form-factor package availability and marking information, visit www.microchip.com/packaging or contact your local sales office.

**TABLE 2: PACKAGES**

| Device | PDIP | SOIC | SSOP | TSSOP | UQFN (4x4) |
|---|---|---|---|---|---|
| PIC16(L)F15325 | • | • | | • | • |
| PIC16(L)F15345 | • | • | • | | • |

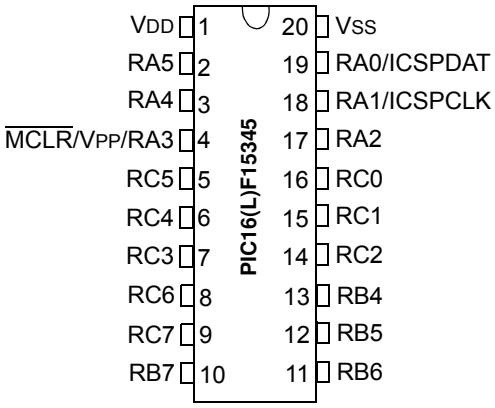
## PIN DIAGRAMS

**14-PIN PDIP, SOIC, TSSOP**



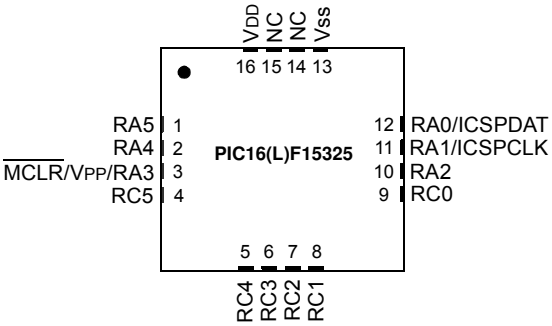

**Note:** See Table 3 for location of all peripheral functions.

**20-PIN PDIP, SOIC, SSOP**




**Note:** See Table 4 for location of all peripheral functions.

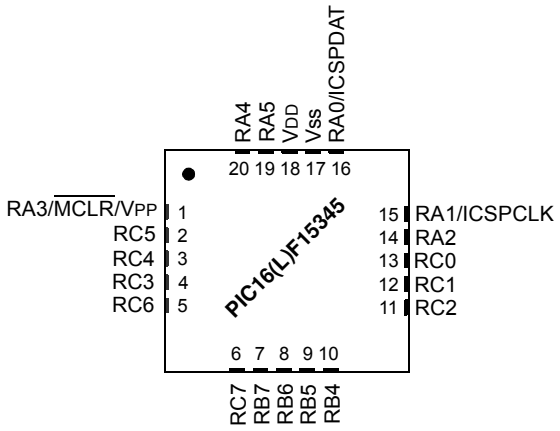
**16-PIN UQFN (4X4)**




**Note 1:** See Table 3 for location of all peripheral functions.

**2:** It is recommended that the exposed bottom pad be connected to VSS.

**20-PIN UQFN (4x4)**




**Note 1:** See Table 4 for location of all peripheral functions.

**2:** It is recommended that the exposed bottom pad be connected to VSS.

## PIN ALLOCATION TABLES

### TABLE 3: 14/16-PIN ALLOCATION TABLE (PIC16(L)F15325)

| I/O(2) | 14-Pin PDIP/SOIC/TSSOP | 16-Pin QFN/UQFN | ADC | Reference | Comparator | NCO | DAC | Timers | CCP | PWM | CWG | MSSP | ZCD | EUSART | CLC | CLKR | Interrupt | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA0 | 13 | 12 | ANA0 | — | C1IN0+ | — | DAC1OUT | — | — | — | — | — | — | — | — | — | IOCA0 | Y | ICSPDAT |
| RA1 | 12 | 11 | ANA1 | VREF+ | C1IN0-<br>C2IN0- | — | DAC1REF+ | T0CKI(1) | — | — | — | — | — | — | — | — | IOCA1 | Y | ICSPCLK |
| RA2 | 11 | 10 | ANA2 | — | — | — | — | — | — | — | CWG1IN(1) | — | ZCD1 | — | — | — | INT(1)<br>IOCA2 | Y | — |
| RA3 | 4 | 3 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | IOCA3 | Y | $\overline{\text{MCLR}}$<br>VPP |
| RA4 | 3 | 2 | ANA4 | — | C1IN1- | — | — | T1G(1)<br>SOSCO | — | — | — | — | — | — | — | — | IOCA4 | Y | CLKOUT<br>OSC2 |
| RA5 | 2 | 1 | ANA5 | — | — | — | — | T1CKI(1)<br>T2IN<br>SOSCIN | | — | — | — | — | — | CLCIN3(1) | — | IOCA5 | Y | CLKIN<br>OSC1<br>EIN |
| RC0 | 10 | 9 | ANC0 | — | C2IN0+ | — | — | — | — | — | — | SCK1(1)<br>SCL1(1,4) | — | — | — | — | IOCC0 | Y | — |
| RC1 | 9 | 8 | ANC1 | — | C1IN1-<br>C2IN1- | — | — | — | — | — | — | SDA1(1,4)<br>SDI1(1) | — | — | CLCIN2(1) | — | IOCC1 | Y | — |
| RC2 | 8 | 7 | ANC2 | — | C1IN2-<br>C2IN2- | — | — | — | — | — | — | — | — | — | — | — | IOCC2 | Y | — |
| RC3 | 7 | 6 | ANC3 | — | C1IN3-<br>C2IN3- | — | — | — | CCP2(1) | — | — | $\overline{\text{SS1}}$(1) | — | — | CLCIN0(1) | — | IOCC3 | Y | — |
| RC4 | 6 | 5 | ANC4 | — | — | — | — | — | — | — | — | — | — | TX1(1)<br>CK1(1) | CLCIN1(1) | — | IOCC4 | Y | — |
| RC5 | 5 | 4 | ANC5 | — | — | — | — | — | CCP1(1) | — | — | — | — | RX1(1)<br>DT1(1) | — | — | IOCC5 | Y | — |
| VDD | 1 | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VDD |
| VSS | 14 | 13 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VSS |

**Note 1:** This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
**2:** All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
**4:** These pins are configured for $I^2C$ logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the $I^2C$ specific or SMBUS input buffer thresholds.

**TABLE 3: 14/16-PIN ALLOCATION TABLE (PIC16(L)F15325) (CONTINUED)**

| I/O[2] | 14-Pin PDIP/SOIC/TSSOP | 16-Pin QFN/UQFN | ADC | Reference | Comparator | NCO | DAC | Timers | CCP | PWM | CWG | MSSP | ZCD | EUSART | CLC | CLKR | Interrupt | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OUT[2] | — | — | — | — | C1OUT | NCO1OUT | — | TMR0 | CCP1 | PWM3OUT | CWG1A | SDO1 | — | DT1[3]<br>DT2[3] | CLC1OUT | CLKR | — | — | — |
| | — | — | — | — | C2OUT | — | — | — | CCP2 | PWM4OUT | CWG1B | SCK1 | — | CK1<br>CK2 | CLC2OUT | — | — | — | — |
| | — | — | — | — | — | — | — | — | — | PWM5OUT | CWG1C | SCL1[3,4] | — | TX1<br>TX2 | CLC3OUT | — | — | — | — |
| | — | — | — | — | — | — | — | — | — | PWM6OUT | CWG1D | SDA1[3,4] | — | — | CLC4OUT | — | — | — | — |

**Note 1:** This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
**2:** All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
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**TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F15345)**

| I/O(2) | 20-Pin PDIP/SOIC/SSOP | 20-Pin UQFN | ADC | Reference | Comparator | NCO | DAC | Timers | CCP | PWM | CWG | MSSP | ZCD | EUSART | CLC | CLKR | Interrupt | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA0 | 19 | 16 | ANA0 | — | C1IN0+ | — | DAC1OUT | — | — | — | — | — | — | — | — | — | IOCA0 | Y | ICSPDAT |
| RA1 | 18 | 15 | ANA1 | VREF+ | C1IN0-<br>C2IN0- | — | DAC1REF+ | T0CKI(1) | — | — | — | — | — | — | — | — | IOCA1 | Y | ICSPCLK |
| RA2 | 17 | 14 | ANA2 | — | — | — | — | — | — | — | CWG1IN(1) | — | ZCD1 | — | CLCIN0(1) | — | INT(1)<br>IOCA2 | Y | — |
| RA3 | 4 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | IOCA3 | Y | $\overline{\text{MCLR}}$ VPP |
| RA4 | 3 | 20 | ANA4 | — | C1IN1- | — | — | T1G(1)<br>SOSCO | — | — | — | — | — | — | — | — | IOCA4 | Y | CLKOUT<br>OSC2 |
| RA5 | 2 | 19 | ANA5 | — | — | — | — | T1CKI(1)<br>T2IN<br>SOSCIN | | — | — | — | — | — | — | — | IOCA5 | Y | CLKIN<br>OSC1<br>EIN |
| RB4 | 13 | 10 | ANB4<br>ADACT(1) | — | — | — | — | — | — | — | — | SCK1(1)<br>SCL1(1,4) | — | — | CLCIN2(1) | — | IOCB4 | — | — |
| RB5 | 12 | 9 | ANB5 | — | — | — | — | — | — | — | — | — | — | RX2(1)<br>DT2(1) | CLCIN3(1) | — | IOCB5 | — | — |
| RB6 | 11 | 8 | ANB6 | — | — | — | — | — | — | — | — | SDA1(1,4)<br>SDI1(1) | — | — | — | — | IOCB6 | Y | — |
| RB7 | 10 | 7 | ANB7 | — | — | — | — | — | — | — | — | — | — | TX2(1)<br>CK2(1) | — | — | IOCB7 | Y | — |
| RC0 | 16 | 13 | ANC0 | — | C2IN0+ | — | — | — | — | — | — | — | — | — | — | — | IOCC0 | Y | — |
| RC1 | 15 | 12 | ANC1 | — | C1IN1-<br>C2IN1- | — | — | — | — | — | — | — | — | — | — | — | IOCC1 | Y | — |
| RC2 | 14 | 11 | ANC2 | — | C1IN2-<br>C2IN2- | — | — | — | — | — | — | — | — | — | — | — | IOCC2 | Y | — |
| RC3 | 7 | 4 | ANC3 | — | C1IN3-<br>C2IN3- | — | — | — | CCP2(1) | — | — | — | — | — | CLCIN1(1) | — | IOCC3 | Y | — |
| RC4 | 6 | 3 | ANC4 | — | — | — | — | — | — | — | — | — | — | — | — | — | IOCC4 | Y | — |
| RC5 | 5 | 2 | ANC5 | — | — | — | — | — | CCP1(1) | — | — | — | — | — | — | — | IOCC5 | Y | — |
| RC6 | 8 | 5 | ANC6 | — | — | — | — | — | — | — | — | $\overline{\text{SS1}}$(1) | — | — | — | — | IOCC6 | Y | — |
| RC7 | 9 | 6 | ANC7 | — | — | — | — | — | — | — | — | — | — | — | — | — | IOCC7 | Y | — |

**Note 1:** This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
**2:** All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
**4:** These pins are configured for $I^2C$ logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the $I^2C$ specific or SMBUS input buffer thresholds.

**TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F15345) (CONTINUED)**

| I/O(2) | 20-Pin PDIP/SOIC/SSOP | 20-Pin UQFN | ADC | Reference | Comparator | NCO | DAC | Timers | CCP | PWM | CWG | MSSP | ZCD | EUSART | CLC | CLKR | Interrupt | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VDD | 1 | 18 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VDD |
| VSS | 20 | 17 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VSS |
| OUT(2) | — | — | — | — | C1OUT | NCO1OUT | — | TMR0 | CCP1 | PWM3OUT | CWG1A | SDO1 | — | DT1(3)<br>DT2(3) | CLC1OUT | CLKR | — | — | — |
| | — | — | — | — | C2OUT | — | — | — | CCP2 | PWM4OUT | CWG1B | SCK1 | — | CK1<br>CK2 | CLC2OUT | — | — | — | — |
| | — | — | — | — | — | — | — | — | — | PWM5OUT | CWG1C | SCL1(3,4) | — | TX1<br>TX2 | CLC3OUT | — | — | — | — |
| | — | — | — | — | — | — | — | — | — | PWM6OUT | CWG1D | SDA1(3,4) | — | — | CLC4OUT | — | — | — | — |

**Note 1:** This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
**2:** All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
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To determine if an errata sheet exists for a particular device, please check with one of the following:

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## 1.0 DEVICE OVERVIEW

The PIC16(L)F15325/45 are described within this data sheet. The PIC16(L)F15325/45 devices are available in 14/20-pin PDIP, SSOP, SOIC, TSSOP, and UQFN packages. Figure 1-1 and Figure 1-2 shows the block diagrams of the PIC16(L)F15325/45 devices. Table 1-2 and Table 1-3 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

**TABLE 1-1: DEVICE PERIPHERAL SUMMARY**

| Peripheral | | PIC16(L)F15325/45 |
|---|---|---|
| Analog-to-Digital Converter | | • |
| Digital-to-Analog Converter (DAC1) | | • |
| Fixed Voltage Reference (FVR) | | • |
| Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1 and EUSART2) | | • |
| Numerically Controlled Oscillator (NCO1) | | • |
| Temperature Indicator Module (TIM) | | • |
| Zero-Cross Detect (ZCD1) | | • |
| Capture/Compare/PWM Modules (CCP) | | |
| | CCP1 | • |
| | CCP2 | • |
| Comparator Module (Cx) | | |
| | C1 | • |
| | C2 | • |
| Configurable Logic Cell (CLC) | | |
| | CLC1 | • |
| | CLC2 | • |
| | CLC3 | • |
| | CLC4 | • |
| Complementary Waveform Generator (CWG) | | |
| | CWG1 | • |
| Master Synchronous Serial Ports (MSSP) | | |
| | MSSP1 | • |
| Pulse-Width Modulator (PWM) | | |
| | PWM3 | • |
| | PWM4 | • |
| | PWM5 | • |
| | PWM6 | • |
| Timers | | |
| | Timer0 | • |
| | Timer1 | • |
| | Timer2 | • |

## 1.1 Register and Bit Naming Conventions

### 1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

### 1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

#### 1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

#### 1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

#### 1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

### 1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

#### 1.1.3.1 Status, Interrupt, and Mirror Bits

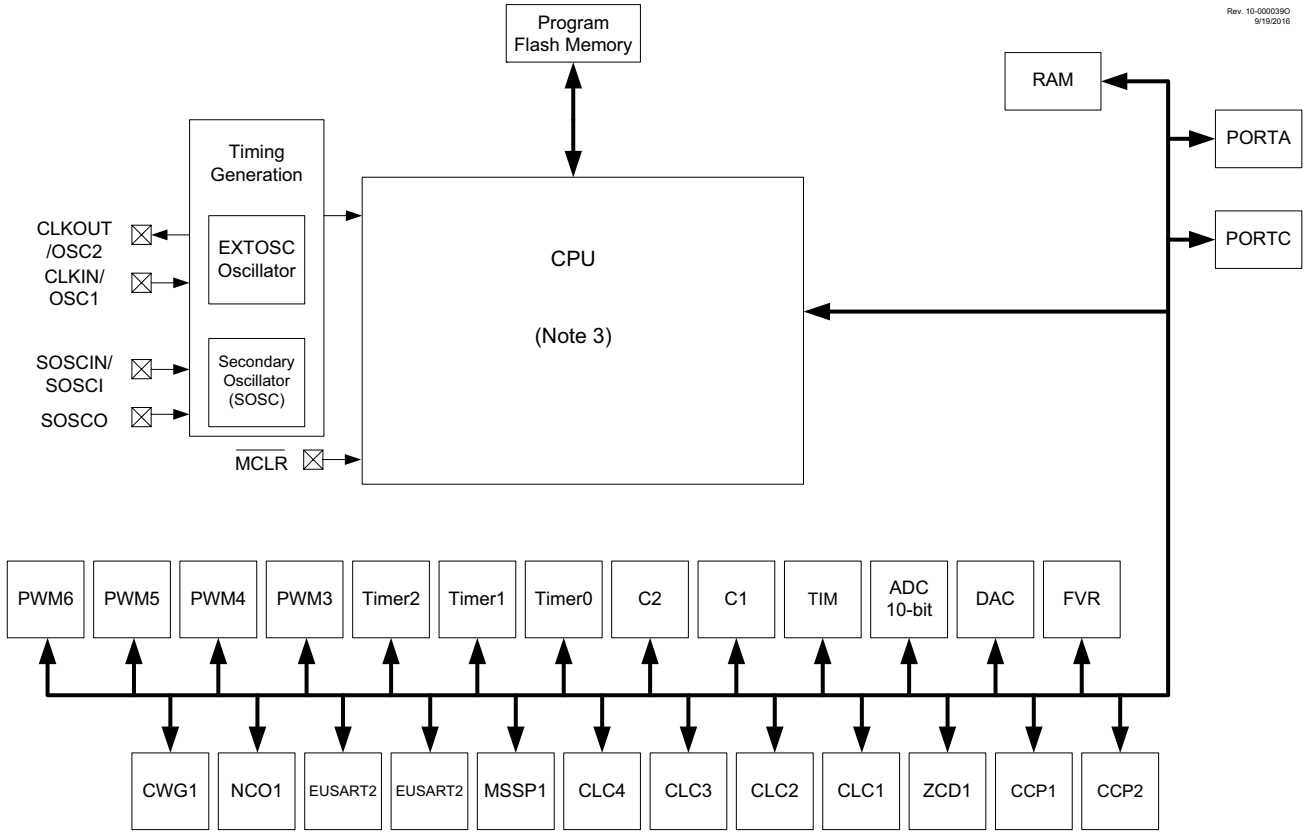
Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

#### 1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

**FIGURE 1-1: PIC16(L)F15325 BLOCK DIAGRAM**

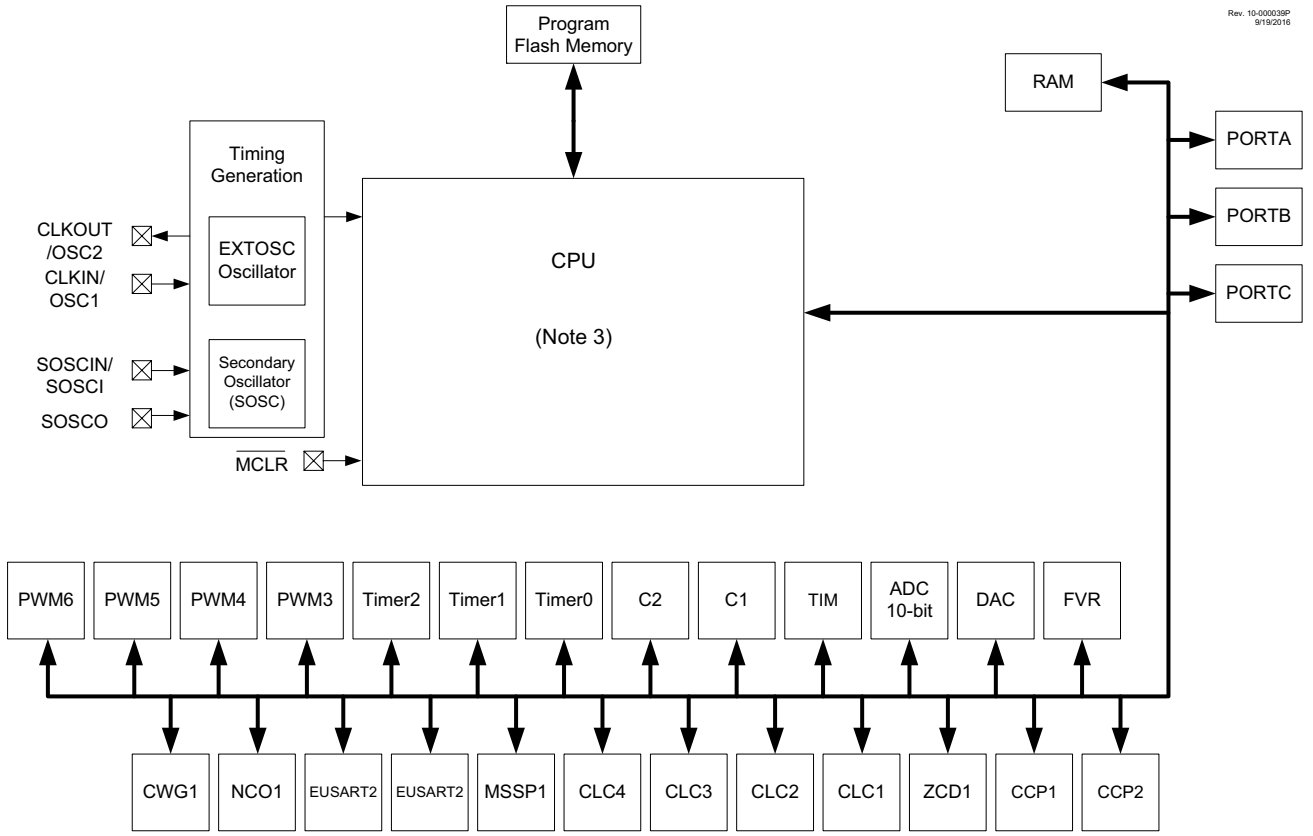



**Note 1:** See applicable chapters for more information on peripherals.

**2:** See Table 1-1 for peripherals available on specific devices.

**3:** See Figure 3-1.

**FIGURE 1-2: PIC16(L)F15345 BLOCK DIAGRAM**




**Note 1:** See applicable chapters for more information on peripherals.

**2:** See Table 1-1 for peripherals available on specific devices.

**3:** See Figure 3-1.

**TABLE 1-2: PIC16(L)F15325 PINOUT DESCRIPTION**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RA0/ANA0/C1IN0+/DAC1OUT/ ICSPDAT/IOCA0 | RA0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA0 | AN | — | ADC Channel A0 input. |
| | C1IN0+ | AN | — | Comparator 1 positive input. |
| | DAC1OUT | — | AN | Digital-to-Analog Converter output. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming™ and debugging data input/ output. |
| | IOCA0 | TTL/ST | — | Interrupt-on-change input. |
| RA1/ANA1/VREF+/C1IN0-/C2IN0-/ DAC1REF+/T0CKI(1)/ICSPCLK/IOCA1 | RA1 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA1 | AN | — | ADC Channel A1 input. |
| | VREF+ | AN | — | External ADC and/or DAC positive reference input. |
| | C1IN0- | AN | — | Comparator 1 negative input. |
| | C2IN0- | AN | — | Comparator 2 negative input. |
| | DAC1REF+ | TTL/ST | AN | DAC positive reference. |
| | T0CKI(1) | TTL/ST | — | Timer0 clock input. |
| | ICSPCLK | ST | — | In-Circuit Serial Programming™ and debugging clock input. |
| | IOCA1 | TTL/ST | — | Interrupt-on-change input. |
| RA2/ANA2/CWG1IN(1)/ZCD1/INT(1)/ IOCA2 | RA2 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA2 | AN | — | ADC Channel A2 input. |
| | CWG1IN(1) | TTL/ST | — | Complementary Waveform Generator 1 input. |
| | ZCD1 | AN | AN | Zero-cross detect input pin (with constant current sink/ source). |
| | INT(1) | TTL/ST | — | External interrupt request input. |
| | IOCA2 | TTL/ST | — | Interrupt-on-change input. |
| RA3/$\overline{\text{MCLR}}$/VPP/IOCA3 | RA3 | TTL/ST | CMOS/OD | General purpose I/O. |
| | $\overline{\text{MCLR}}$ | ST | — | Master clear input with internal weak pull up resistor. |
| | VPP | HV | — | ICSP™ High-Voltage Programming mode entry input. |
| | IOCA3 | TTL/ST | — | Interrupt-on-change input. |
| RA4/ANA4/C1IN1-/T1G(1)/SOSCO/ CLKOUT/OSC2/IOCA4 | RA4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA4 | AN | — | ADC Channel A4 input. |
| | C1IN1- | AN | — | Comparator 1 negative input. |
| | T1G(1) | ST | — | Timer1 Gate input. |
| | SOSCO | — | AN | 32.768 kHz secondary oscillator crystal driver output. |
| | CLKOUT | — | CMOS/OD | FOSC/4 digital output (in non-crystal/resonator modes). |
| | OSC2 | — | XTAL | External Crystal/Resonator (LP, XT, HS modes) driver output. |
| | IOCA4 | TTL/ST | — | Interrupt-on-change input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 1-2: PIC16(L)F15325 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RA5/ANA5/T1CKI(1)/T2IN/SOSCIN/ CLCIN3(1)/CLKIN/OSC1/EIN/IOCA5 | RA5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA5 | AN | — | ADC Channel A5 input. |
| | T1CKI(1) | TTL/ST | — | Timer1 external digital clock input. |
| | T2IN | TTL/ST | — | Timer2 external input. |
| | SOSCIN | AN | — | 32.768 kHz secondary oscillator crystal driver input. |
| | CLCIN3(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | CLKIN | TTL/ST | — | External digital clock input. |
| | OSC1 | XTAL | — | External Crystal/Resonator (LP, XT, HS modes) driver input. |
| | EIN | TTL/ST | — | External digital clock input. |
| | IOCA5 | TTL/ST | — | Interrupt-on-change input. |
| RC0/ANC0/C2IN0+/SCL1(1,4)/SCK1(1)/ IOCC0 | RC0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC0 | AN | — | ADC Channel C0 input. |
| | C2IN0+ | AN | — | Comparator 2 positive input. |
| | SCL1(1,4) | $I^2C$ | OD | $I^2C$, OD, MSSP1 $I^2C$ input/output. |
| | SCK1(1) | TTL/ST | CMOS/OD | MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output). |
| | IOCC0 | TTL/ST | — | Interrupt-on-change input. |
| RC1/ANC1/C1IN1-/C2IN1-/SDA1(1,4)/ SDI1(1)/CLCIN2(1)/IOCC1 | RC1 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC1 | AN | — | ADC Channel C1 input. |
| | C1IN1- | AN | — | Comparator 1 negative input. |
| | C2IN1- | AN | — | Comparator 2 negative input. |
| | SDA1(1,4) | $I^2C$ | OD | MSSP1 $I^2C$ serial data input/output. |
| | SDI1(1) | TTL/ST | — | MSSP1 SPI serial data input. |
| | CLCIN2(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCC1 | TTL/ST | — | Interrupt-on-change input. |
| RC2/ANC2/C1IN2-/C2IN2-/IOCC2 | RC2 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC2 | AN | — | ADC Channel C2 input. |
| | C1IN2- | AN | — | Comparator 1 negative input. |
| | C2IN2- | AN | — | Comparator 2 negative input. |
| | IOCC2 | TTL/ST | — | Interrupt-on-change input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 1-2: PIC16(L)F15325 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RC3/ANC3/C1IN3-/C2IN3-/CCP2(1)/SS1(1)/CLCIN0(1)/IOCC3 | RC3 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC3 | AN | — | ADC Channel C3 input. |
| | C1IN3- | AN | — | Comparator 1 positive input. |
| | C2IN3- | AN | — | Comparator 2 positive input. |
| | CCP2(1) | TTL/ST | CMOS/OD | Capture/compare/PWM2 (default input location for capture function). |
| | SS1(1) | TTL/ST | — | MSSP1 SPI slave select input. |
| | CLCIN0(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCC3 | TTL/ST | — | Interrupt-on-change input. |
| RC4/ANC4/TX1(1)/CK1(1)/CLCIN1(1)/IOCC4 | RC4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC4 | AN | — | ADC Channel C4 input. |
| | TX1 | — | CMOS | EUSART1 asynchronous transmit. |
| | CLCIN1(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | CK1(1) | TTL/ST | CMOS/OD | EUSART1 synchronous mode clock input/output. |
| | IOCC4 | TTL/ST | — | Interrupt-on-change input. |
| RC5/ANC5/CCP1(1)/RX1(1)/DT1(1)/IOCC5 | RC5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC5 | AN | — | ADC Channel C5 input. |
| | CCP1(1) | TTL/ST | CMOS/OD | Capture/compare/PWM1 (default input location for capture function). |
| | RX1(1) | TTL/ST | — | EUSART1 Asynchronous mode receiver data input. |
| | DT1(1) | TTL/ST | CMOS/OD | EUSART1 Synchronous mode data input/output. |
| | IOCC5 | TTL/ST | — | Interrupt-on-change input. |
| VDD | VDD | Power | — | Positive supply voltage input. |
| VSS | VSS | Power | — | Ground reference. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 1-2: PIC16(L)F15325 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| OUT(2) | C1OUT | — | CMOS/OD | Comparator 1 output. |
| | C2OUT | — | CMOS/OD | Comparator 2 output. |
| | SDO1 | — | CMOS/OD | MSSP1 SPI serial data output. |
| | SCK1 | — | CMOS/OD | MSSP1 SPI serial clock output. |
| | DT1(3) | — | CMOS/OD | EUSART Synchronous mode data output. |
| | TX1 | — | CMOS/OD | EUSART1 Asynchronous mode transmitter data output. |
| | CK1 | — | CMOS/OD | EUSART1 Synchronous mode clock output. |
| | DT2(3) | — | CMOS/OD | EUSART Synchronous mode data output. |
| | TX2 | — | CMOS/OD | EUSART2 Asynchronous mode transmitter data output. |
| | CK2 | — | CMOS/OD | EUSART2 Synchronous mode clock output. |
| | SCL1(3,4) | — | CMOS/OD | MSSP1 $I^2C$ output. |
| | SDA1(3,4) | — | CMOS/OD | MSSP1 $I^2C$ output. |
| | DT1(3) | — | CMOS/OD | EUSART Synchronous mode data output. |
| | TMR0 | — | CMOS/OD | Timer0 output. |
| | CCP1 | — | CMOS/OD | CCP1 output (compare/PWM functions). |
| | CCP2 | — | CMOS/OD | CCP2 output (compare/PWM functions). |
| | PWM3OUT | — | CMOS/OD | PWM3 output. |
| | PWM4OUT | — | CMOS/OD | PWM4 output. |
| | PWM5OUT | — | CMOS/OD | PWM5 output. |
| | PWM6OUT | — | CMOS/OD | PWM6 output. |
| | CWG1A | — | CMOS/OD | Complementary Waveform Generator 1 output A. |
| | CWG1B | — | CMOS/OD | Complementary Waveform Generator 1 output B. |
| | CWG1C | — | CMOS/OD | Complementary Waveform Generator 1 output C. |
| | CWG1D | — | CMOS/OD | Complementary Waveform Generator 1 output D. |
| | CLC1OUT | — | CMOS/OD | Configurable Logic Cell 1 output. |
| | CLC2OUT | — | CMOS/OD | Configurable Logic Cell 2 output. |
| | CLC3OUT | — | CMOS/OD | Configurable Logic Cell 3 output. |
| | CLC4OUT | — | CMOS/OD | Configurable Logic Cell 4 output. |
| | NCO1OUT | — | CMOS/OD | Numerically Controller Oscillator output. |
| | CLKR | — | CMOS/OD | Clock Reference module output. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 1-3: PIC16(L)F15345 PINOUT DESCRIPTION**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RA0/ANA0/C1IN0+/DAC1OUT/ ICSPDAT/IOCA0 | RA0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA0 | AN | — | ADC Channel A0 input. |
| | C1IN0+ | AN | — | Comparator 1 positive input. |
| | DAC1OUT | — | AN | Digital-to-Analog Converter output. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming™ and debugging data input/ output. |
| | IOCA0 | TTL/ST | — | Interrupt-on-change input. |
| RA1/ANA1/VREF+/C1IN0-/C2IN0-/ DAC1REF+/T0CKI(1)/ICSPCLK/IOCA1 | RA1 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA1 | AN | — | ADC Channel A1 input. |
| | VREF+ | AN | — | External ADC and/or DAC positive reference input. |
| | C1IN0- | AN | — | Comparator 1 negative input. |
| | C2IN0- | AN | — | Comparator 2 negative input. |
| | DAC1REF+ | TTL/ST | AN | DAC positive reference. |
| | T0CKI(1) | TTL/ST | — | Timer0 clock input. |
| | ICSPCLK | ST | — | In-Circuit Serial Programming™ and debugging clock input. |
| | IOCA1 | TTL/ST | — | Interrupt-on-change input. |
| RA2/ANA2/CWG1IN(1)/ZCD1/ CLCIN0(1)/INT(1)/IOCA2 | RA2 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA2 | AN | — | ADC Channel A2 input. |
| | CWG1IN(1) | TTL/ST | — | Complementary Waveform Generator 1 input. |
| | ZCD1 | AN | AN | Zero-cross detect input pin (with constant current sink/ source). |
| | CLCIN0(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | INT(1) | TTL/ST | — | External interrupt request input. |
| | IOCA2 | TTL/ST | — | Interrupt-on-change input. |
| RA3/$\overline{\text{MCLR}}$/VPP/IOCA3 | RA3 | TTL/ST | CMOS/OD | General purpose I/O. |
| | $\overline{\text{MCLR}}$ | ST | — | Master clear input with internal weak pull up resistor. |
| | VPP | HV | — | ICSP™ High-Voltage Programming mode entry input. |
| | IOCA3 | TTL/ST | — | Interrupt-on-change input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$; HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**5:** For 14/16-pin package only.

**6:** For 20-pin package only

**TABLE 1-3: PIC16(L)F15345 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RA4/ANA4/C1IN1-/T1G(1)/SOSCO/ CLKOUT/OSC2/IOCA4 | RA4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA4 | AN | — | ADC Channel A4 input. |
| | C1IN1- | AN | — | Comparator 1 negative input. |
| | T1G(1) | ST | — | Timer1 Gate input. |
| | SOSCO | — | AN | 32.768 kHz secondary oscillator crystal driver output. |
| | CLKOUT | — | CMOS/OD | FOSC/4 digital output (in non-crystal/resonator modes). |
| | OSC2 | — | XTAL | External Crystal/Resonator (LP, XT, HS modes) driver output. |
| | IOCA4 | TTL/ST | — | Interrupt-on-change input. |
| RA5/ANA5/T1CKI(1)/T2IN/SOSCIN/ CLKIN/OSC1/EIN/IOCA5 | RA5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA5 | AN | — | ADC Channel A5 input. |
| | T1CKI(1) | TTL/ST | — | Timer1 external digital clock input. |
| | T2IN | TTL/ST | — | Timer2 external input. |
| | SOSCIN | AN | — | 32.768 kHz secondary oscillator crystal driver input. |
| | CLKIN | TTL/ST | — | External digital clock input. |
| | OSC1 | XTAL | — | External Crystal/Resonator (LP, XT, HS modes) driver input. |
| | EIN | TTL/ST | — | External digital clock input. |
| | IOCA5 | TTL/ST | — | Interrupt-on-change input. |
| RB4/ANB4/ADACT(1)/SCK1(1)/ SCL1(1,4)/CLCIN2(1)/IOCB4 | RB4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB4 | AN | — | ADC Channel B4 input. |
| | ADACT(1) | TTL/ST | — | ADC Auto-Conversion Trigger input. |
| | SCK1(1) | TTL/ST | CMOS/OD | MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output). |
| | SCL1(1,4) | I2C | OD | MSSP1 I2C input/output. |
| | CLCIN2(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCB4 | TTL/ST | — | Interrupt-on-change input. |
| RB5/ANB5/RX2(1)/DT2(1)/CLCIN3(1)/ IOCB5 | RB5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB5 | AN | — | ADC Channel B5 input. |
| | RX2(1) | TTL/ST | — | EUSART2 Asynchronous mode receiver data input. |
| | DT2(3) | TTL/ST | CMOS/OD | EUSART2 Synchronous mode data input/output. |
| | CLCIN3(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCB5 | TTL/ST | — | Interrupt-on-change input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I2C = Schmitt Trigger input with I2C
HV = High Voltage; XTAL = Crystal levels

**Note**
**1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.
**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
**4:** These pins are configured for I2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I2C specific or SMBus input buffer thresholds.
**5:** For 14/16-pin package only.
**6:** For 20-pin package only

**TABLE 1-3: PIC16(L)F15345 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RB6/ANB6/SDA1(1,4)/SDI1(1)/IOCB6 | RB6 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB6 | AN | — | ADC Channel B6 input. |
| | SDA1(1,4) | $I^2C$ | OD | MSSP1 $I^2C$ serial data input/output. |
| | SDI1(1) | TTL/ST | — | MSSP1 SPI serial data input. |
| | IOCB6 | TTL/ST | — | Interrupt-on-change input. |
| RB7/ANB7/TX2(1)/CK2(1)/IOCB7 | RB7 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB7 | AN | — | ADC Channel B7 input. |
| | TX2(1) | — | CMOS | EUSART2 asynchronous transmit. |
| | CK2(1) | TTL/ST | CMOS/OD | EUSART2 synchronous mode clock input/output. |
| | IOCB7 | TTL/ST | — | Interrupt-on-change input. |
| RC0/ANC0/C2IN0+/IOCC0 | RC0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC0 | AN | — | ADC Channel C0 input. |
| | C2IN0+ | AN | — | Comparator 2 positive input. |
| | IOCC0 | TTL/ST | — | Interrupt-on-change input. |
| RC1/ANC1/C1IN1-/C2IN1-/IOCC1 | RC1 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC1 | AN | — | ADC Channel C1 input. |
| | C1IN1- | AN | — | Comparator 1 negative input. |
| | C2IN1- | AN | — | Comparator 2 negative input. |
| | IOCC1 | TTL/ST | — | Interrupt-on-change input. |
| RC2/ANC2/C1IN2-/C2IN2-/IOCC2 | RC2 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC2 | AN | — | ADC Channel C2 input. |
| | C1IN2- | AN | — | Comparator 1 negative input. |
| | C2IN2- | AN | — | Comparator 2 negative input. |
| | IOCC2 | TTL/ST | — | Interrupt-on-change input. |
| RC3/ANC3/C1IN3-/C2IN3-/CCP2(1)/ CLCIN1(1)/IOCC3 | RC3 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC3 | AN | — | ADC Channel C3 input. |
| | C1IN3- | AN | — | Comparator 1 negative input. |
| | C2IN3- | AN | — | Comparator 2 negative input. |
| | CCP2(1) | TTL/ST | CMOS/OD | Capture/compare/PWM2 (default input location for capture function). |
| | CLCIN1(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCC3 | TTL/ST | — | Interrupt-on-change input. |
| RC4/ANC4/IOCC4 | RC4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC4 | AN | — | ADC Channel C4 input. |
| | IOCC4 | TTL/ST | — | Interrupt-on-change input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**5:** For 14/16-pin package only.

**6:** For 20-pin package only

**TABLE 1-3: PIC16(L)F15345 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RC5/ANC5/CCP1(1)/IOCC5 | RC5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC5 | AN | — | ADC Channel C5 input. |
| | CCP1(1) | TTL/ST | CMOS/OD | Capture/compare/PWM1 (default input location for capture function). |
| | IOCC5 | TTL/ST | — | Interrupt-on-change input. |
| RC6/ANC6/$\overline{SS1}$(1)/IOCC6 | RC6 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC6 | AN | — | ADC Channel C6 input. |
| | $\overline{SS1}$(1) | TTL/ST | — | MSSP1 SPI slave select input. |
| | IOCC6 | TTL/ST | — | Interrupt-on-change input. |
| RC7/ANC7/IOCC7 | RC7 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC7 | AN | — | ADC Channel C7 input. |
| | IOCC7 | TTL/ST | — | Interrupt-on-change input. |
| VDD | VDD | Power | — | Positive supply voltage input. |
| VSS | VSS | Power | — | Ground reference. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**5:** For 14/16-pin package only.

**6:** For 20-pin package only

**TABLE 1-3: PIC16(L)F15345 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| OUT(2) | C1OUT | — | CMOS/OD | Comparator 1 output. |
| | C2OUT | — | CMOS/OD | Comparator 2 output. |
| | SDO1 | — | CMOS/OD | MSSP1 SPI serial data output. |
| | SCK1 | — | CMOS/OD | MSSP1 SPI serial clock output. |
| | DT1(3) | — | CMOS/OD | EUSART Synchronous mode data output. |
| | TX1 | — | CMOS/OD | EUSART1 Asynchronous mode transmitter data output. |
| | CK1 | — | CMOS/OD | EUSART1 Synchronous mode clock output. |
| | DT2(3) | — | CMOS/OD | EUSART Synchronous mode data output. |
| | TX2 | — | CMOS/OD | EUSART2 Asynchronous mode transmitter data output. |
| | CK2 | — | CMOS/OD | EUSART2 Synchronous mode clock output. |
| | SCL1(3,4) | — | CMOS/OD | MSSP1 $I^2C$ output. |
| | SDA1(3,4) | — | CMOS/OD | MSSP1 $I^2C$ output. |
| | DT1(3) | — | CMOS/OD | EUSART Synchronous mode data output. |
| | TMR0 | — | CMOS/OD | Timer0 output. |
| | CCP1 | — | CMOS/OD | CCP1 output (compare/PWM functions). |
| | CCP2 | — | CMOS/OD | CCP2 output (compare/PWM functions). |
| | PWM3OUT | — | CMOS/OD | PWM3 output. |
| | PWM4OUT | — | CMOS/OD | PWM4 output. |
| | PWM5OUT | — | CMOS/OD | PWM5 output. |
| | PWM6OUT | — | CMOS/OD | PWM6 output. |
| | CWG1A | — | CMOS/OD | Complementary Waveform Generator 1 output A. |
| | CWG1B | — | CMOS/OD | Complementary Waveform Generator 1 output B. |
| | CWG1C | — | CMOS/OD | Complementary Waveform Generator 1 output C. |
| | CWG1D | — | CMOS/OD | Complementary Waveform Generator 1 output D. |
| | CLC1OUT | — | CMOS/OD | Configurable Logic Cell 1 output. |
| | CLC2OUT | — | CMOS/OD | Configurable Logic Cell 2 output. |
| | CLC3OUT | — | CMOS/OD | Configurable Logic Cell 3 output. |
| | CLC4OUT | — | CMOS/OD | Configurable Logic Cell 4 output. |
| | NCO1OUT | — | CMOS/OD | Numerically Controller Oscillator output. |
| | CLKR | — | CMOS/OD | Clock Reference module output. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**5:** For 14/16-pin package only.

**6:** For 20-pin package only