Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC16(L)F1704/8

14/20-Pin 8-Bit Advanced Analog Flash Microcontrollers

High-Performance RISC CPU

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 14 Kbytes Linear Program Memory Addressing
- Operating Speed:
  - DC – 32 MHz
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory
- High-Endurance Flash Data Memory (HEF)
  - 128 bytes of nonvolatile data storage
  - 100k erase/write cycles

Flexible Oscillator Structure

- 16 MHz Internal Oscillator Block:
  - Accurate to ±1%, typical
  - Software selectable frequency range from 16 MHz to 250 kHz
  - PLL multiplier to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 µA @ 32 kHz, 1.8V, typical
  - 32 µA/MHz @ 1.8V, typical

Special Microcontroller Features

- Operating Voltage Range:
  - 1.8V-3.6V (PIC16LF1704/8)
  - 2.3V-5.5V (PIC16F1704/8)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C
- Power-on Reset (POR)
- Low Power Brown-Out Reset (LPBOR)
- Extended Watch-Dog Timer (WDT):
  - Programmable period from 1 ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Power-Saving Sleep mode

Digital Peripheral Features

- Up to 17 I/O Pins and one Input-only Pin:
  - High current sink/source for LED drivers
  - Individually programmable weak pull-ups
  - Interrupt-on-change pin option with edge selectable option
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Timer2:
  - Up to three (TMR2/4/6)
  - 8-Bit Timer/Counter
  - 8-Bit Period Register
  - Prescaler and Postscaler
- Capture, Compare, PWM (CCP) Module
- Master Synchronous Serial Port (SSP) with SPI and I^2C with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on Start

Digital Peripheral Features (Continued)

- Complementary Output Generator (COG):
  - Push-Pull, Full Bridge, and Steering modes
  - Dedicated Rise/Fall Input Triggers
  - Dedicated Deadtime Delay Counters
  - Dedicated Phase Delay Counters
  - Dedicated Blanking Delay Counters
  - Concurrent Auto-Shutdown Selection
- Two Pulse Width Modulation (PWM) modules:
  - 10-bit Duty-Cycle Control
- Three Configurable Logic Cell (CLC) modules:
  - Generate a selected function of up to four inputs
  - Combinational and State Logic
  - External or Internal input/output pins
  - Operation in Sleep
- Peripheral Pin Select (PPS):
  - Digital outputs mapped to any GPIO pin
  - Digital inputs from any GPIO pin
  - CLC input multiplexing

Analog Peripheral Features

- Operational Amplifiers:
  - Up to two configurable op amps
  - Selectable internal and external channels
  - High/Low selectable Gain Bandwidth Product
- Two High-Speed Comparators:
  - 60 ns response time
  - Low-power/High-power mode
  - Comparator outputs externally accessible
  - Software hysteresis enable
- Analog-to-Digital Converter (ADC) module
  - 10-bit resolution, 12 channels
  - Auto conversion start capability
  - Conversion available during Sleep
- 8-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Positive and negative reference selection
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Zero-Cross Detection Circuit:
  - Constant Voltage Output
  - Current Source/Sink
  - Interrupt on Edge Detect
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels

PIC16(L)F170x Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash (bytes)	I/O's(2)	10-bit ADC (ch)	8-bit DAC	High-Speed/ Comparators	Op Amp	Zero Cross	Timers (8/16-bit)	CCP	PWM	COG	EUSART	MSSP (I^2C/SPI)	CLC	PPS	Debug(1)	XLP
PIC16(L)F1703	(3)	2048	256	128	12	8	0	0	2	1	2/1	2	0	0	0	1	0	Y	I/E	Y
PIC16(L)F1704	(1)	4096	512	128	12	8	1	2	2	1	4/1	2	2	1	1	1	3	Y	I/E	Y
PIC16(L)F1705	(2)	8192	1024	128	12	8	1	2	2	1	4/1	2	2	1	1	1	3	Y	I/E	Y
PIC16(L)F1707	(3)	2048	256	128	18	12	0	0	2	1	2/1	2	0	0	0	1	0	Y	I/E	Y
PIC16(L)F1708	(1)	4096	512	128	18	12	1	2	2	1	4/1	2	2	1	1	1	3	Y	I/E	Y
PIC16(L)F1709	(2)	8192	1024	128	18	12	1	2	2	1	4/1	2	2	1	1	1	3	Y	I/E	Y

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – using Debug Header; E – using Emulation Header.
2: One pin is input-only.

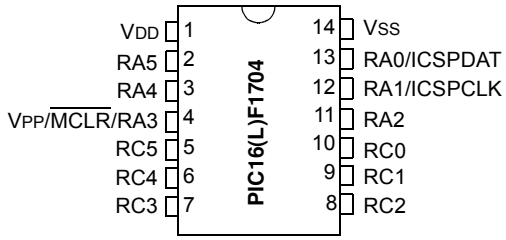
Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001715 PIC16(L)F1704/8 Data Sheet, 14/20-Pin Flash, 8-bit Microcontrollers.
2: DS40001729 PIC16(L)F1705/9 Data Sheet, 14/20-Pin Flash, 8-bit Microcontrollers.
3: DS40001722 PIC16(L)F1703/7 Data Sheet, 14/20-Pin Flash, 8-bit Microcontrollers

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

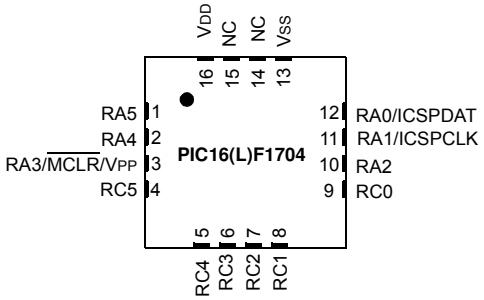
PIN DIAGRAMS

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP DIAGRAM FOR PIC16(L)F1704



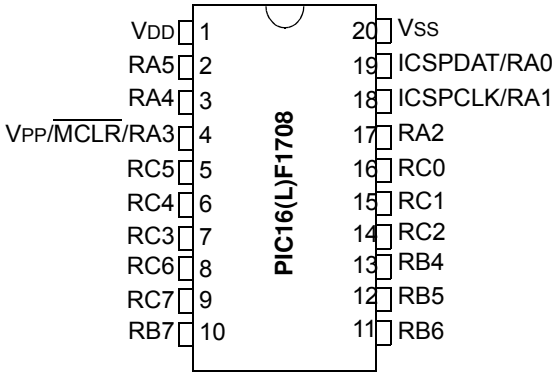
Note: See Table 1 for the pin allocation table.

FIGURE 2: 16-PIN QFN



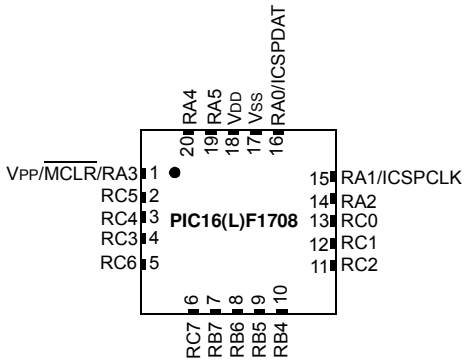
Note: See Table 1 for the pin allocation table.

FIGURE 3: 20-PIN PDIP, SOIC,SSOP



Note: See Table 2 for the pin allocation table.

FIGURE 4: 20-PIN QFN



Note: See Table 2 for the pin allocation table.

Pin Allocation Tables

TABLE 1: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1704)

I/O(2)	PDIP/SOIC/SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	13	12	AN0	VREF-	C1IN+	—	DAC1OUT1	—	—	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	—	DAC1OUT2	ZCD	T0CKI(1)	—	—	COGIN(1)	—	—	—	INT(1) IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	AN3	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	1	—	—	—	—	—	—	T1CKI(1) SOSCI	—	—	—	—	—	CLCIN3(1)	IOC	Y	CLKIN OSC1
RC0	10	9	AN4	—	C2IN+	OPA1IN+	—	—	—	—	—	—	SCK(1) SCL(3)	—	—	IOC	Y	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	OPA1IN-	—	—	—	—	—	—	SDI(1) SDA(3)	—	CLCIN2(1)	IOC	Y	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	OPA1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	OPA2OUT	—	—	—	CCP2(1)	—	—	$\overline{\text{SS}}$(1)	—	CLCIN0(1)	IOC	Y	—
RC4	6	5	—	—	—	OPA2IN-	—	—	—	—	—	—	—	CK(1)	CLCIN1(1)	IOC	Y	—
RC5	5	4	—	—	—	OPA2IN+	—	—	—	CCP1(1)	—	—	—	RX(1,3)	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	—	—	—	—	CPP1	PWM3OUT	COGA	SDA(3)	CK	CLC1OUT	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CPP2	PWM4OUT	COGB	SCL(3)	DT(3)	CLC2OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGC	SDO	TX	CLC3OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGD	SCK	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F1708)

I/O(2)	PDIP/SOIC/SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	19	16	AN0	VREF-	C1IN+	—	DAC1OUT1	—	—	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	15	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	14	AN2	—	—	—	DAC1OUT2	ZCD	T0CKI(1)	—	—	COGIN(1)	—	—	—	INT(1) IOC	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	20	AN3	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	19	—	—	—	—	—	—	T1CKI SOSCI	—	—	—	—	—	CLCIN3(1)	IOC	Y	CLKIN OSC1
RB4	13	10	AN10	—	—	OPA1IN-	—	—	—	—	—	—	SDI(1) SDA(3)	—	—	IOC	Y	—
RB5	12	9	AN11	—	—	OPA1IN+	—	—	—	—	—	—	—	RX(1,3)		IOC	Y	—
RB6	11	8	—	—	—	—	—	—	—	—	—	—	SCK(1) SCL(3)	—	—	IOC	Y	—
RB7	10	7	—	—	—	—	—	—	—	—	—	—	—	CK(1)	—	IOC	Y	—
RC0	16	13	AN4	—	C2IN+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLCIN2(1)	IOC	Y	—
RC2	14	11	AN6	—	C1IN2- C2IN2-	OPA1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	C1IN3- C2IN3-	OPA2OUT	—	—	—	CCP2(1)	—	—	—	—	CLCIN0(1)	IOC	Y	—
RC4	6	3	—	—	—	—	—	—	—	—	—	—	—	—	CLCIN1(1)	IOC	Y	—
RC5	5	2	—	—	—	—	—	—	—	CCP1(1)	—	—	—	—	—	IOC	Y	—
RC6	8	5	AN8	—	—	OPA2IN-	—	—	—	—	—	—	$\overline{\text{SS}}$(1)	—	—	IOC	Y	—
RC7	9	6	AN9	—	—	OPA2IN+	—	—	—	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	—	—	—	—	CPP1	PWM3OUT	COGA	SDA(3)	CK	CLC1OUT	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CPP2	PWM4OUT	COGB	SCL(3)	DT(3)	CLC2OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGC	SDO	TX	CLC3OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGD	SCK	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-2.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

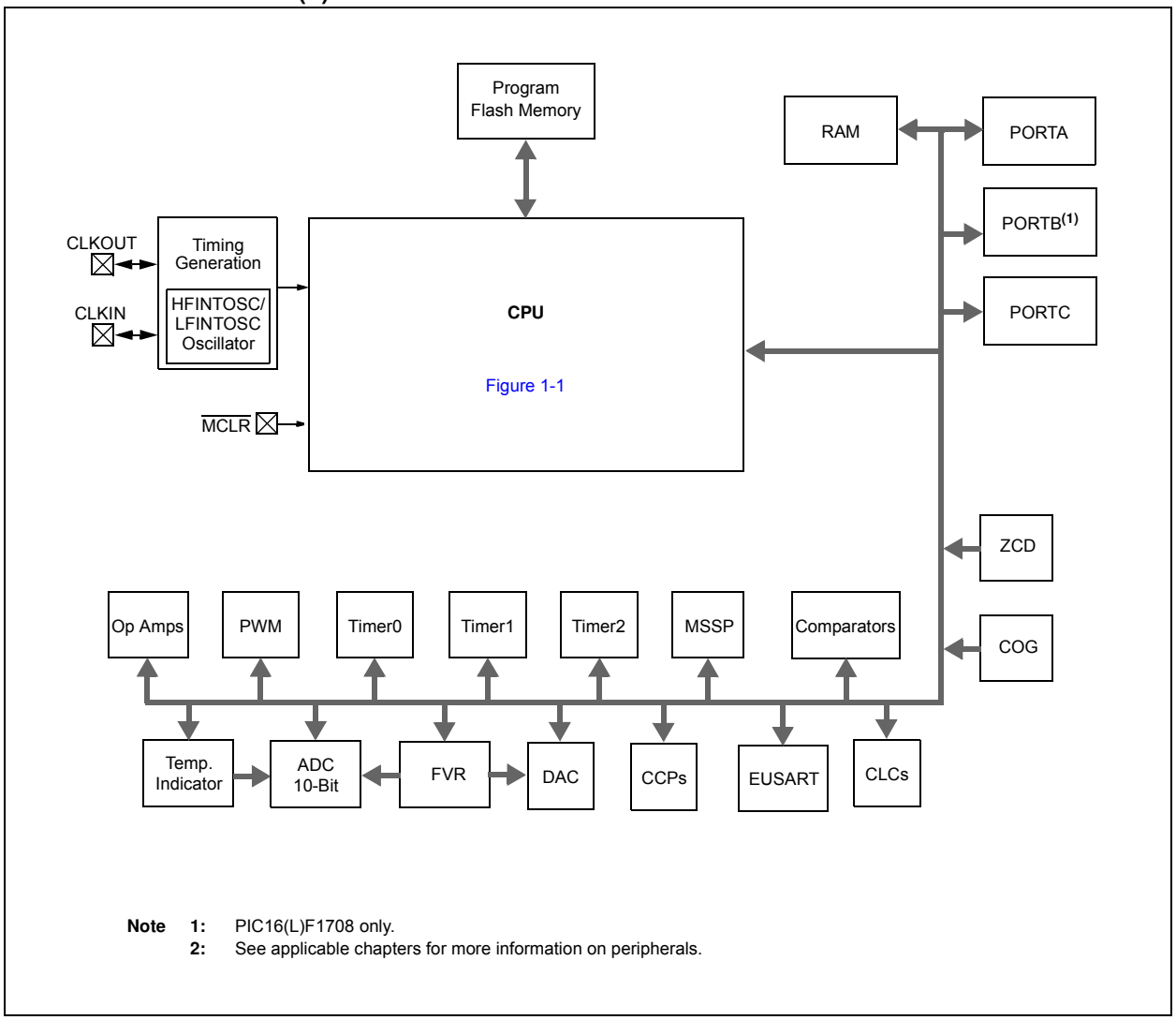
The PIC16(L)F1704/8 are described within this data sheet. They are available in 14-pin and 20-pin DIP packages and 16-pin and 20-pin QFN packages. Figure 1-1 shows a block diagram of the PIC16(L)F1704/8 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1704	PIC16(L)F1708
Analog-to-Digital Converter (ADC)		●	●
Digital-to-Analog Converter (DAC)		●	●
Complementary Output Generator (COG)		●	●
Fixed Voltage Reference (FVR)		●	●
Zero Cross Detection (ZCD)		●	●
Temperature Indicator		●	●
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	●	●
	CCP2	●	●
Comparators			
	C1	●	●
	C2	●	●
Configurable Logic Cell (CLC)			
	CLC1	●	●
	CLC2	●	●
	CLC3	●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)			
	EUSART	●	●
Master Synchronous Serial Ports			
	MSSP	●	●
Op Amp			
	Op Amp 1	●	●
	Op Amp 2	●	●
Pulse Width Modulator (PWM)			
	PWM3	●	●
	PWM4	●	●
Timers			
	Timer0	●	●
	Timer1	●	●
	Timer2	●	●

FIGURE 1-1: PIC16(L)F1704/8 BLOCK DIAGRAM



Note 1: PIC16(L)F1708 only.
2: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1704 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/VREF-/C1IN+/ DAC1OUT/ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	VREF-	AN	—	ADC Negative Voltage Reference input.
	C1IN+	AN	—	Comparator C1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/AN1/VREF+/C1IN0-/C2IN0-/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	VREF+	AN	—	ADC Voltage Reference input.
	C1IN0-	AN	—	Comparator C2 negative input.
	C2IN0-	AN	—	Comparator C3 negative input.
	ICSPCLK	ST	—	Serial Programming Clock.
RA2/AN2/DAC1OUT2/ZCD/ T0CKI(1)/COGIN(1)/INT(1)	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ZCD	—	AN	Zero Cross Detection Current Source/Sink.
	T0CKI	TTL/ST	—	Timer0 clock input.
	COGIN	TTL/ST	—	Complementary Output Generator input.
	INT	TTL/ST	—	External interrupt.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL/ST	CMOS	General purpose input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
RA4/AN3/T1G(1)/SOSCO/ OSC2/CLKOUT	RA4	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	T1G	TTL/ST	—	Timer1 gate input.
	SOSCO	XTAL	XTAL	Secondary Oscillator Connection.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA5/T1CKI(1)/SOSCI/ CLCIN3(1)/OSC1/CLKIN	RA5	TTL/ST	CMOS	General purpose I/O.
	T1CKI	TTL/ST	—	Timer1 clock input.
	SOSCI	XTAL	XTAL	Secondary Oscillator Connection.
	CLCIN3	TTL/ST	—	Configurable Logic Cell source input.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	TTL/ST	—	External clock input (EC mode).
RC0/AN4/C2IN+/OPA1IN+/ SCK(1)/SCL(3)	RC0	TTL/ST	—	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	C2IN+	AN	—	Comparator positive input.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	SCK	TTL/ST	—	SPI clock.
	SCL	I^2C	—	I^2C clock.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1704 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/AN5/C1IN1-/C2IN1-/ OPA1IN-/SDI(1)/SDA(3)/ CLCIN2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	SDI	CMOS	—	SPI data input.
	SDA	I^2C	—	I^2C data input.
	CLCIN2	TTL/ST	—	Configurable Logic Cell source input.
RC2/AN6/C1IN2-/C2IN2-/ OPA1OUT	RC2	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
RC3/AN7/C1IN3-/C2IN3-/ OPA2OUT/CCP2(1)/$\overline{SS}$(1)/ CLCIN0(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
	CCP2	TTL/ST	CMOS	Capture/Compare/PWM2.
	$\overline{SS}$	TTL/ST	—	Slave Select input.
	CLCIN0	TTLST	—	Configurable Logic Cell source input.
RC4/OPA2IN-/CK(1)/CLCIN1(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CK	TTL/ST	CMOS	USART synchronous clock.
	CLCIN1	TTL/ST	—	Configurable Logic Cell source input.
RC5/OPA2IN+/CCP1(1)/RX(1)	RC5	TTL/ST	CMOS	General purpose I/O.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP1	TTL/ST	CMOS	Capture/Compare/PWM1.
	RX	TTL/ST	—	USART asynchronous input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1704 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT	—	CMOS	Comparator output.
	C2OUT	—	CMOS	Comparator output.
	CCP1	—	CMOS	Capture/Compare/PWM1 output.
	CCP2	—	CMOS	Capture/Compare/PWM2 output.
	PWM3OUT	—	CMOS	PWM3 output.
	PWM4OUT	—	CMOS	PWM4 output.
	COGA	—	CMOS	Complementary Output Generator Output A.
	COGB	—	CMOS	Complementary Output Generator Output B.
	COGC	—	CMOS	Complementary Output Generator Output C.
	COGD	—	CMOS	Complementary Output Generator Output D.
	SDA(3)	—	OD	I^2C data input/output.
	SDO	—	CMOS	SPI data output.
	SCK	—	CMOS	SPI clock output.
	SCL(3)	—	OD	I^2C clock output.
	TX/CK	—	CMOS	USART asynchronous TX data/synchronous clock output.
	DT	—	CMOS	USART synchronous data output.
	CLC1OUT	—	CMOS	Configurable Logic Cell 1 source output.
	CLC2OUT	—	CMOS	Configurable Logic Cell 2 source output.
	CLC3OUT	—	CMOS	Configurable Logic Cell 3 source output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1708 PIN OUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/VREF-/C1IN+/ DAC1OUT/ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	VREF-	AN	—	ADC Negative Voltage Reference input.
	C1IN+	AN	—	Comparator C1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/AN1/VREF+/C1IN0-/C2IN0-/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	VREF+	AN	—	ADC Voltage Reference input.
	C1IN0-	AN	—	Comparator C2 negative input.
	C2IN0-	AN	—	Comparator C3 negative input.
	ICSPCLK	ST	—	Serial Programming Clock.
RA2/AN2/DAC1OUT2/ZCD/ T0CKI(1)/COGIN(1)/INT(1)	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	ZCD	—	AN	Zero-Cross Detection Current Source/Sink.
	T0CKI	ST	—	Timer0 clock input.
	COGIN	ST	CMOS	Complementary Output Generator input.
	INT	ST	—	External interrupt.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL/ST	CMOS	General purpose I/O.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
RA4/AN3/T1G(1)/SOSCO/ OSC2/CLKOUT	RA4	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	T1G	ST	—	Timer1 gate input.
	SOSCO	XTAL	XTAL	Secondary Oscillator Connection.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA5/T1CKI/SOSCI/ CLCIN3(1)/OSC1/CLKIN	RA5	TTL/ST	CMOS	General purpose I/O.
	T1CKI	ST	—	Timer1 clock input.
	SOSCI	XTAL	XTAL	Secondary Oscillator Connection.
	CLCIN3	ST	—	Configurable Logic Cell source input.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External clock input (EC mode).
RB4/AN10/OPA1IN-/SCK(1)/ SDA(3)	RB4	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	SCK	ST	CMOS	SPI clock.
	SDA	I2C	OD	I2C data input/output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I2C = Schmitt Trigger input with I2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-2.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These I2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1708 PIN OUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB5/AN11/OPA1IN+/RX(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	RX	ST	—	USART asynchronous input.
RB6/SDI(1)/SCL(3)	RB6	TTL/ST	CMOS	General purpose I/O.
	SDI	CMOS	—	SPI data input.
	SCL	I^2C	OD	I^2C clock.
RB7/CK(1)	RB7	TTL/ST	CMOS	General purpose I/O.
	CK	ST	CMOS	USART synchronous clock.
RC0/AN4/C2IN+	RC0	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	C2IN+	AN	—	Comparator positive input.
RC1/AN5/C1IN1-/C2IN1-/ CLCIN2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	CLCIN2	ST	—	Configurable Logic Cell source input.
RC2/AN6/C1IN2-/C2IN2-/ OPA1OUT	RC2	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
RC3/AN7/C1IN3-/C2IN3-/ OPA2OUT/CCP2(1)/CLCIN0(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	CLCIN0	ST	—	Configurable Logic Cell source input.
RC4/CLCIN1(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	CLCIN1	ST	—	Configurable Logic Cell source input.
RC5/CCP1(1)	RC5	TTL/ST	CMOS	General purpose I/O.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC6/AN8/OPA2IN-/$\overline{SS}$(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	$\overline{SS}$	ST	—	Slave Select input.
RC7/AN9/OPA2IN+	RC7	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
VDD	VDD	Power	—	Positive supply.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-2.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1708 PIN OUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT	—	CMOS	Comparator output.
	C2OUT	—	CMOS	Comparator output.
	CCP1	—	CMOS	Capture/Compare/PWM1 output.
	CCP2	—	CMOS	Capture/Compare/PWM2 output.
	PWM3OUT	—	CMOS	PWM3 output.
	PWM4OUT	—	CMOS	PWM4 output.
	COGA	—	CMOS	Complementary Output Generator Output A.
	COGB	—	CMOS	Complementary Output Generator Output B.
	COGC	—	CMOS	Complementary Output Generator Output C.
	COGD	—	CMOS	Complementary Output Generator Output D.
	SDA(3)	—	OD	I^2C data input/output.
	SDO	—	CMOS	SPI data output.
	SCK	—	CMOS	SPI clock output.
	SCL(3)	I^2C	OD	I^2C clock output.
	TX/CK	—	CMOS	USART asynchronous TX data/synchronous clock output.
	DT	—	CMOS	USART synchronous data output.
	CLC1OUT	—	CMOS	Configurable Logic Cell 1 source output.
	CLC2OUT	—	CMOS	Configurable Logic Cell 2 source output.
	CLC3OUT	—	CMOS	Configurable Logic Cell 3 source output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 12-2.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-3.

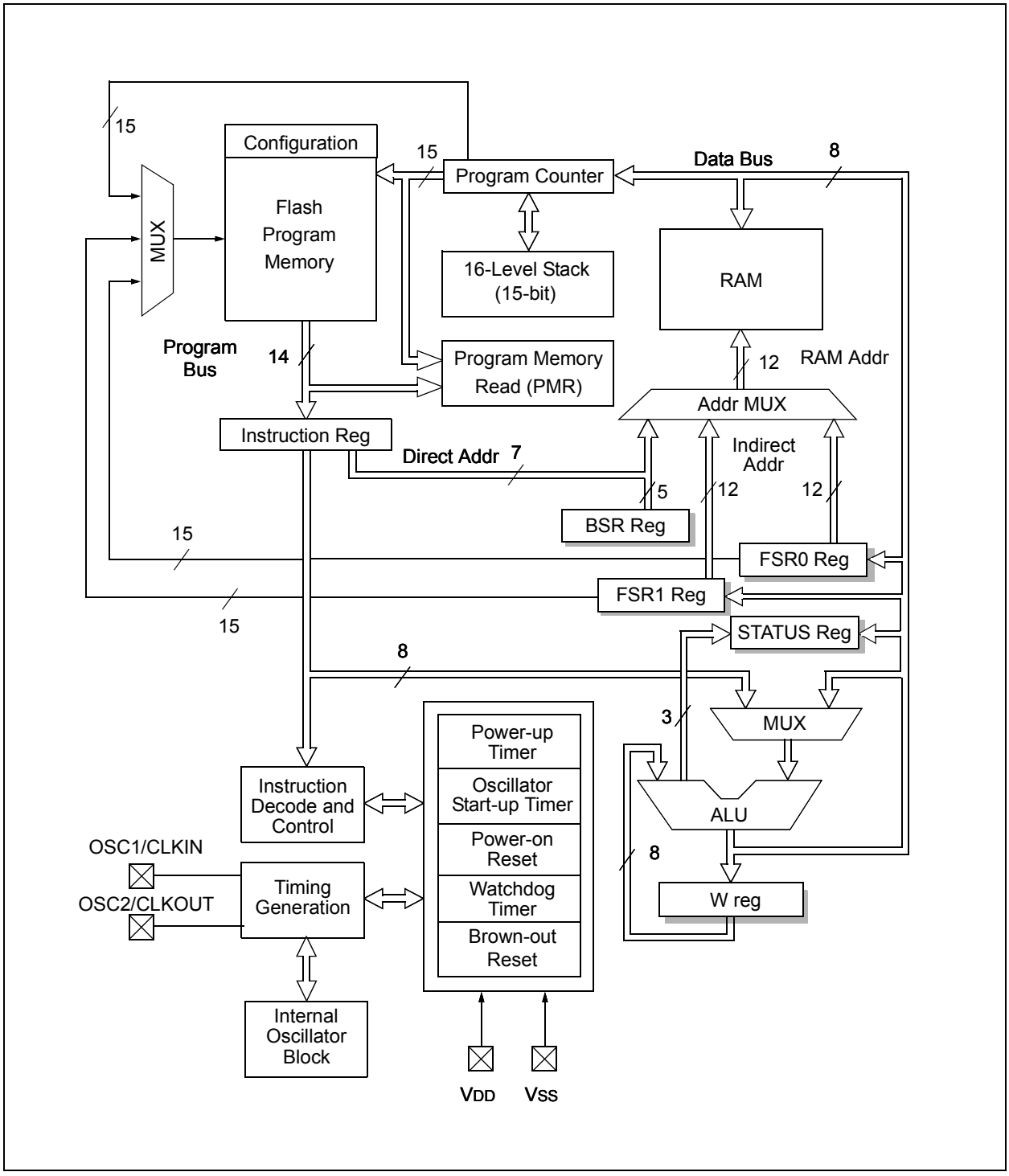
3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"** for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 3.6 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.7 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 31.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

Note 1: The method to access Flash memory through the PMCON registers is described in **Section 10.0 "Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

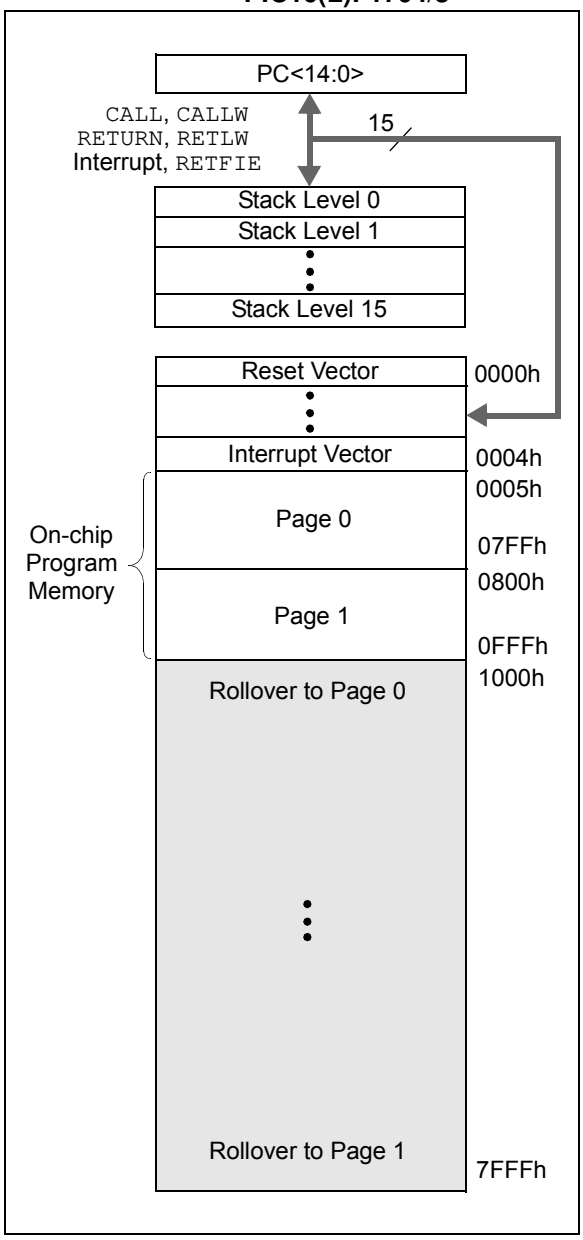
The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1704/8 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range(1)
PIC16(L)F1704/8	4,096	0FFFh	0F80h - 0FFFh

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1704/8



3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
  DW DATA0              ;First constant
  DW DATA1              ;Second constant
  DW DATA2
  DW DATA3
my_function
  ;… LOTS OF CODE…
  MOVLW   DATA_INDEX
  ADDLW   LOW constants
  MOVWF   FSR1L
  MOVLW   HIGH constants;MSb sets
                         automatically
  MOVWF   FSR1H
  BTFSC   STATUS, C     ;carry from ADDLW?
  INCF    FSR1H, f      ;yes
  MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 High-Endurance Flash

This device has a 128-byte section of high-endurance Program Flash Memory (PFM) in lieu of data EEPROM. This area is especially well suited for non-volatile data storage that is expected to be updated frequently over the life of the end product. See **Section 10.2 "Flash Program Memory Overview"** for more information on writing data to PFM. See **Section 3.1.1.2 "Indirect Read with FSR"** for more information about using the FSR registers to read byte data stored in PFM.

3.3 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-2):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.7 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper five bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

3.3.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-9.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 31.0 "Instruction Set Summary"**).

Note:	The C and DC bits operate as $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bits, respectively, in subtraction.

3.4 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT Time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Digit Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit(1) (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

3.4.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.4.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The General Purpose RAM occupies the 80 bytes after the SFR registers of selected data memory banks.

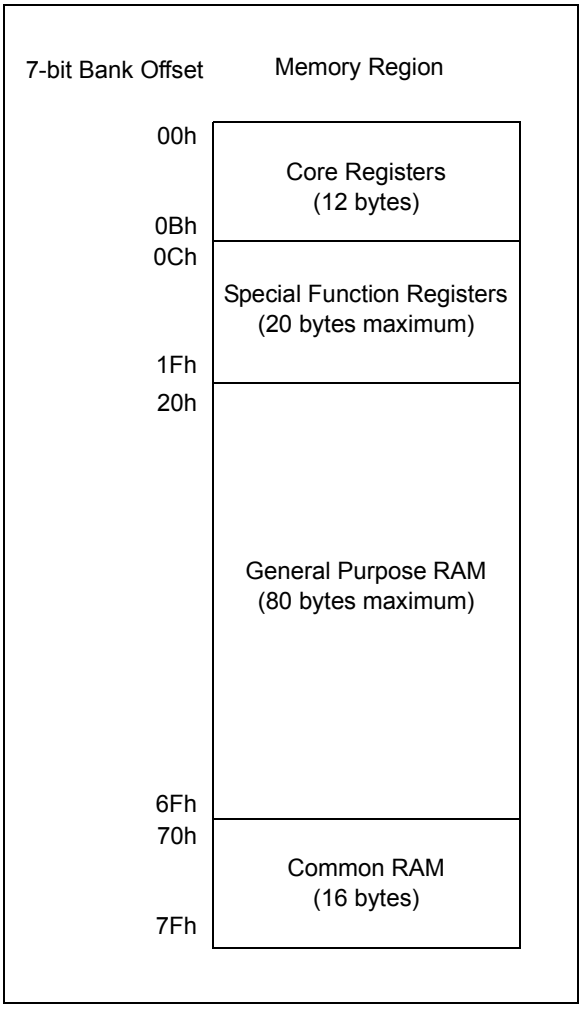
3.4.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.7.2 "Linear Data Memory"** for more information.

3.4.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-2: BANKED MEMORY PARTITIONING



3.4.4 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Tables 3-3 through 3-8.

TABLE 3-3: PIC16(L)F1704 MEMORY MAP (BANKS 0-7)

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	—	08Dh	—	10Dh	—	18Dh	—	20Dh	—	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	PMADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	PMADRH	212h	SSP1ADD	292h	CCPR1H	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	—	094h	—	114h	CM2CON1	194h	PMDATH	214h	SSP1STAT	294h	—	314h	—	394h	—
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	SSP1CON	295h	—	315h	—	395h	—
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSP1CON2	296h	—	316h	—	396h	—
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON(1)	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	—	218h	—	298h	CCPR2L	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RC1REG	219h	—	299h	CCPR2H	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TX1REG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	SP1BRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	ZCD1CON	19Ch	SP1BRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	—	19Dh	RC1STA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	TX1STA	21Eh	—	29Eh	CCPTMRS	31Eh	—	39Eh	—
01Fh	—	09Fh	ADCON2	11Fh	—	19Fh	BAUD1CON	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 16 Bytes	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		32Fh			
070h	Common RAM 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	330h	Unimplemented Read as '0'		
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		36Fh		3EFh	
												370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
												37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16LF1704.