Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC16(L)F1717/8/9

Cost-Effective 8-Bit Intelligent Analog Flash Microcontrollers

Description:

PIC16(L)F1717/8/9 microcontrollers combine Intelligent Analog integration with low cost and extreme low power (XLP) to suit a variety of general purpose applications. These 28-pin and 40-pin devices deliver on-chip op amps, Core Independent Peripherals (CLC, NCO and COG), Peripheral Pin Select and Zero-Cross Detect, providing for increased design flexibility.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - 0-32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- One 16-Bit Timer
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

Memory:

- Up to 16 Kwords Flash Program Memory
- Up to 2048 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- High-Endurance Flash (HEF):
  - 128B of nonvolatile data storage
  - 100K Erase/Write cycles

Operating Characteristics:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1717/8/9)
  - 2.3V to 5.5V (PIC16F1717/8/9)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals:

- Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Complementary Output Generator (COG):
  - Rising/falling edge dead-band control/ blanking
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0 Hz < FNCO < 32 MHz
  - Resolution: FNCO/220
- Capture/Compare/PWM (CCP) module
- PWM: Two 10-Bit Pulse-Width Modulators
- Serial Communications:
  - SPI, I^2C, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-Change with edge-select
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Intelligent Analog Peripherals:

- Operational Amplifiers:
  - Two configurable rail-to-rail op amps
  - Selectable internal and external channels
  - 2 MHz gain bandwidth product
- High-Speed Comparators:
  - Up to two comparators
  - 50 ns response time
  - Rail-to-rail inputs
- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 28 external channels
  - Conversion available during Sleep
  - Temperature indicator
- Zero-Cross Detector (ZCD):
  - Detect when AC signal on pin crosses ground
- 8-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Internal Voltage Reference module

Clocking Structure:

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Two external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
  - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC16(L)F171X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High Endurance Flash (bytes)	I/Os(2)	10-bit ADC (ch)	5/8-bit DAC	High-Speed/ Comparators	Op Amp	Zero Cross	Timers (8/16-bit)	CCP	PWM	COG	EUSART	MSSP (I^2C/SPI)	CLC	NCO	PPS	Debug(1)	XLP
PIC16(L)F1713	(1)	4096	512	128	25	17	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1716	(1)	8192	1024	128	25	17	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1717	(2)	8192	1024	128	36	28	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1718	(2)	16384	2048	128	25	17	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y
PIC16(L)F1719	(2)	16384	2048	128	36	28	1/1	2	2	1	4/1	2	2	1	1	1	4	1	Y	I/E	Y

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – using Debug Header; E – using Emulation Header.
2: One pin is input-only.

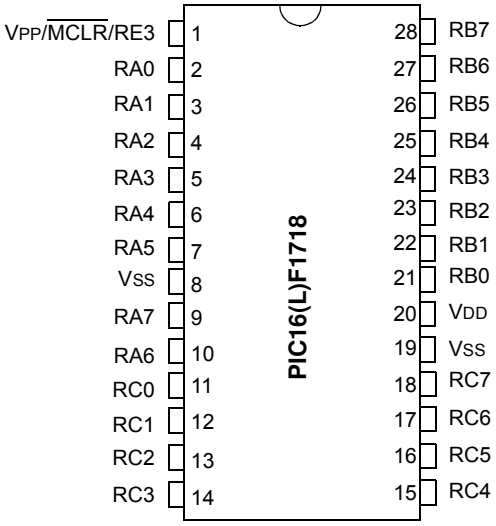
Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001726 PIC16(L)F1713/6 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.
2: DS40001740 PIC16(L)F1717/8/9 Data Sheet, 28/40-Pin Flash, 8-bit Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

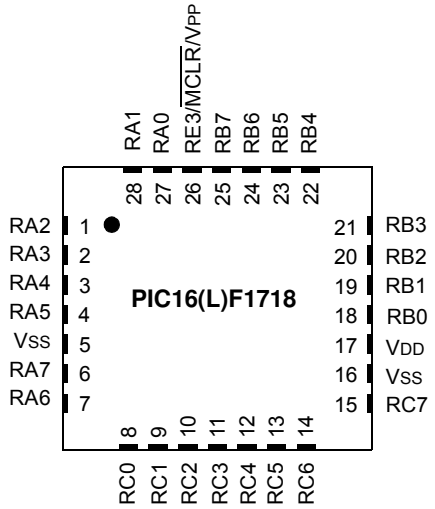
Pin Diagrams

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP



Note: See Table 1 for the pin allocation table.

FIGURE 2: 28-PIN (U)QFN



Note: See Table 1 for the pin allocation table.

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1718)

I/O[2]	SPDIP,SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pull-up	Basic
RA0	2	27	AN0		C1IN0- C2IN0-																							CLCIN0[1]				IOC	Y	
RA1	3	28	AN1		C1IN1- C2IN1-		OPA1OUT																					CLCIN1[1]				IOC	Y	
RA2	4	1	AN2	V_{REF}-	C1IN0+ C2IN0+			DAC1OUT1																								IOC	Y	
RA3	5	2	AN3	V_{REF}+	C1IN1+																											IOC	Y	
RA4	6	3					OPA1IN+			T0CKI[1]																						IOC	Y	
RA5	7	4	AN4				OPA1IN-	DAC2OUT1																nSS[1]								IOC	Y	
RA6	10	7																														IOC	Y	OSC2 CLKOUT
RA7	9	6																														IOC	Y	OSC1 CLKIN
RB0	21	18	AN12		C2IN1+				ZCD										COG1IN[1]													INT[1] IOC	Y	
RB1	22	19	AN10		C1IN3- C2IN3-		OPA2OUT																									IOC	Y	
RB2	23	20	AN8				OPA2IN-																									IOC	Y	
RB3	24	21	AN9		C1IN2- C2IN2-		OPA2IN+																									IOC	Y	
RB4	25	22	AN11																													IOC	Y	
RB5	26	23	AN13							T1G[1]																						IOC	Y	
RB6	27	24																												CLCIN2[1]		IOC	Y	ICSPCLK
RB7	28	25						DAC1OUT2 DAC2OUT2																						CLCIN3[1]			IOC	Y	ICSPDAT
RC0	11	8								T1CKI[1] SOSCO																						IOC	Y	
RC1	12	9								SOSCI			CCP2[1]																			IOC	Y	
RC2	13	10	AN14										CCP1[1]																			IOC	Y	
RC3	14	11	AN15																					SCL/SCK[1]								IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

5: Alternate inputs are excluded from dot shaded areas.

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1718) (CONTINUED)

I/O[2]	SPDIP,SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pull-up	Basic
RC4	15	12	AN16																			SDI[1] SDA[1]									IOC	Y	
RC5	16	13	AN17																												IOC	Y	
RC6	17	14	AN18																						CK[3]						IOC	Y	
RC7	18	15	AN19																						RX[3]						IOC	Y	
RE3	1	26																													IOC	Y	$\overline{MCLR}$ V_{PP}
V_{DD}	20	17																															V_{DD}
V_{SS}	8	5																															V_{SS}
	19	16																															
OUT[4]					C1OUT	C2OUT							CCP1	CCP2	NCO1OUT	PWM3OUT	PWM4OUT	COG1A	COG1B	COG1C	COG1D	SDA[3]	SCK/SCL[3]	SDO	TX/CK	DT[3]	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT			
IN[5]										T1G	T1CKI	T0CKI	CCP1	CCP2				COG1IN				SDI	SCK/SCL[3]	SS	RX[3]	CK	CLCIN0	CLCIN1	CLCIN2	CLCIN3	INT		

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

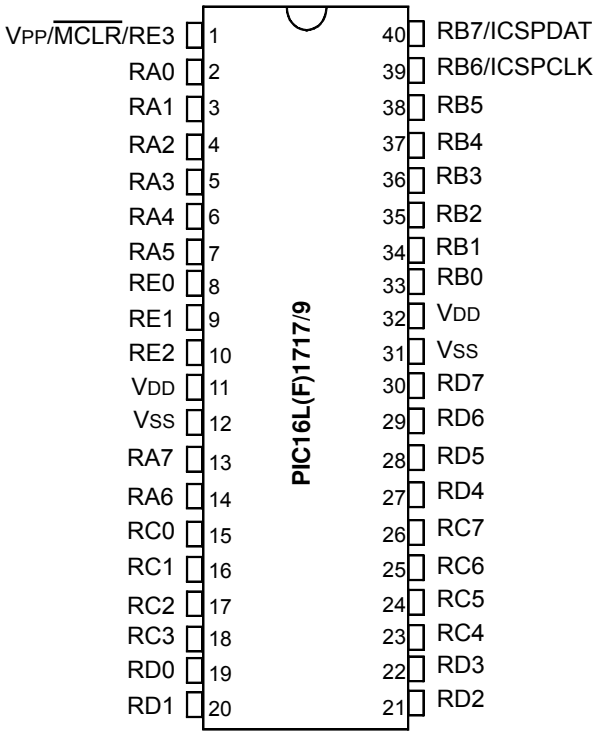
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

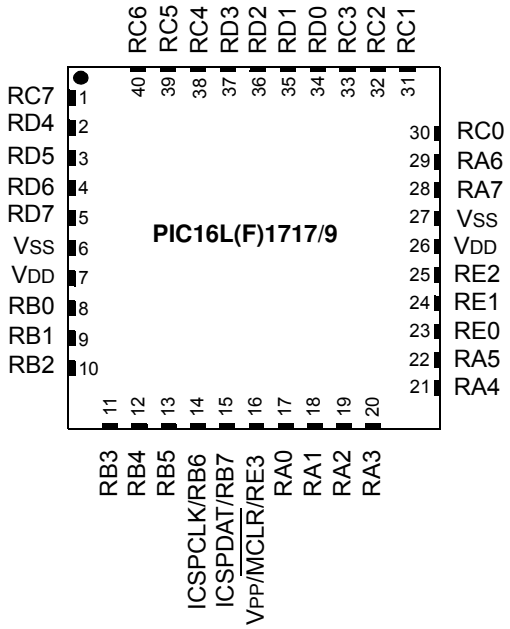
5: Alternate inputs are excluded from dot shaded areas.

FIGURE 3: 40-PIN PDIP



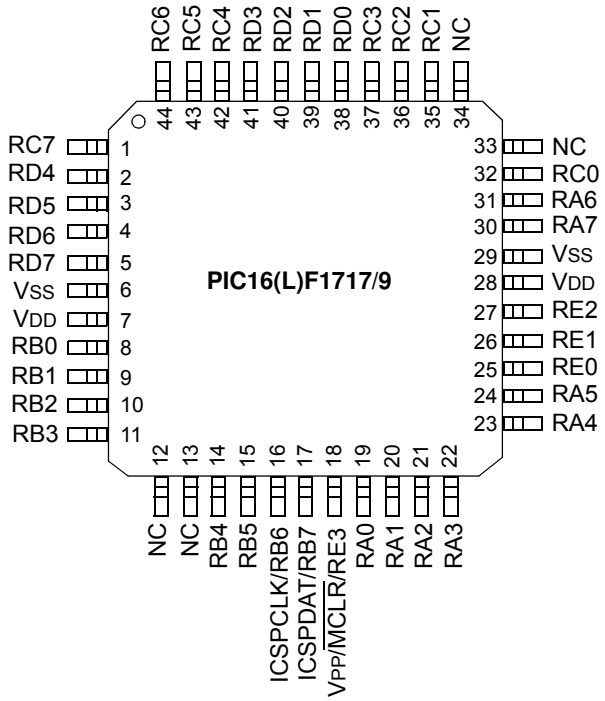
Note: See Table 2 for the pin allocation table.

FIGURE 4: 40-PIN UQFN (5X5)



Note: See Table 2 for the pin allocation table.

FIGURE 5: 44-PIN TQFP (10X10)



Note: See Table 2 for the pin allocation table.

TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1717/9)

I/O(2)	PDIP	TQFP	UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pullup	Basic
RA0	2	19	17	AN0		C1IN0- C2IN0-																						CLCIN0(1)				IOC	Y	
RA1	3	20	18	AN1		C1IN1- C2IN1-		OPA1OUT																				CLCIN1(1)				IOC	Y	
RA2	4	21	19	AN2	V_{REF}-	C1IN0+ C2IN0+			DAC1OUT1																							IOC	Y	
RA3	5	22	20	AN3	V_{REF}+	C1IN1+																										IOC	Y	
RA4	6	23	21					OPA1IN+			T0CKI(1)																					IOC	Y	
RA5	7	24	22	AN4				OPA1IN-	DAC2OUT1															nSS(1)								IOC	Y	
RA6	14	31	29																													IOC	Y	OSC2 CLKOUT
RA7	13	30	28																													IOC	Y	OSC1 CLKIN
RB0	33	8	8	AN12		C2IN1+				ZCD										COG1IN(1)												INT(1) IOC	Y	
RB1	34	9	9	AN10		C1IN3- C2IN3-		OPA2OUT																								IOC	Y	
RB2	35	10	10	AN8				OPA2IN-																								IOC	Y	
RB3	36	11	11	AN9		C1IN2- C2IN2-		OPA2IN+																								IOC	Y	
RB4	37	14	12	AN11																												IOC	Y	
RB5	38	15	13	AN13							T1G(1)																					IOC	Y	
RB6	39	16	14																											CLCIN2(1)			IOC	Y	ICSPCLK
RB7	40	17	15						DAC1OUT2 DAC2OUT2																					CLCIN3(1)			IOC	Y	ICSPDAT
RC0	15	32	30								T1CKI(1) SOSCO																					IOC	Y	
RC1	16	35	31								SOSCI			CCP2(1)																		IOC	Y	
RC2	17	36	32	AN14										CCP1(1)																		IOC	Y	
RC3	18	37	33	AN15																				SCL/SCK(1)								IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

5: Alternate inputs are excluded from dot shaded areas.

TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1717/9) (CONTINUED)

I/O(2)	PDIP	TQFP	UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pullup	Basic
RC4	23	42	38	AN16																			SDI(1) SDA(1)									IOC	Y	
RC5	24	43	39	AN17																												IOC	Y	
RC6	25	44	40	AN18																						CK(3)						IOC	Y	
RC7	26	1	1	AN19																						RX(3)						IOC	Y	
RD0	19	38	34	AN20																													Y	
RD1	20	39	35	AN21																													Y	
RD2	21	40	36	AN22																													Y	
RD3	22	41	37	AN23																													Y	
RD4	27	2	2	AN24																													Y	
RD5	28	3	3	AN25																													Y	
RD6	29	4	4	AN26																													Y	
RD7	30	5	5	AN27																													Y	
RE0	8	25	23	AN5																													Y	
RE1	9	26	24	AN6																													Y	
RE2	10	27	25	AN7																													Y	
RE3	1	18	16																													IOC	Y	$\overline{MCLR}$ V_{PP}
V_{DD}	11	7	7																														V_{DD}
	32	28	26																														
V_{SS}	12	6	6																														V_{SS}
	31	29	27																														
OUT(4)						C1OUT	C2OUT							CCP1	CCP2	NCO1OUT	PWM3OUT	PWM4OUT	COG1A	COG1B	COG1C	COG1D	SDA(3)	SCK/SCL(3)	SDO	TX/CK	DT(3)	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT			
IN(5)											T1G	T1CKI	T0CKI	CCP1	CCP2				COG1IN				SDI	SCK/SCL(3)	SS	RX(3)	CK	CLCIN0	CLCIN1	CLCIN2	CLCIN3	INT		

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

5: Alternate inputs are excluded from dot shaded areas.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

The PIC16(L)F1717/8/9 devices are described within this data sheet. They are available in the following package configurations:

- 28-pin SPDIP, SSOP, SOIC, QFN and UQFN
- 40-pin PDIP and UQFN
- 44-pin TQFP

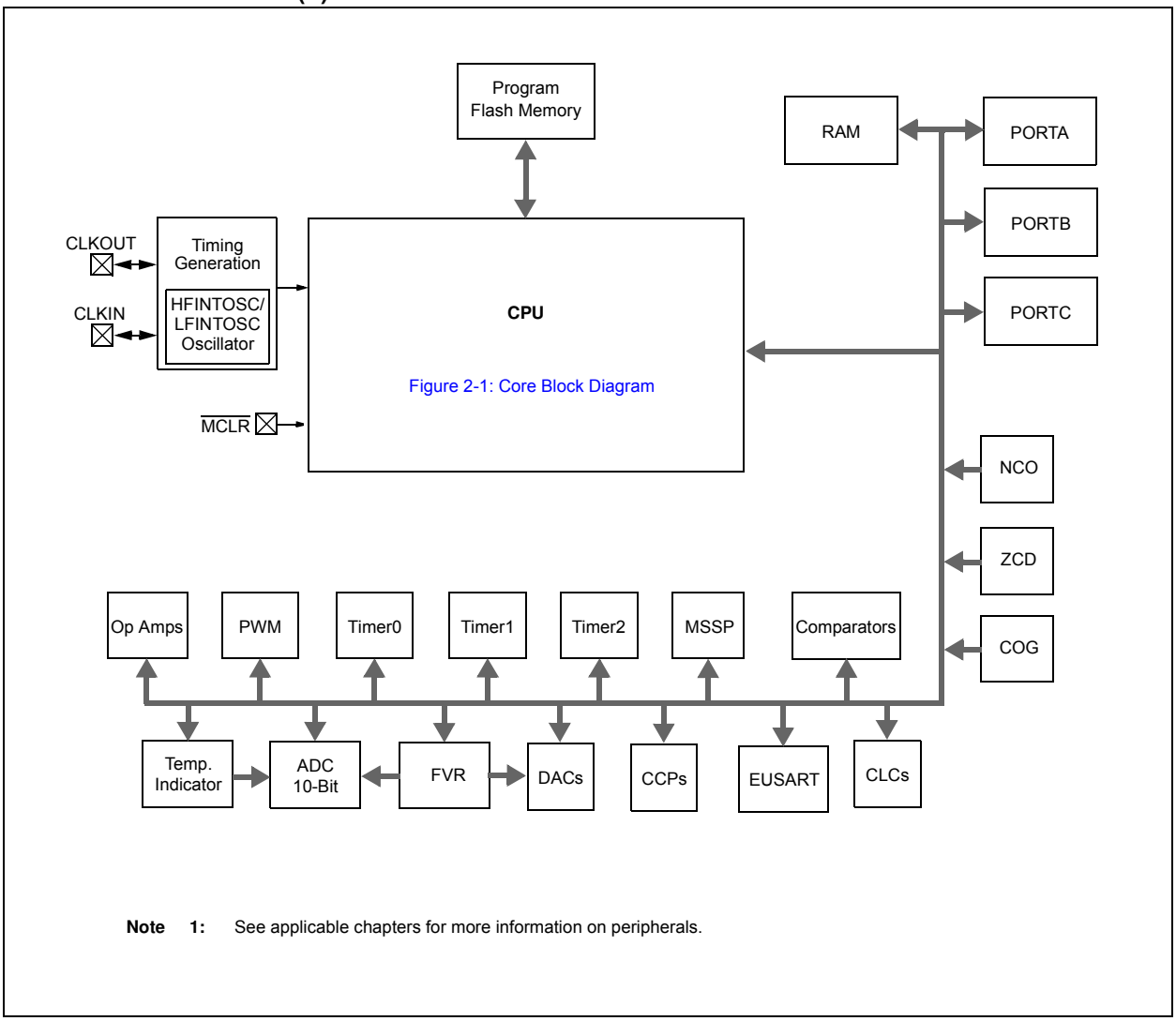
Figure 1-1 and Figure 1-2 show block diagrams of the PIC16(L)F1717/8/9 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

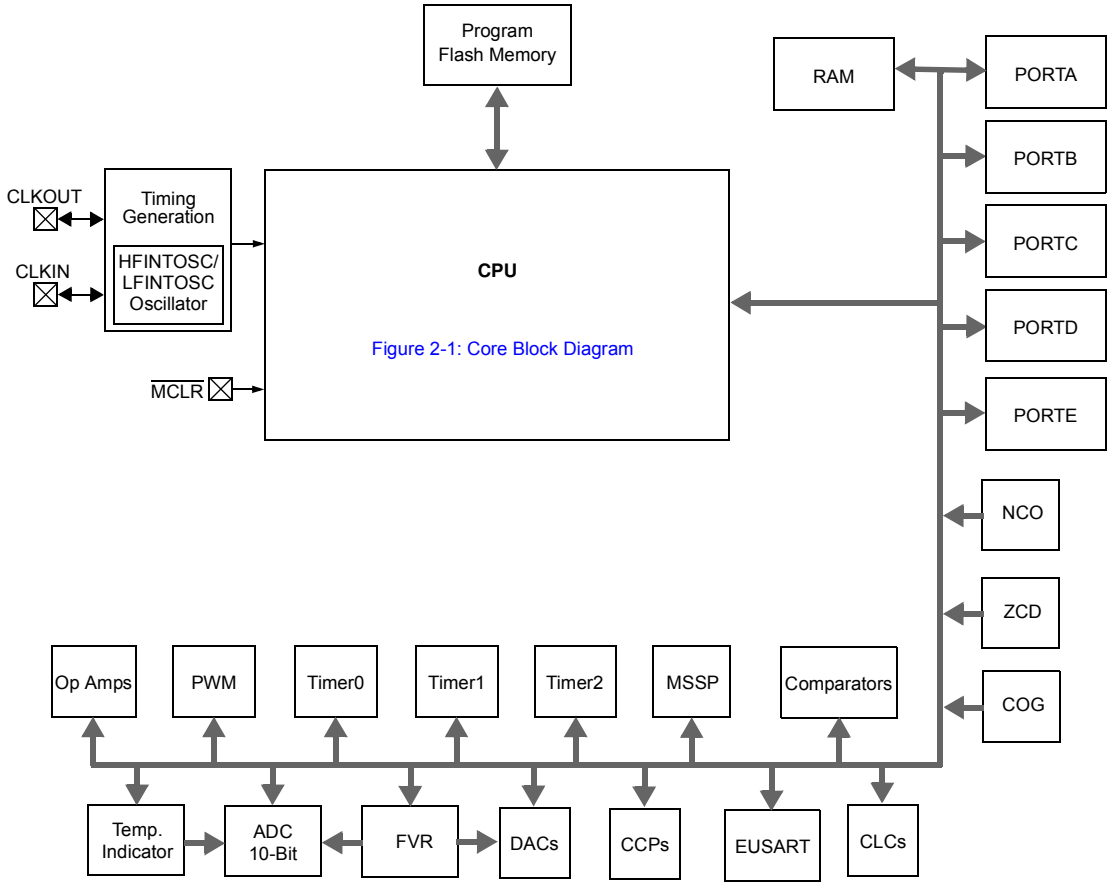
Peripheral		PIC16(L)F1717	PIC16(L)F1718	PIC16(L)F1719
Analog-to-Digital Converter (ADC)		●	●	●
Fixed Voltage Reference (FVR)		●	●	●
Zero-Cross Detection (ZCD)		●	●	●
Temperature Indicator		●	●	●
Complementary Output Generator (COG)				
	COG	●	●	●
Numerically Controlled Oscillator (NCO)				
	NCO	●	●	●
Digital-to-Analog Converter (DAC)				
	DAC1	●	●	●
	DAC2	●	●	●
Capture/Compare/PWM (CCP/ECCP) Modules				
	CCP1	●	●	●
	CCP2	●	●	●
Comparators				
	C1	●	●	●
	C2	●	●	●
Configurable Logic Cell (CLC)				
	CLC1	●	●	●
	CLC2	●	●	●
	CLC3	●	●	●
	CLC4	●	●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)				
	EUSART	●	●	●
Master Synchronous Serial Ports				
	MSSP	●	●	●
Op Amp				
	Op Amp 1	●	●	●
	Op Amp 2	●	●	●
Pulse-Width Modulator (PWM)				
	PWM3	●	●	●
	PWM4	●	●	●
Timers				
	Timer0	●	●	●
	Timer1	●	●	●
	Timer2	●	●	●

FIGURE 1-1: PIC16(L)F1718 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

FIGURE 1-2: PIC16(L)F1717/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1718 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ CLCIN0(1)	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator C2 negative input.
	C2IN0-	AN	—	Comparator C3 negative input.
	CLCIN0	TTL/ST	—	Configurable Logic Cell source input.
RA1/AN1/C1IN1-/C2IN1-/ OPA1OUT/CLCIN1(1)	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
	CLCIN1	TTL/ST	—	Configurable Logic Cell source input.
RA2/AN2/VREF-/C1IN0+/C2IN0+/ DAC1OUT1	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	VREF-	AN	—	ADC Negative Voltage Reference input.
	C1IN0+	AN	—	Comparator C2 positive input.
	C2IN0+	AN	—	Comparator C3 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
RA3/AN3/VREF+/C1IN1+	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC Voltage Reference input.
	C1IN1+	AN	—	Comparator C1 positive input.
RA4/OPA1IN+/T0CKI(1)	RA4	TTL/ST	CMOS	General purpose I/O.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	T0CKI	TTL/ST	—	Timer0 gate input.
RA5/AN4/OPA1IN-/DAC2OUT1/ $\overline{SS}$(1)	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	DAC2OUT1	—	AN	Digital-to-Analog Converter output.
	$\overline{SS}$	TTL/ST	—	Slave Select enable input.
RA6/OSC2/CLKOUT	RA6	TTL/ST	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA7/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External clock input (EC mode).
RB0/AN12/C2IN1+/ZCD/ COGIN(1)	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	ZCD	AN	—	Zero-Cross Detection Current Source/Sink.
	COGIN	TTL/ST	CMOS	Complementary Output Generator input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1718 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB1/AN10/C1IN3-/C2IN3-/ OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
RB3/AN9/C1IN2-/C2IN2-/ OPA2IN+	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
RB4/AN11	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
RB5/AN13/T1G(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	T1G	TTL/ST	—	Timer1 gate input.
RB6/CLCIN2(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	CLCIN2	TTL/ST	—	Configurable Logic Cell source input.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/DAC2OUT2/ CLCIN3(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	DAC2OUT2	—	AN	Digital-to-Analog Converter output.
	CLCIN3	TTL/ST	—	Configurable Logic Cell source input.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1CKI(1)/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	T1CKI	TTL/ST	—	Timer1 clock input.
	SOSCO	XTAL	XTAL	Secondary Oscillator Connection.
RC1/SOSCI/CCP2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	SOSCI	XTAL	XTAL	Secondary Oscillator Connection.
	CCP2	TTL/ST	—	Capture input
RC2/AN14/CCP1(1)	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	CCP1	TTL/ST	—	Capture input
RC3/AN15/SCK(1)/SCL(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	SCK	TTL/ST	—	SPI clock input
	SCL	I^2C	—	I^2C clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1718 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN16/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	SDI	TTL/ST	—	SPI Data input.
	SDA	I^2C	—	I^2C Data input.
RC5/AN17	RC5	TTL/ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
RC6/AN18/CK(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	CK	TTL/ST		EUSART synchronous clock.
RC7/AN19/RX(1)	RC7	TTL/ST	CMOS	General purpose I/O.
	AN19	AN	—	ADC Channel 19 input.
	RX	TTL/ST	—	EUSART receive.
RE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master clear input.
	VPP	HV	—	Programming enable.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	NCO1OUT		CMOS	Numerically controlled oscillator output.
	PWM3OUT		CMOS	PWM3 output.
	PWM4OUT		CMOS	PWM4 output.
	COG1A		CMOS	Complementary output generator output A.
	COG1B		CMOS	Complementary output generator output B.
	COG1C		CMOS	Complementary output generator output C.
	COG1D		CMOS	Complementary output generator output D.
	SDA(3)		OD	I^2C Data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX/CK		CMOS	EUSART asynchronous TX data/synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable Logic Cell 1 output.
	CLC2OUT		CMOS	Configurable Logic Cell 2 output.
	CLC3OUT		CMOS	Configurable Logic Cell 3 output.
	CLC4OUT		CMOS	Configurable Logic Cell 4 output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1717/9 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0-/C2IN0-/ CLCIN0(1)	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0-	AN	—	Comparator C2 negative input.
	C2IN0-	AN	—	Comparator C3 negative input.
	CLCIN0	TTL/ST	—	Configurable Logic Cell source input.
RA1/AN1/C1IN1-/C2IN1-/ OPA1OUT/CLCIN1(1)	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
	CLCIN1	TTL/ST	—	Configurable Logic Cell source input.
RA2/AN2/VREF-/C1IN0+/C2IN0+/ DAC1OUT1	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	VREF-	AN	—	ADC Negative Voltage Reference input.
	C1IN0+	AN	—	Comparator C2 positive input.
	C2IN0+	AN	—	Comparator C3 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
RA3/AN3/VREF+/C1IN1+	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC Voltage Reference input.
	C1IN1+	AN	—	Comparator C1 positive input.
RA4/OPA1IN+/T0CKI(1)	RA4	TTL/ST	CMOS	General purpose I/O.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	T0CKI	TTL/ST	—	Timer0 gate input.
RA5/AN4/OPA1IN-/DAC2OUT1/ $\overline{SS}$(1)	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	DAC2OUT1	—	AN	Digital-to-Analog Converter output.
	$\overline{SS}$	—	—	Slave Select enable input.
RA6/OSC2/CLKOUT	RA6	TTL/ST	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA7/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External clock input (EC mode).
RB0/AN12/C2IN1+/ZCD/ COGIN(1)	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	ZCD	AN	—	Zero-Cross Detection Current Source/Sink.
	COGIN	TTL/ST	—	Complementary Output Generator input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1717/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB1/AN10/C1IN3-/C2IN3-/ OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
RB3/AN9/C1IN2-/C2IN2-/ OPA2IN+	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
RB4/AN11	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
RB5/AN13/T1G(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	T1G	TTL/ST	—	Timer1 gate input.
RB6/CLCIN2(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	CLCIN2	TTL/ST	—	Configurable Logic Cell source input.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/DAC2OUT2/ CLCIN3(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	DAC2OUT2	—	AN	Digital-to-Analog Converter output.
	CLCIN3	TTL/ST	—	Configurable Logic Cell source input.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1CKI(1)/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	T1CKI	ST	—	Timer1 clock input.
	SOSCO	XTAL	XTAL	Secondary Oscillator Connection.
RC1/SOSCI/CCP2(1)	RC1	TTL/ST	CMOS	General purpose I/O.
	SOSCI	XTAL	XTAL	Secondary Oscillator Connection.
	CCP2	TTL/ST	—	Capture input.
RC2/AN14/CCP1(1)	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	CCP1	TTL/ST	—	Capture input.
RC3/AN15/SCK(1)/SCL(1)	RC3	TTL/ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	SCK	TTL/ST	—	SPI clock input.
	SCL	I^2C	OD	I^2C clock.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1717/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN16/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	SDI	TTL/ST	—	SPI Data input.
	SDA(3)	I^2C	—	I^2C Data input.
RC5/AN17	RC5	TTL/ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
RC6/AN18/CK(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	CK	TTL/ST		EUSART synchronous clock.
RC7/AN19/RX(1)	RC7	TTL/ST	CMOS	General purpose I/O.
	AN19	AN	—	ADC Channel 19 input.
	RX	TTL/ST	—	EUSART receive.
RDO/AN20	RD0	TTL/ST	CMOS	General purpose I/O.
	AN20	AN	—	ADC Channel 20 input.
RD1/AN21	RD1	TTL/ST	CMOS	General purpose I/O.
	AN21	AN	—	ADC Channel 21 input.
RD2/AN22	RD2	TTL/ST	CMOS	General purpose I/O.
	AN22	AN	—	ADC Channel 22 input.
RD3/AN23	RD3	TTL/ST	CMOS	General purpose I/O.
	AN23	AN	—	ADC Channel 23 input.
RD4/AN24	RD4	TTL/ST	CMOS	General purpose I/O.
	AN24	AN	—	ADC Channel 24 input.
RD5/AN25	RD5	TTL/ST	CMOS	General purpose I/O.
	AN25	AN	—	ADC Channel 25 input.
RD6/AN26	RD6	TTL/ST	CMOS	General purpose I/O.
	AN26	AN	—	ADC Channel 26 input.
RD7/AN27	RD7	TTL/ST	CMOS	General purpose I/O.
	AN27	AN	—	ADC Channel 27 input.
RE0/AN5	RE0	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
RE1/AN6	RE1	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
RE2/AN7	RE2	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
RE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master clear input.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1717/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	NCO1OUT		CMOS	Numerically controlled oscillator output.
	PWM3OUT		CMOS	PWM3 output.
	PWM4OUT		CMOS	PWM4 output.
	COG1A		CMOS	Complementary output generator output A.
	COG1B		CMOS	Complementary output generator output B.
	COG1C		CMOS	Complementary output generator output C.
	COG1D		CMOS	Complementary output generator output D.
	SDA(3)		OD	I^2C Data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX/CK		CMOS	EUSART asynchronous TX data/synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable Logic Cell 1 output.
	CLC2OUT		CMOS	Configurable Logic Cell 2 output.
	CLC3OUT		CMOS	Configurable Logic Cell 3 output.
	CLC4OUT		CMOS	Configurable Logic Cell 4 output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

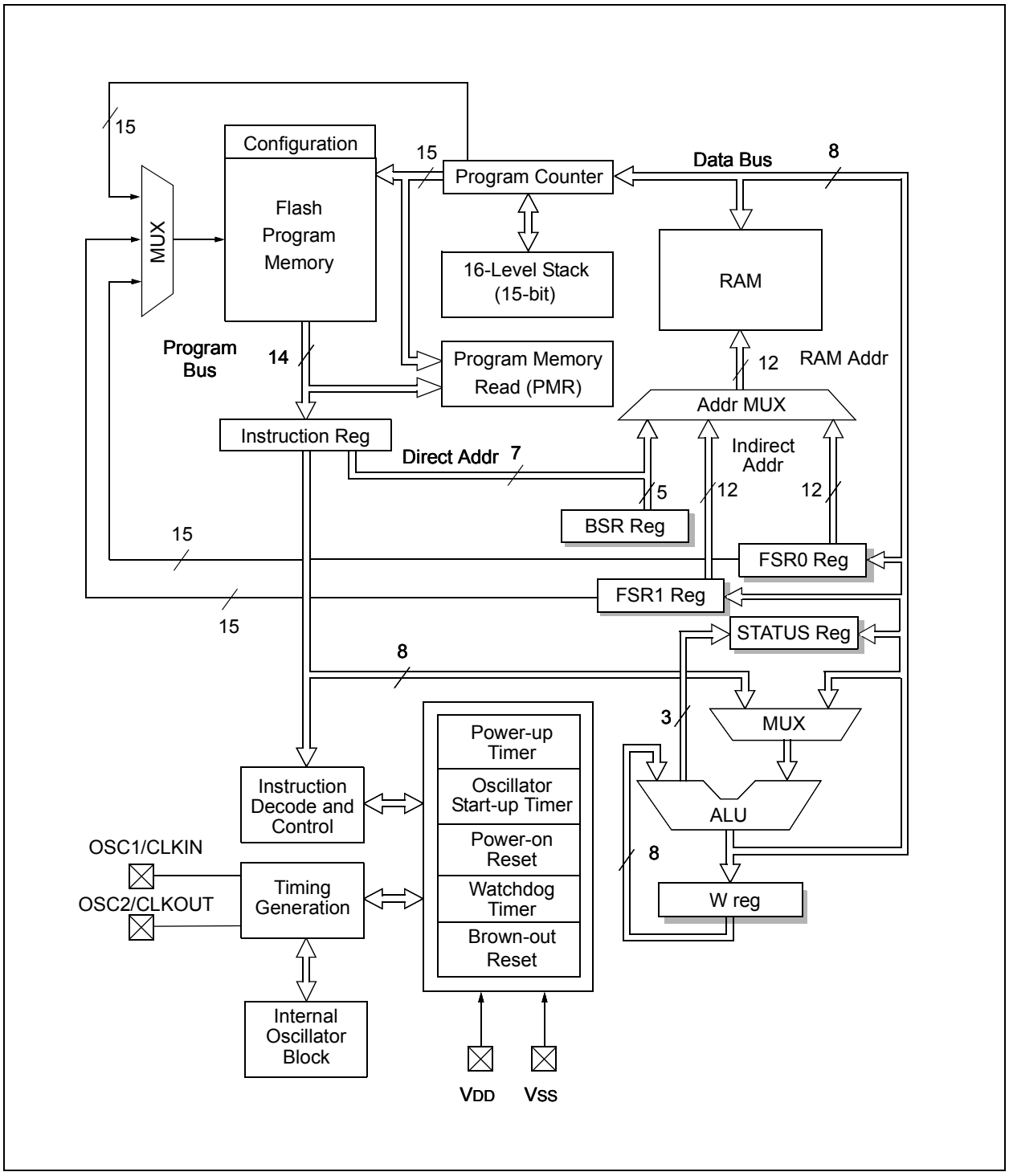
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

2.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"** for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 3.6 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.7 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 33.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

Note 1: The method to access Flash memory through the PMCON registers is described in **Section 10.0 "Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1717/8/9 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

3.2 High-Endurance Flash

This device has a 128-byte section of high-endurance program Flash memory (PFM) in lieu of data EEPROM. This area is especially well suited for nonvolatile data storage that is expected to be updated frequently over the life of the end product. See **Section 10.2 "Flash Program Memory Overview"** for more information on writing data to PFM. See **Section 3.2.1.2 "Indirect Read with FSR"** for more information about using the FSR registers to read byte data stored in PFM.

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range(1)
PIC16(L)F1717	8,192	1FFFh	1F80h-1FFFh
PIC16(L)F1718/9	16,384	3FFFh	3F80h-3FFFh

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1717

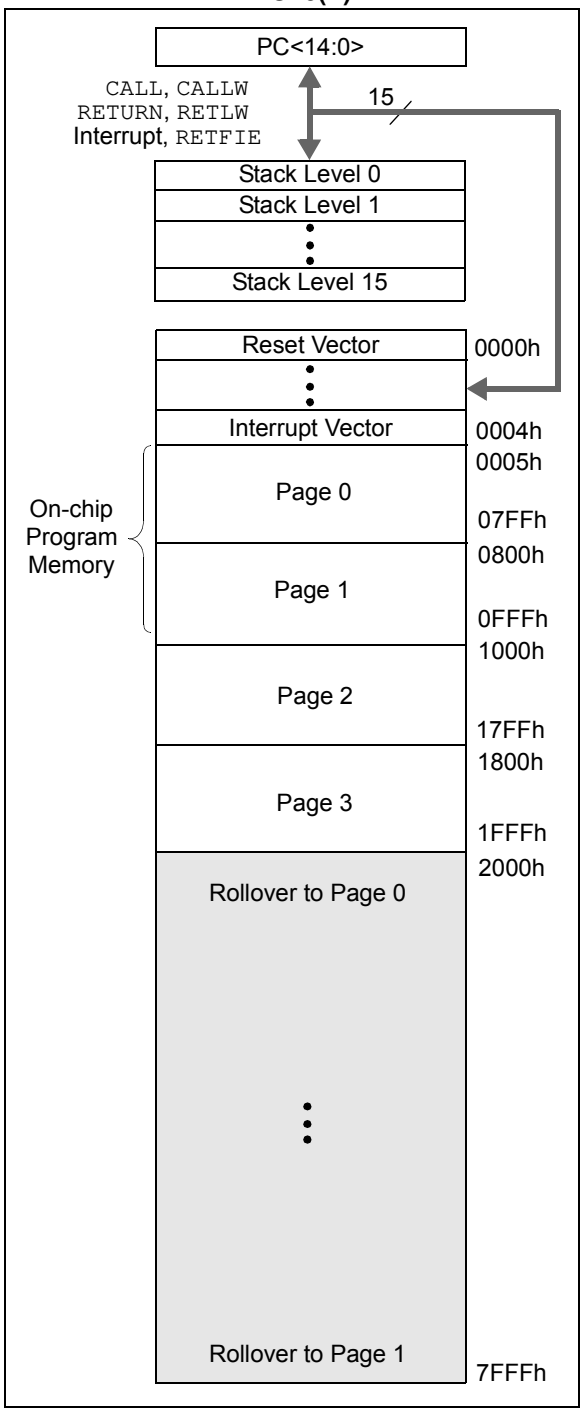


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1718/9