Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PIC16(L)F1764/5/8/9

14/20-Pin, 8-Bit Flash Microcontrollers

Description

The PIC16(L)F1764/5/8/9 family offers intelligent analog with digital peripherals to create up to two independent closed-loop channels. These 14 and 20-pin devices enable the ability to interconnect the on-chip peripherals to create custom functions specific to each application; helping simplify the implementation of a complex control system and give designers the flexibility to innovate.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (EWDT):
  - Low-power 31 kHz WDT
  - Software-selectable prescaler
  - Software-selectable enable

Memory

- Up to 14 Kbytes Flash Program Memory
- Up to 1024 Bytes Data RAM Memory
- Direct, Indirect and Relative Addressing modes
- High-Endurance Flash (HEF):
  - 128B of nonvolatile data storage
  - 100K erase/write cycles

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1764/5/8/9)
  - 2.3V to 5.5V (PIC16F1764/5/8/9)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 32 μA/MHz @ 1.8V, typical
- Low-Power BOR (LPBOR):
  - 200 nA in Sleep

Digital Peripherals

- Configurable Logic Cell (CLC):
  - Up to three CLCs; up to four selected inputs
  - Integrated combinational and state logic
- Up to Two Complementary Output Generators (COG):
  - Push-Pull, Full-Bridge and Steering modes
- Up to Two Capture/Compare/PWM (CCP) modules
- Pulse-Width Modulators (PWM):
  - Up to two 10-bit PWMs
  - Up to two 16-bit PWMs
- Peripheral Pin Select (PPS):
  - Configure any digital pin to output
- Serial Communications:
  - Enhanced USART (EUSART)
  - SPI, I^2C, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-On-Change (IOC) with edge select
- Up to Two Data Signal Modulators (DSM)

Intelligent Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 12 external channels
  - Conversion available during Sleep
- Up to Two Operational Amplifiers (OPA):
  - Selectable internal and external channels
- Up to Four Fast Comparators (COMP):
  - Up to five external inverting inputs
  - Up to eight external non-inverting inputs
  - Fixed Voltage Reference at non-inverting input(s)
  - Comparator outputs externally accessible
- Digital-to-Analog Converters (DAC):
  - Up to two 10-bit resolution DACs
  - Up to two 5-bit resolution DACs

Intelligent Analog Peripherals (Cont.)

- Voltage Reference:
  - Fixed Voltage Reference (FVR): 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detector (ZCD):
  - Detect high-voltage AC signal
- Programmable Ramp Generator (PRG):
  - Slope compensation
  - Ramp generation
- High-Current Drive I/Os:
  - 100 mA capacity @ 5V

Clocking Structure

- 16 MHz Internal Oscillator:
  - ±1% at calibration
  - Selectable frequency range, 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 4x Phase-Locked Loop (PLL):
  - For up to 32 MHz internal operation
- External Oscillator Block with:
  - Three External Clock modes up to 32 MHz

TABLE 1: PIC16(L)F1764/5/8/9 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (Words/Kbytes)	High-Endurance Flash (B)	Data SRAM (Bytes)	I/O Pins(2)	16-Bit Timers	8-Bit Timers w/HLT	Comparator	10-Bit ADC (ch)	5/10-Bit DAC	CCP	10/16-Bit PWM	COG	Data Signal Modulator	CLC	Op Amp	Zero-Cross Detect	Programmable Ramp Gen	High-Current I/Os	Peripheral Pin Select	EUSART	I^2C/SPI	Debug(1)
PIC16(L)F1764	**(A)**	4096/7	128	512	12	3	1/3	2	8	1/1	1	1/1	1	1	3	1	1	1	2	Y	1	1	I/H
PIC16(L)F1765	**(A)**	8192/14	128	1024	12	3	1/3	2	8	1/1	1	1/1	1	1	3	1	1	1	2	Y	1	1	I/H
PIC16(L)F1768	**(A)**	4096/7	128	512	18	3	1/3	4	12	2/2	2	2/2	2	2	3	2	1	2	2	Y	1	1	I/H
PIC16(L)F1769	**(A)**	8192/14	128	1024	18	3	1/3	4	12	2/2	2	2/2	2	2	3	2	1	2	2	Y	1	1	I/H

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – via ICD Header; E – Emulation Product.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

A. DS-40001775 PIC16(L)F1764/5/8/9 Data Sheet, 14/20-Pin 8-Bit Flash Microcontrollers.

Note: For other small form factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

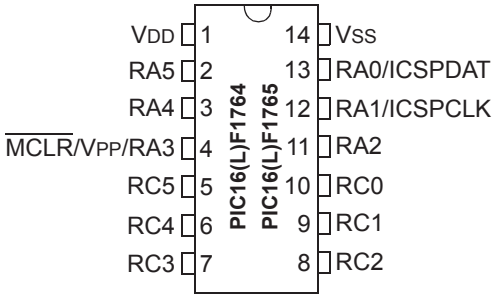
TABLE 2: PACKAGES

Packages	PDIP	SOIC	TSSOP	QFN	SSOP
PIC16(L)F1764	●	●	●	●	
PIC16(L)F1765	●	●	●	●	
PIC16(L)F1768	●	●		●	●
PIC16(L)F1769	●	●		●	●

Note: Pin details are subject to change.

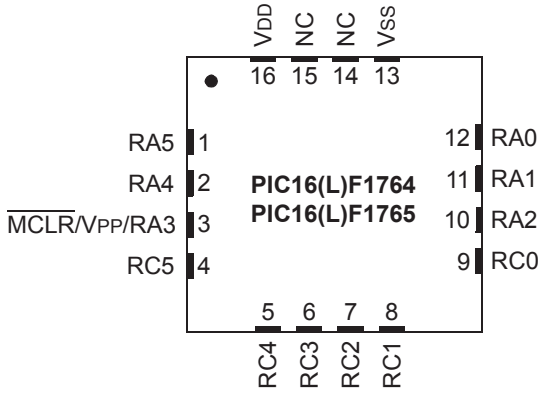
PIN DIAGRAMS

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



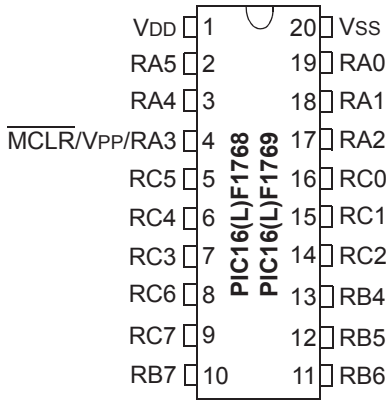
Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 16-PIN QFN (4x4)



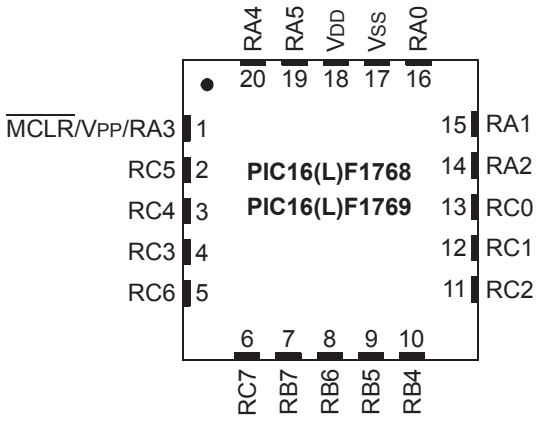
Note: See Table 3 for location of all peripheral functions.

FIGURE 3: 20-PIN PDIP, SOIC, SSOP



Note: See Table 4 for location of all peripheral functions.

FIGURE 4: 20-PIN QFN (4x4)



Note: See Table 4 for location of all peripheral functions.

PIN ALLOCATION TABLES

TABLE 3: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1764/5)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RA0	13	12	AN0	VREF- DAC1REF- DAC3REF-	DAC1OUT1 DAC3OUT1	—	C1IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPDAT
RA1	12	11	AN1	VREF+ DAC1REF+ DAC3REF+	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPCLK
RA2	11	10	AN2	—	—	—	—	ZCD	—	T0CKI(1)	—	—	COG1IN(1)	—	—	—	—	INT(1) IOC	Y	—	—
RA3	4	3	—	—	—	—	—	—	—	T6IN(1)	—	—	—	—	MD1CH(1)	—	—	IOC	Y	—	$\frac{V_{PP}}{MCLR}$
RA4	3	2	AN3	—	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	MD1CL(1)	—	—	IOC	Y	—	OSC2 CLKOUT
RA5	2	1	—	—	—	—	—	—	—	T1CKI(1) T2IN(1) SOSCI	—	—	—	CLCIN3(1)	MD1MOD(1)	—	—	IOC	Y	—	OSC1 CLKIN
RC0	10	9	AN4	—	—	OPA1IN+	C2IN0+	—	—	T5CKI(1)	—	—	—	—	—	—	SCL(1) SCK(1,3)	IOC	Y	—	—
RC1	9	8	AN5	—	—	OPA1IN-	C1IN1- C2IN1-	—	—	T4IN(1)	—	—	—	CLCIN2(1)	—	—	SDI(1) SDA(1,3)	IOC	Y	—	—
RC2	8	7	AN6	—	—	OPA1OUT	C1IN2- C2IN2-	—	PRG1IN0	—	—	—	—	—	—	—	—	IOC	Y	—	—
RC3	7	6	AN7	—	—	—	C1IN3- C2IN3-	—	—	T5G(1)	—	—	—	CLCIN0(1)	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC4	6	5	—	—	—	—	—	—	PRG1R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	CK(1)	—	IOC	Y	Y	—
RC5	5	4	—	—	—	—	—	—	PRG1F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	RX(1,3)	—	IOC	Y	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3	CCP1	COG1A	CLC1OUT	MD1OUT	DT(3)	SDO	INT	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM5	—	COG1B	CLC2OUT	—	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG1C	CLC3OUT	—	CK	SCK	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG1D	—	—	—	SCL(3)	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768/9)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RA0	19	16	AN0	VREF- DAC1REF- DAC2REF- DAC3REF- DAC4REF-	DAC1OUT1 DAC2OUT1 DAC3OUT1 DAC4OUT1	—	C1IN0+ C3IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPDAT
RA1	18	15	AN1	VREF+ DAC1REF+ DAC2REF+ DAC3REF+ DAC4REF+	—	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPCLK
RA2	17	14	AN2	—	—	—	—	ZCD	—	T0CKI(1)	—	—	COG1IN(1) COG2IN(1)	—	—	—	—	INT(1) IOC	Y	—	—
RA3(4)	4	1	—	—	—	—	—	—	—	T6IN(1)	—	—	—	—	MD1CH(1) MD2CH(1)	—	—	IOC	Y	—	VPP MCLR ICD
RA4	3	20	AN3	—	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	MD1CL(1) MD2CL(1)	—	—	IOC	Y	—	OSC2 CLKOUT
RA5	2	19	—	—	—	—	—	—	—	T1CKI(1) T2IN(1) SOSCI	—	—	—	CLCIN3(1)	MD1MOD(1) MD2MOD(1)	—	—	IOC	Y	—	OSC1 CLKIN
RB4	13	10	AN10	—	—	OPA1IN0-	—	—	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3)	IOC	Y	—	—
RB5	12	9	AN11	—	—	OPA1IN0+	—	—	—	—	—	—	—	—	—	RX(1,3)	—	IOC	Y	—	—
RB6	11	8	—	—	—	—	C1IN1+ C3IN1+	—	—	—	—	—	—	—	—	—	SCL(1) SCK(1,3)	IOC	Y	—	—
RB7	10	7	—	—	—	—	C2IN1+ C4IN1+	—	—	—	—	—	—	—	—	CK(1)	—	IOC	Y	—	—
RC0	16	13	AN4	—	—	—	C2IN0+ C4IN0+	—	—	T5CKI(1)	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	15	12	AN5	—	—	—	C1IN1- C2IN1- C3IN1- C4IN1-	—	—	T4IN(1)	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	—
RC2	14	11	AN6	—	—	OPA1OUT OPA2IN1- OPA2IN1+	C1IN2- C2IN2-	—	PRG1IN0 PRG2IN1	—	—	—	—	—	—	—	—	IOC	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.
2: All pin outputs default to PORT latch data. Any input capable pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Input only.

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768/9) (CONTINUED)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RC3	7	4	AN7	—	—	OPA2OUT OPA1IN1- OPA1IN1+	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1	T5G(1)	—	CCP2(1)	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RC4	6	3	—	—	—	—	—	—	PRG1R(1) PRG2R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	Y	—
RC5	5	2	—	—	—	—	—	—	PRG1F(1) PRG2F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	—	—	IOC	Y	Y	—
RC6	8	5	AN8	—	—	OPA2IN0-	—	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC7	9	6	AN9	—	—	OPA2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3	CCP1	COG1A	CLC1OUT	MD1OUT	DT(3)	SDO	—	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM4	CCP2	COG1B	CLC2OUT	MD2OUT	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	C3OUT	—	—	—	PWM5	—	COG1C	CLC3OUT	—	CK	SCK	—	—	—	—
	—	—	—	—	—	—	C4OUT	—	—	—	PWM6	—	COG1D	—	—	—	SCL(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2A	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2B	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2C	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2D	—	—	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.
2: All pin outputs default to PORT latch data. Any input capable pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Input only.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

The PIC16(L)F1764/5/8/9 are described within this data sheet. See Table 2 for available package configurations.

Figure 1-1 shows a block diagram of the PIC16(L)F1764/5 devices. Figure 1-2 shows a block diagram of the PIC16(L)F1768/9 devices. Table 1-2 and Table 1-3 show the pinout descriptions.

Refer to Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1764	PIC16(L)F1765	PIC16(L)F1768	PIC16(L)F1769
Analog-to-Digital Converter (ADC)		●	●	●	●
Fixed Voltage Reference (FVR)		●	●	●	●
Zero-Cross Detection (ZCD)		●	●	●	●
Temperature Indicator		●	●	●	●
Complementary Output Generator (COG)					
	COG1	●	●	●	●
	COG2			●	●
Programmable Ramp Generator (PRG)					
	PRG1	●	●	●	●
	PRG2			●	●
10-Bit Digital-to-Analog Converter (DAC)					
	DAC1	●	●	●	●
	DAC2			●	●
5-Bit Digital-to-Analog Converter (DAC)					
	DAC3	●	●	●	●
	DAC4			●	●
Capture/Compare/PWM (CCP/ECCP) Modules					
	CCP1	●	●	●	●
	CCP2			●	●
Comparators					
	C1	●	●	●	●
	C2	●	●	●	●
	C3			●	●
	C4			●	●
Configurable Logic Cell (CLC)					
	CLC1	●	●	●	●
	CLC2	●	●	●	●
	CLC3	●	●	●	●
Data Signal Modulator (DSM)					
	DSM1	●	●	●	●
	DSM2			●	●

TABLE 1-1: DEVICE PERIPHERAL SUMMARY (CONTINUED)

Peripheral		PIC16(L)F1764	PIC16(L)F1765	PIC16(L)F1768	PIC16(L)F1769
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)					
	EUSART	●	●	●	●
Master Synchronous Serial Ports					
	MSSP	●	●	●	●
Op Amp					
	Op Amp 1	●	●	●	●
	Op Amp 2			●	●
10-Bit Pulse-Width Modulator (PWM)					
	PWM3	●	●	●	●
	PWM4			●	●
16-Bit Pulse-Width Modulator (PWM)					
	PWM5	●	●	●	●
	PWM6			●	●
8-Bit Timers					
	Timer0	●	●	●	●
	Timer2	●	●	●	●
	Timer4	●	●	●	●
	Timer6	●	●	●	●
16-Bit Timers					
	Timer1	●	●	●	●
	Timer3	●	●	●	●
	Timer5	●	●	●	●

1.1 Register and Bit Naming Conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterName*bits.*ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2, and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW  ~(1<<G1MD1)
ANDWF  COG1CON0,F
MOVLW  1<<G1MD2 | 1<<G1MD0
IORWF  COG1CON0,F
```

Example 2:

```
BSF    COG1CON0,G1MD2
BCF    COG1CON0,G1MD1
BSF    COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt and Mirror Bits

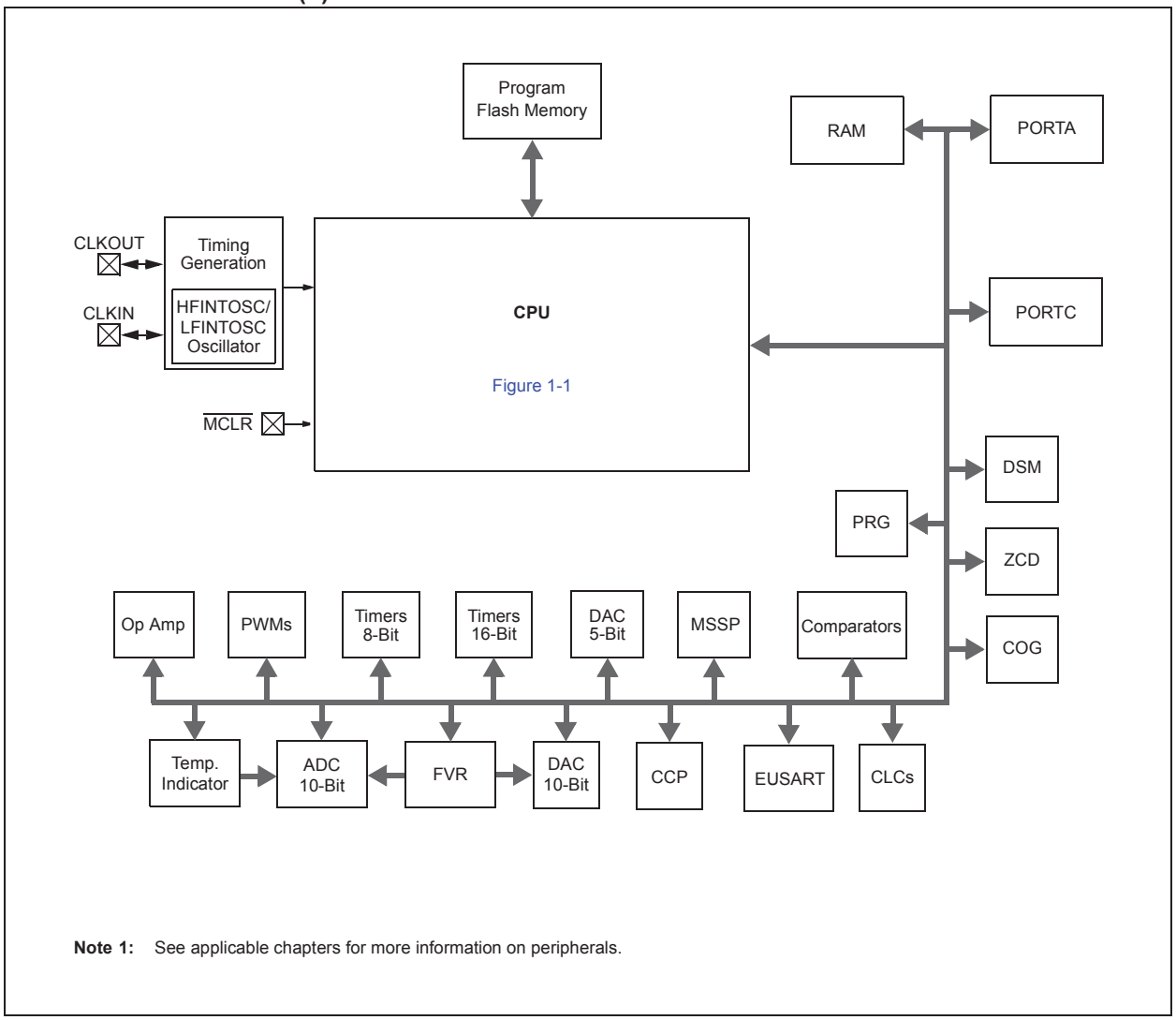
Status, interrupt enables, interrupt flags and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique, so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

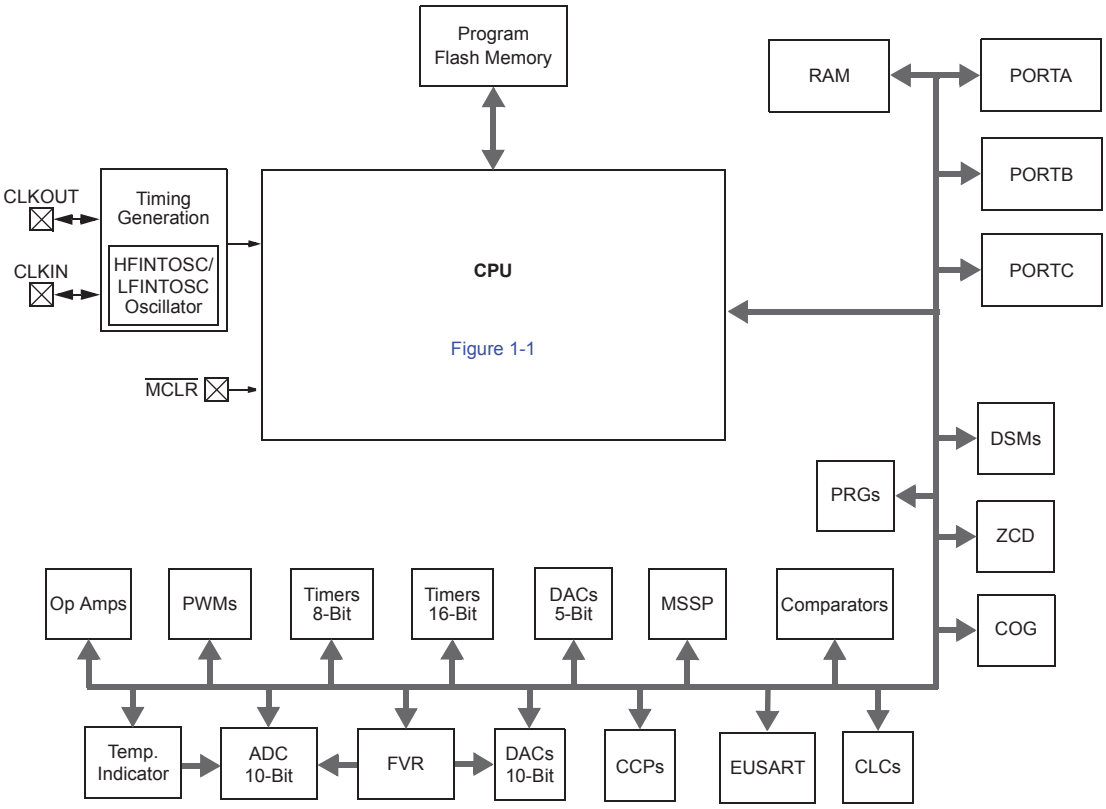
- EUSART
- MSSP

FIGURE 1-1: PIC16(L)F1764/5 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

FIGURE 1-2: PIC16(L)F1768/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16(L)F1764/5 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0+/VREF-/ DAC1REF-/DAC3REF-/ DAC1OUT1/DAC3OUT1/ ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	VREF-	AN	—	ADC negative reference.
	DAC1REF-	AN	—	DAC1 negative reference.
	DAC3REF-	AN	—	DAC3 negative reference.
	DAC1OUT1	—	AN	DAC1 voltage output.
	DAC3OUT1	—	AN	DAC3 voltage output.
	ICSPDAT	ST	CMOS	ICSP™ data I/O.
RA1/AN1/C1IN0-/C2IN0-/VREF+/ DAC1REF+/DAC3REF+/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	VREF+	AN	—	ADC positive reference.
	DAC1REF+	AN	—	DAC1 positive reference.
	DAC3REF+	AN	—	DAC3 positive reference.
	ICSPCLK	ST	—	Serial programming clock.
RA2/AN2/ZCD/T0CKI/COG1IN/ INT	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	ZCD	AN	—	Zero-Cross Detection input.
	T0CKI	TTL/ST	—	Timer0 clock input.
	COG1IN(1)	TTL/ST	—	Complementary Output Generator 1 input.
	INT(1)	TTL/ST	—	Interrupt input.
RA3/T6IN/MD1CH/$\overline{\text{MCLR}}$/VPP	RA3	TTL/ST	—	General purpose input.
	T6IN(1)	TTL/ST	—	Timer6 clock input.
	MD1CH(1)	TTL/ST	—	Data Signal Modulator 1 high carrier input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear input.
	VPP	HV	—	Programming enable.
RA4/AN3/SOSCO/T1G/ MD1CL/OSC2/CLKOUT	RA4	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	SOSCO	—	XTAL	Secondary Oscillator connection.
	T1G(1)	TTL/ST	—	Timer1 gate input.
	MD1CL(1)	TTL/ST	—	Data Signal Modulator 1 low carrier input.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1764/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/T1CKI/T2IN/CLCIN3/ MD1MOD/SOSCI/OSC1/CLKIN	RA5	TTL/ST	CMOS	General purpose I/O.
	T1CKI(1)	TTL/ST	—	Timer1 clock input.
	T2IN(1)	TTL/ST	—	Timer2 clock input.
	CLCIN3(1)	TTL/ST	—	CLC Input 3.
	MD1MOD(1)	TTL/ST	—	Data Signal Modulator modulation input.
	SOSCI	—	XTAL	Secondary Oscillator connection.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External Clock input (EC mode).
RC0/AN4/OPA1IN+/C2IN0+/ T5CKI/SCL/SCK	RC0	TTL/ST	CMOS	General purpose I/O.
	AN4	AN		ADC Channel 4 input.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	C2IN0+	AN	—	Comparator 2 positive input.
	T5CKI(1)	TTL/ST	—	Timer5 clock input.
	SCL(1,3)	I^2C	—	I^2C clock output.
	SCK(1)	TTL/ST	—	SPI clock input.
RC1/AN5/OPA1IN-/C1IN1-/ C2IN1-/T4IN/CLCIN2/SDI/SDA	RC1	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	XTAL	ADC Channel 5 input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	T4IN(1)	TTL/ST	—	Timer4 clock input.
	CLCIN2(1)	TTL/ST	—	CLC Input 2.
	SDI(1)	TTL/ST	—	SPI data input.
	SDA(1)	I^2C	—	I^2C data output.
RC2/AN6/OPA1OUT/C1IN2-/ C2IN2-/PRG1IN0	RC2	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
	C1IN2-	AN	—	Comparator 1 negative input.
	C2IN2-	AN	—	Comparator 2 negative input.
	PRG1IN0	AN	—	Ramp Generator 1 reference voltage input.
RC3/AN7/C1IN3-/C2IN3-/T5G/ CLCIN0/$\overline{SS}$	RC3	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	T5G(1)	TTL/ST	—	Timer5 gate input.
	CLCIN0(1)	TTL/ST	—	CLC Input 0.
	$\overline{SS}$(1)	TTL/ST	—	SPI Slave Select input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1764/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/T3G/PRG1R/CLCIN1/CK	RC4	TTL/ST	CMOS	General purpose I/O.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	PRG1R(1)	TTL/ST	—	Ramp generator set_rising input.
	CLCIN1(1)	TTL/ST	—	CLC Input 1.
	CK(1)	TTL/ST	—	EUSART clock input.
RC5/T3CKI/PRG1F/CCP1/RX	RC5	TTL/ST	CMOS	General purpose I/O.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	PRG1F(1)	TTL/ST	—	Ramp generator set_falling input.
	CCP1(1)	TTL/ST	—	CCP1 capture input.
	RX(1,3)	TTL/ST	—	EUSART receive input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	CCP1		CMOS	Compare/PWM1 output.
	MD1OUT		CMOS	Data Signal Modulator 1 output.
	PWM3		CMOS	PWM3 output.
	PWM5		CMOS	PWM5 output.
	COG1A		CMOS	Complementary Output Generator Output A.
	COG1B		CMOS	Complementary Output Generator Output B.
	COG1C		CMOS	Complementary Output Generator Output C.
	COG1D		CMOS	Complementary Output Generator Output D.
	SDA(3)		OD	I^2C data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX		CMOS	EUSART asynchronous TX data out.
	CK		CMOS	EUSART synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable Logic Cell 1 output.
	CLC2OUT		CMOS	Configurable Logic Cell 2 output.
	CLC3OUT		CMOS	Configurable Logic Cell 3 output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1768/9 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0+/C3IN0+/VREF-/ DAC1REF-/DAC2REF-/ DAC3REF-/DAC4REF-/ DAC1OUT1/DAC2OUT1./ DAC3OUT1/DAC4OUT1/ ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	AN0	AN	—	ADC Channel 0 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	C3IN0+	AN		Comparator C3 positive input.
	DAC1REF-	AN	—	DAC1 negative reference.
	DAC2REF-	AN	—	DAC2 negative reference.
	DAC3REF-	AN	—	DAC3 negative reference.
	DAC4REF-	AN	—	DAC4 negative reference.
	DAC1OUT1	—	AN	DAC1 voltage output.
	DAC2OUT1	—	AN	DAC2 voltage output.
	DAC3OUT1	—	AN	DAC3 voltage output.
	DAC4OUT1	—	AN	DAC4 voltage output.
	VREF-	AN	—	ADC negative reference.
	ICSPDAT	ST	CMOS	ICSP™ data I/O.
RA1/AN1/C1IN0-/C2IN0-/ C3IN0-/C4IN0-/VREF+/ DAC1REF+/DAC2REF+/ DAC3REF+/DAC4REF+/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	AN1	AN	—	ADC Channel 1 input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	C3IN0-	AN	—	Comparator C3 negative input.
	C4IN0-	AN	—	Comparator C4 negative input.
	DAC1REF+	AN	—	DAC1 positive reference.
	DAC2REF+	AN	—	DAC2 positive reference.
	DAC3REF+	AN	—	DAC3 positive reference.
	DAC4REF+	AN	—	DAC4 positive reference.
	VREF+	AN	—	ADC positive reference.
	ICSPCLK	ST	—	Serial programming clock.
RA2/AN2/ZCD/T0CKI/COG1IN/ COG2IN/INT	RA2	TTL/ST	CMOS	General purpose I/O.
	AN2	AN	—	ADC Channel 2 input.
	ZCD	AN	—	Zero-Cross Detection input.
	T0CKI(1)	TTL/ST	—	Timer0 clock input.
	COG1IN(1)	TTL/ST	—	Complementary Output Generator 1 input.
	COG2IN(1)	TTL/ST	—	Complementary Output Generator 2 input.
	INT(1)	TTL/ST	—	Interrupt input.
RA3/T6IN/MD1CH/MD2CH/ $\overline{\text{MCLR}}$/VPP	RA3	TTL/ST	—	General purpose input.
	T6IN(1)	TTL/ST	—	Timer6 clock input.
	MD1CH(1)	TTL/ST	—	Data Signal Modulator 1 high carrier input.
	MD2CH(1)	TTL/ST	—	Data Signal Modulator 2 high carrier input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear input.
	VPP	HV	—	Programming enable.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1768/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA4/AN3/SOSCO/T1G/ DSM1CL/DSM2CL/OSC2/ CLKOUT	RA4	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	SOSCO	—	XTAL	Secondary Oscillator connection.
	T1G(1)	TTL/ST	—	Timer1 gate input.
	DSM1CL(1)	TTL/ST	—	Data Signal Modulator 1 low carrier input.
	DSM2CL(1)	TTL/ST	—	Data Signal Modulator 2 low carrier input.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
RA5/T1CKI/T2IN/CLCIN3/ DSM1MOD/DSM2MOD/ SOSCI/OSC1/CLKIN	RA5	TTL/ST	CMOS	General purpose I/O.
	T1CKI(1)	TTL/ST	—	Timer1 clock input.
	T2IN(1)	TTL/ST	—	Timer2 clock input.
	CLCIN3(1)	TTL/ST	—	CLC Input 3.
	DSM1MOD(1)	TTL/ST	—	Data Signal Modulator 1 modulation input.
	DSM2MOD(1)	TTL/ST	—	Data Signal Modulator 2 modulation input.
	SOSCI	XTAL	—	Secondary Oscillator connection.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External Clock input (EC mode).
RB4/AN10/OPA1IN0-/SDI/SDA	RB4	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	OPA1IN0-	AN	—	Operational Amplifier 1 inverting input.
	SDI(1)	TTL/ST	—	SPI data input.
	SDA(1,3)	I^2C	—	I^2C data output.
RB5/AN11/OPA1IN0+/RX	RB5	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	OPA1IN0+	AN	—	Operational Amplifier 1 non-inverting input.
	RX(1,3)	TTL/ST	—	EUSART receive input.
RB6/C1IN1+/C3IN1+/SCK/SCL	RB6	TTL/ST	CMOS	General purpose I/O.
	C1IN1+	AN	—	Comparator C1 positive input.
	C3IN1+	AN	—	Comparator C3 positive input.
	SCK(1)	TTL/ST	—	SPI clock input.
	SCL(1,3)	I^2C	—	I^2C clock output.
RB7/C2IN1+/C4IN1+/CK	RB7	TTL/ST	CMOS	General purpose I/O.
	C2IN1+	AN	—	Comparator C2 positive input.
	C4IN1+	AN	—	Comparator C4 positive input.
	CK(1)	TTL/ST	—	EUSART clock input.
RC0/AN4/C2IN0+/C4IN0+/ T5CKI	RC0	TTL/ST	CMOS	General purpose I/O.
	AN4	AN		ADC Channel 4 input.
	C2IN0+	AN	—	Comparator C2 positive input.
	C4IN0+	AN	—	Comparator C4 positive input.
	T5CKI(1)	TTL/ST	—	Timer5 clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1768/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/AN5/C1IN1-/C2IN1-/ C3IN1-/C4IN1-/T4IN/CLCIN2	RC1	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	XTAL	ADC Channel 5 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	C3IN1-	AN	—	Comparator 3 negative input.
	C4IN1-	AN	—	Comparator 4 negative input.
	T4IN(1)	TTL/ST	—	Timer4 clock input.
	CLCIN2(1)	TTL/ST	—	CLC Input 2.
RC2/AN6/OPA1OUT/OPA2IN1-/ OPA2IN1+/C1IN2-/C2IN2-/ PRG1IN0/PRG2IN1	RC2	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
	OPA2IN1-	AN		Operational Amplifier 2 inverting input.
	OPA2IN1+	AN		Operational Amplifier 2 non-inverting input.
	C1IN2-	AN	—	Comparator 1 negative input.
	C2IN2-	AN	—	Comparator 2 negative input.
	PRG1IN0	AN	—	Ramp Generator 1 reference voltage input.
	PRG2IN1	AN	—	Ramp Generator 2 reference voltage input.
RC3/AN7/OPA2OUT/OPA1IN1-/ OPA1IN1+/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/PRG1IN1/ PRG2IN0/T5G/CCP2/CLCIN0	RC3	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
	OPA1IN1-	AN		Operational Amplifier 1 inverting input.
	OPA1IN1+	AN		Operational Amplifier 1 non-inverting input.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	C3IN3-	AN	—	Comparator 3 negative input.
	C4IN3-	AN	—	Comparator 4 negative input.
	PRG1IN1	AN	—	Ramp Generator 1 reference voltage input.
	PRG2IN0	AN	—	Ramp Generator 2 reference voltage input.
	T5G(1)	TTL/ST	—	Timer5 gate input.
	CCP2(1)	TTL/ST	—	CCP2 capture input.
	CLCIN0(1)	TTL/ST	—	CLC Input 0.
RC4/T3G/PRG1R/PRG2R/ CLCIN1	RC4	TTL/ST	CMOS	General purpose I/O.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	PRG1R(1)	TTL/ST	—	Ramp Generator 1 set_rising input.
	PRG2R(1)	TTL/ST	—	Ramp Generator 2 set_rising input.
	CLCIN1(1)	TTL/ST	—	CLC Input 1.
RC5/T3CKI/PRG1F/PRG2F/ CCP1	RC5	TTL/ST	CMOS	General purpose I/O.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	PRG1F(1)	TTL/ST	—	Ramp Generator 1 set_falling input.
	PRG2F(1)	TTL/ST	—	Ramp Generator 2 set_falling input.
	CCP1(1)	TTL/ST	—	CCP1 capture input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1768/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC6/AN8/OPA2IN0-/$\overline{SS}$	RC6	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN0-	AN	—	Operational Amplifier 2 inverting input.
	$\overline{SS}$(1)	TTL/ST	—	SPI Slave Select input.
RC7/AN9/OPA2IN0+	RC7	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	OPA2IN0+	AN	—	Operational Amplifier 2 non-inverting input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	C3OUT		CMOS	Comparator 3 output.
	C4OUT		CMOS	Comparator 4 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	MD1OUT		CMOS	Data Signal Modulator 1 output.
	MD2OUT		CMOS	Data Signal Modulator 2 output.
	PWM3		CMOS	PWM3 output.
	PWM4		CMOS	PWM4 output.
	PWM5		CMOS	PWM5 output.
	PWM6		CMOS	PWM6 output.
	COG1A		CMOS	Complementary Output Generator 1 Output A.
	COG1B		CMOS	Complementary Output Generator 1 Output B.
	COG1C		CMOS	Complementary Output Generator 1 Output C.
	COG1D		CMOS	Complementary Output Generator 1 Output D.
	COG2A		CMOS	Complementary Output Generator 2 Output A.
	COG2B		CMOS	Complementary Output Generator 2 Output B.
	COG2C		CMOS	Complementary Output Generator 2 Output C.
	COG2D		CMOS	Complementary Output Generator 2 Output D.
	SDA(3)		OD	I^2C data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX		CMOS	EUSART asynchronous TX data out.
	CK		CMOS	EUSART synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable Logic Cell 1 output.
	CLC2OUT		CMOS	Configurable Logic Cell 2 output.
	CLC3OUT		CMOS	Configurable Logic Cell 3 output.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

1.2 Peripheral Connection Matrix

Input selection multiplexers on many of the peripherals enable selecting the output of another peripheral, such that the signal path is contained entirely within the device. Although the peripheral output can also be routed to a pin with the PPS selection feature, it is not necessary to do so. Table 1-4 shows all the possible inter-peripheral signal connections. Please refer to the corresponding peripheral section to obtain the multiplexer selection codes for the desired connection.

TABLE 1-4: PERIPHERAL CONNECTION MATRIX

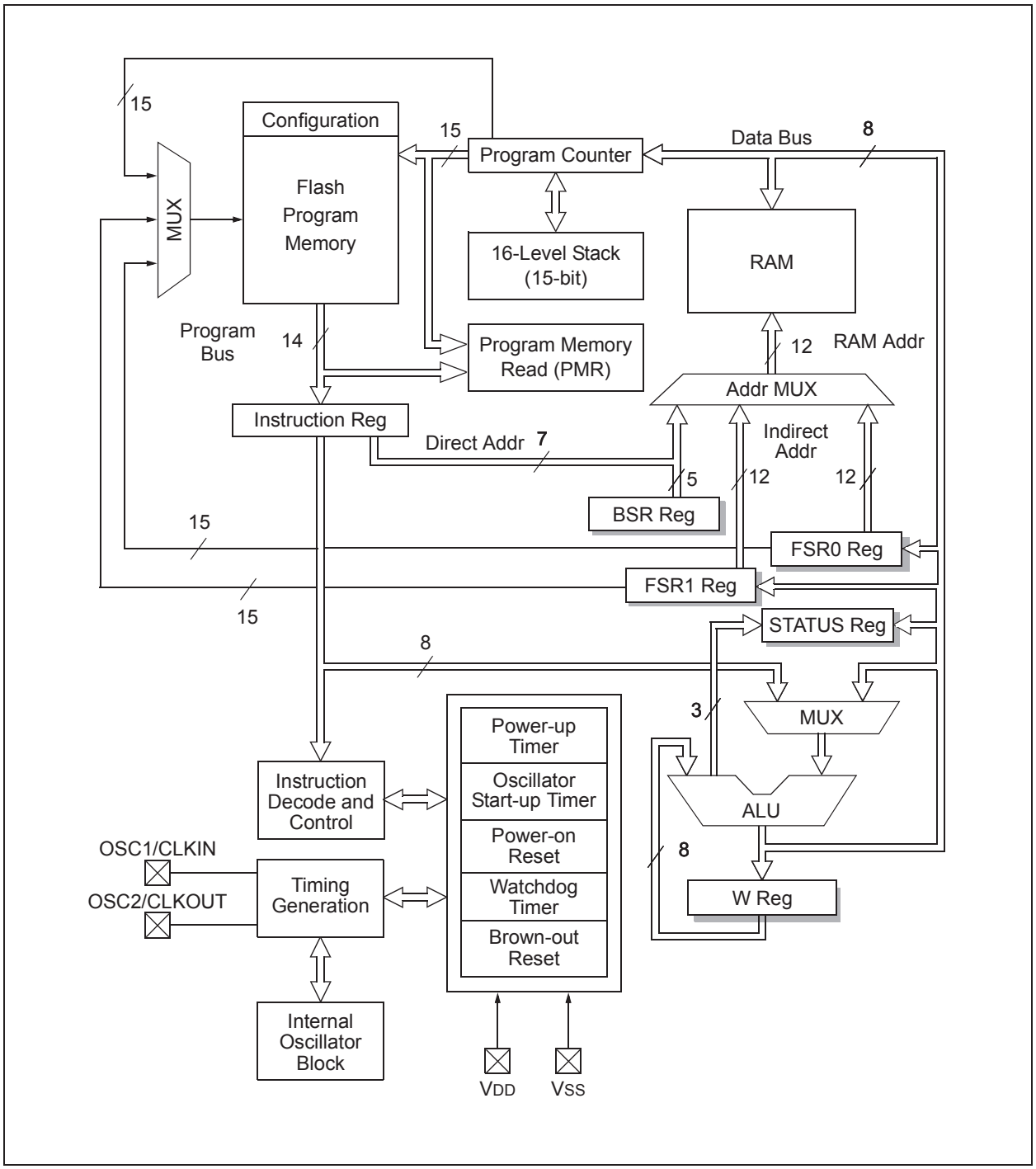
	Peripheral Input																							
Peripheral Output	**ADC Trigger**	**COG Clock**	**COG Rising/Falling**	**COG Shutdown**	**10-Bit DAC**	**5-Bit DAC**	**PRG Analog Input**	**PRG Rising/Falling**	**Comparator +**	**Comparator -**	**CLC**	**DSM CH**	**DSM CL**	**DSM Mod**	**Op Amp +**	**Op Amp -**	**Op Amp Override**	**10-Bit PWM**	**16-Bit PWM**	**CCP Capture**	**CCP Clock**	**Timer2/4/6 Clock**	**Timer2/4/6 Reset**	**Timer1/3/5 Gate**	**Timer0 Clock**
FVR					●	●	●		●	●					●	●									
ZCD											●						●					●			
PRG									●						●	●									
10-Bit DAC							●		●						●	●									
5-Bit DAC							●		●						●	●									
CCP	●		●					●			●	●	●	●			●						●		
Comparator (sync)	●							●			●						●			●			●	●	
Comparator (async)			●	●										●											
CLC	●		●	●							●	●	●	●			●			●		●	●		
DSM																									
COG																	●								
EUSART TX/CK											●			●											
EUSART DT											●			●											
MSSP SCK/SCL											●			●											
MSSP SDO/SDA											●			●											
Op Amp							●																		
10-Bit PWM	●		●					●			●	●	●	●			●						●		
16-Bit PWM	●		●					●			●	●	●	●			●						●		
Timer0 Overflow	●										●													●	
Timer2 = T2PR				●							●							●			●		●		
Timer4 = T4PR				●							●							●			●		●		
Timer6 = T6PR				●							●							●			●		●		
Timer2 Postscale	●			●							●							●			●		●		
Timer4 Postscale	●			●							●							●			●		●		
Timer6 Postscale	●			●							●							●			●		●		
Timer1 Overflow	●										●							●			●				
Timer3 Overflow	●										●							●			●				
Timer5 Overflow	●										●							●			●				
SOSC																			●			●			
FOSC/4		●																				●			
FOSC		●									●	●	●						●			●			
HFINTOSC		●									●	●	●						●			●			
LFINTOSC											●								●			●			
MFINTOSC																						●			
IOCIF											●									●	●				
PPS Input Pin			●	●				●				●	●	●						●	●	●	●	●	●

2.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-Level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"** for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a Software Reset. See **Section 3.5 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSRs). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSRn points to program memory, there is one additional instruction cycle in instructions using INDFn to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 35.0 "Instruction Set Summary"** for more details.

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory:
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory:
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

Note 1: The method to access Flash memory through the PMCON registers is described in **Section 10.0 "Flash Program Memory Control"**.

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit Program Counter (PC) capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1764/5/8/9 family. Accessing a location above these boundaries will cause a wrap around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 3-1).

3.2 High-Endurance Flash

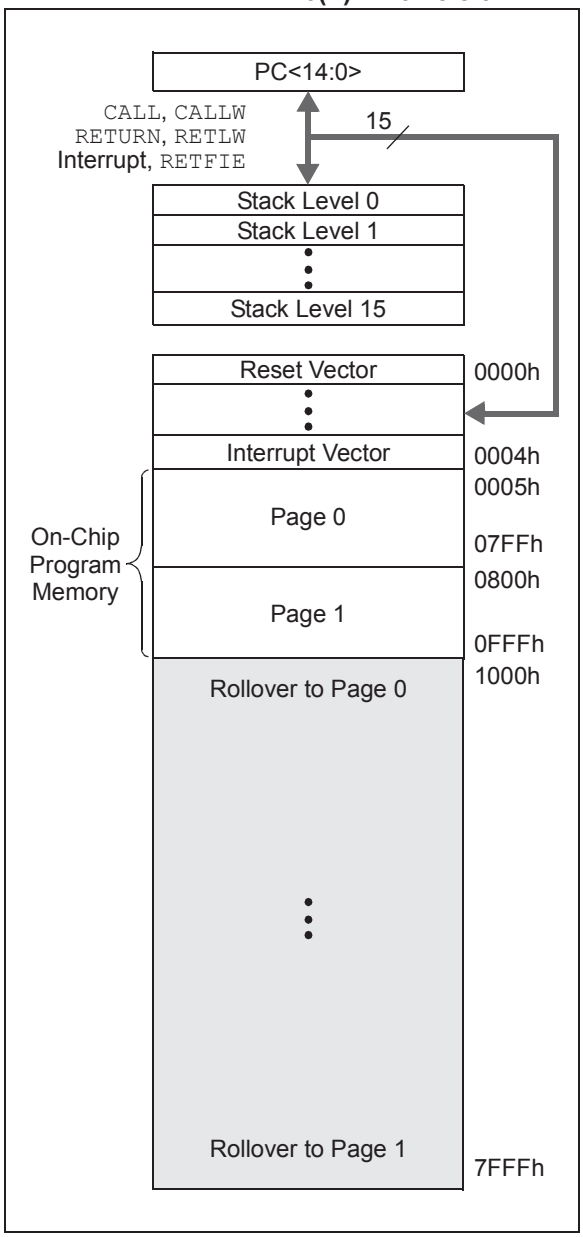
This device has a 128-byte section of high-endurance Program Flash Memory (PFM) in lieu of data EEPROM. This area is especially well suited for nonvolatile data storage that is expected to be updated frequently over the life of the end product. See **Section 10.2 "Flash Program Memory Overview"** for more information on writing data to PFM. See **Section 3.2.1.2 "Indirect Read with FSRn"** for more information about using the FSRn registers to read byte data stored in PFM.

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range(1)
PIC16(L)F1764	4,096	0FFFh	0F80h-0FFFh
PIC16(L)F1765	8,192	1FFFh	1F80h-1FFFh
PIC16(L)F1768	4,096	0FFFh	0F80h-0FFFh
PIC16(L)F1769	8,192	1FFFh	1F80h-1FFFh

Note 1: High-endurance Flash applies to the low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1764/5/8/9



3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of `RETLW` instructions. The second method is to set an FSRn to point to the program memory.

3.2.1.1 `RETLW` Instruction

The `RETLW` instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: `RETLW` INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The `BRW` instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the `BRW` instruction is not available, so the older table read method must be used.

3.2.1.2 Indirect Read with FSRn

The program memory can be accessed as data by setting bit 7 of the FSRnH register and reading the matching INDFn register. The `MOVIW` instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDFn registers. Instructions that access the program memory via the FSRn require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSRn.

The high directive will set bit 7 if a label points to a location in program memory.